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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	27648
Number of I/O	60
Number of Gates	90000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	180-WFQFN Dual Rows, Exposed Pad
Supplier Device Package	180-QFN (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/afs090-2qng180

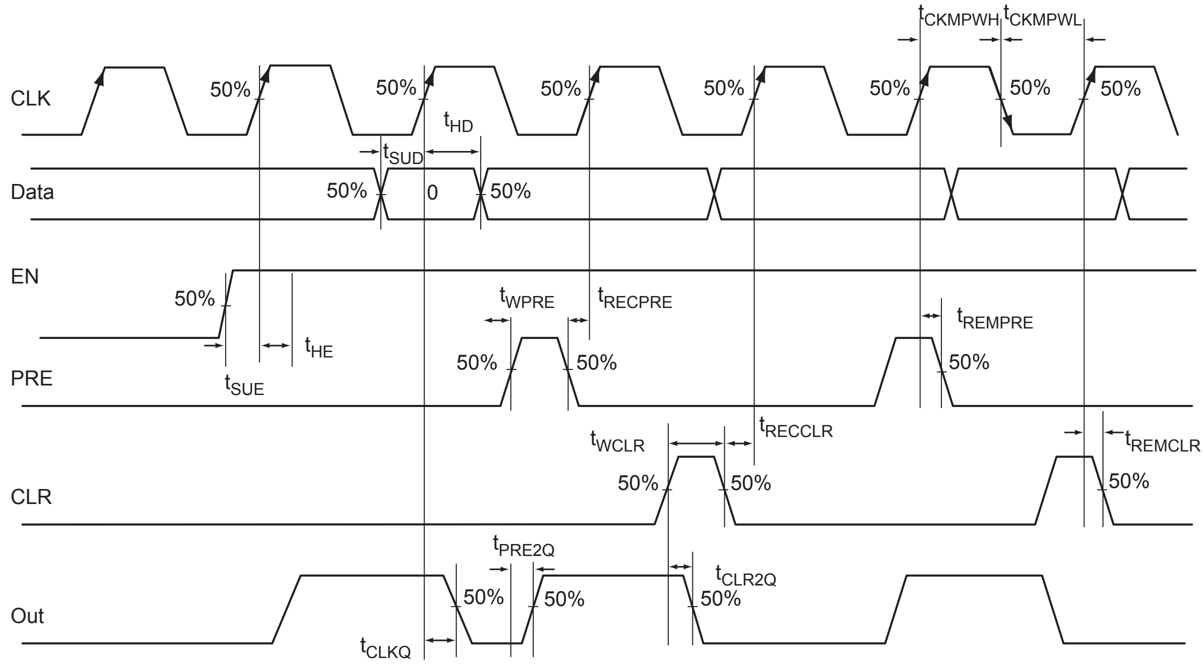


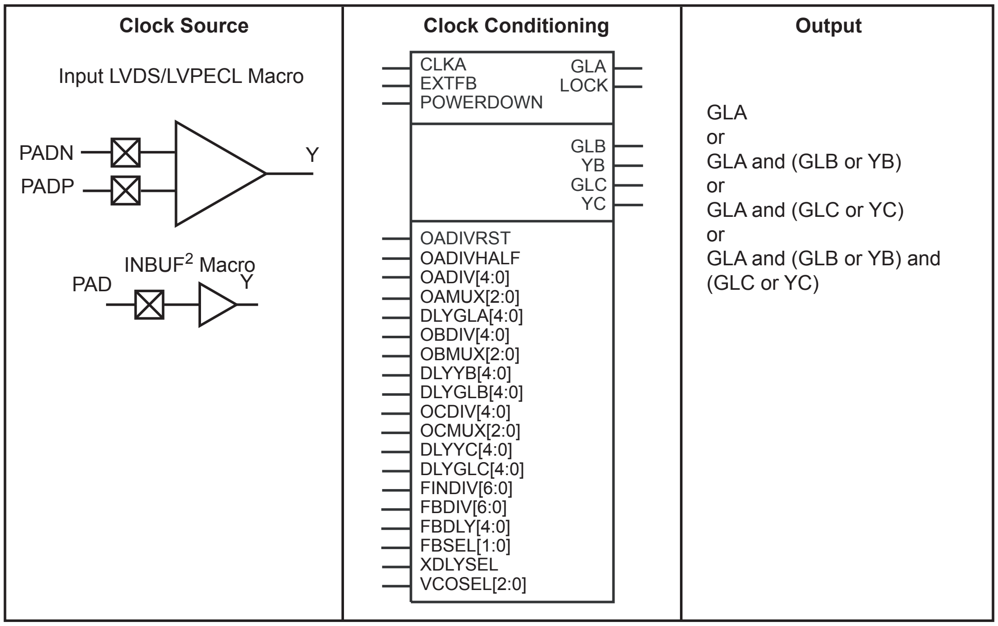
Figure 2-6 • **Sequential Timing Model and Waveforms**

Sequential Timing Characteristics

Table 2-2 • **Register Delays**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	ns
t_{SUD}	Data Setup Time for the Core Register	0.43	0.49	0.57	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.45	0.52	0.61	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.37	0.43	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.41	0.48	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Notes:

1. *Visit the Microsemi SoC Products Group website for application notes concerning dynamic PLL reconfiguration. Refer to the "PLL Macro" section on page 2-27 for signal descriptions.*
2. *Many specific INBUF macros support the wide variety of single-ended and differential I/O standards for the Fusion family.*
3. *Refer to the IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide for more information.*

***Figure 2-19 •* Fusion CCC Options: Global Buffers with the PLL Macro**

***Table 2-11 •* Available Selections of I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

CLKBUF Macros
CLKBUF_LVCMOS5
CLKBUF_LVCMOS33[1]
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_LVDS[2]
CLKBUF_LVPECL

Notes:

1. *This is the default macro. For more details, refer to the IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide.*
2. *The B-LVDS and M-LVDS standards are supported with CLKBUF_LVDS.*

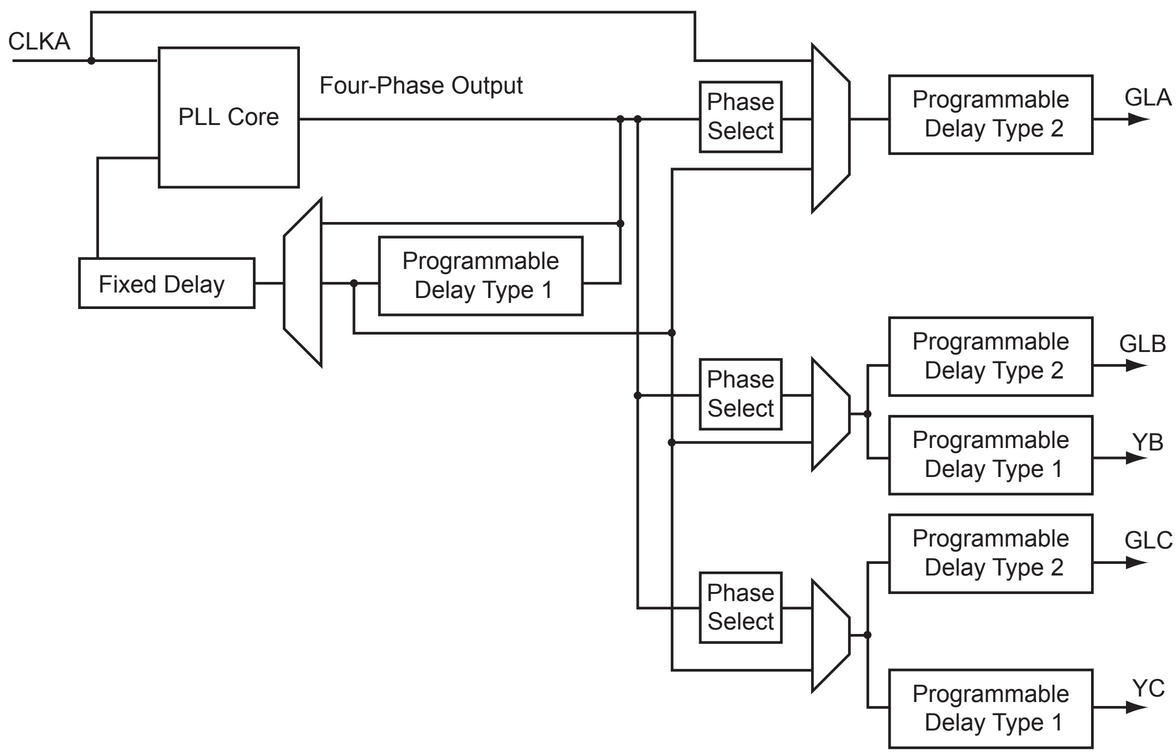
CCC Physical Implementation

The CCC circuit is composed of the following (Figure 2-23):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-23 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability (not shown)

CCC Programming

The CCC block is fully configurable. It is configured via static flash configuration bits in the array, set by the user in the programming bitstream, or configured through an asynchronous dedicated shift register, dynamically accessible from inside the Fusion device. The dedicated shift register permits changes of parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Note: Clock divider and multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

***Figure 2-23* • PLL Block**

Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to zero) any page within the FB.

The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in Figure 2-37.

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = '01')
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = '01')
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = '11')
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = '10')

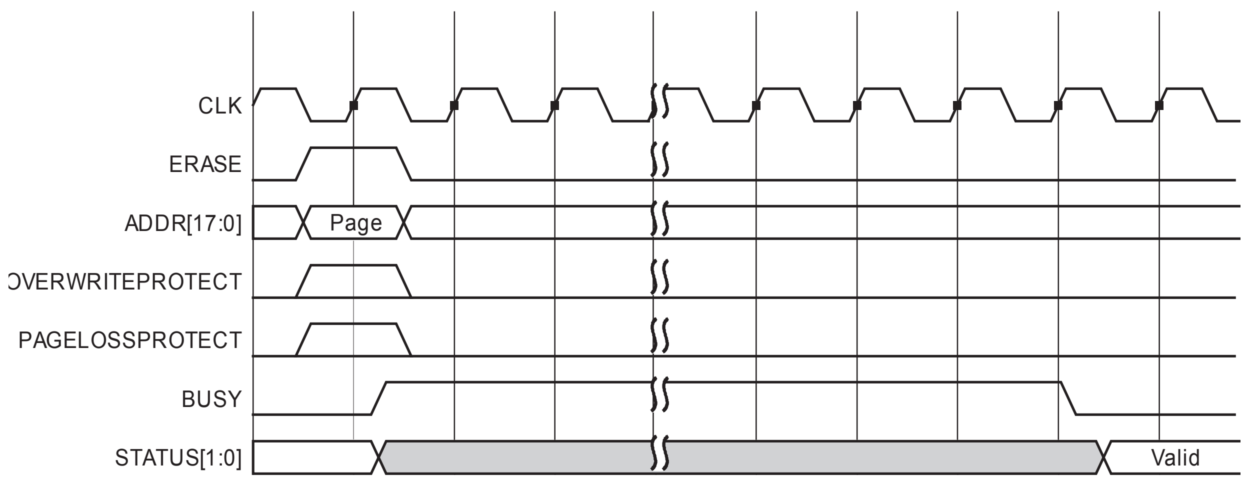


***Figure 2-37* • FB Erase Page Waveform**

Read Operation

Read operations are designed to read data from the FB Array, Page Buffer, Block Buffer, or status registers. Read operations support a normal read and a read-ahead mode (done by asserting READNEXT). Also, the timing for Read operations is dependent on the setting of PIPE.

The following diagrams illustrate representative timing for Non-Pipe Mode (Figure 2-38) and Pipe Mode (Figure 2-39) reads of the flash memory block interface.

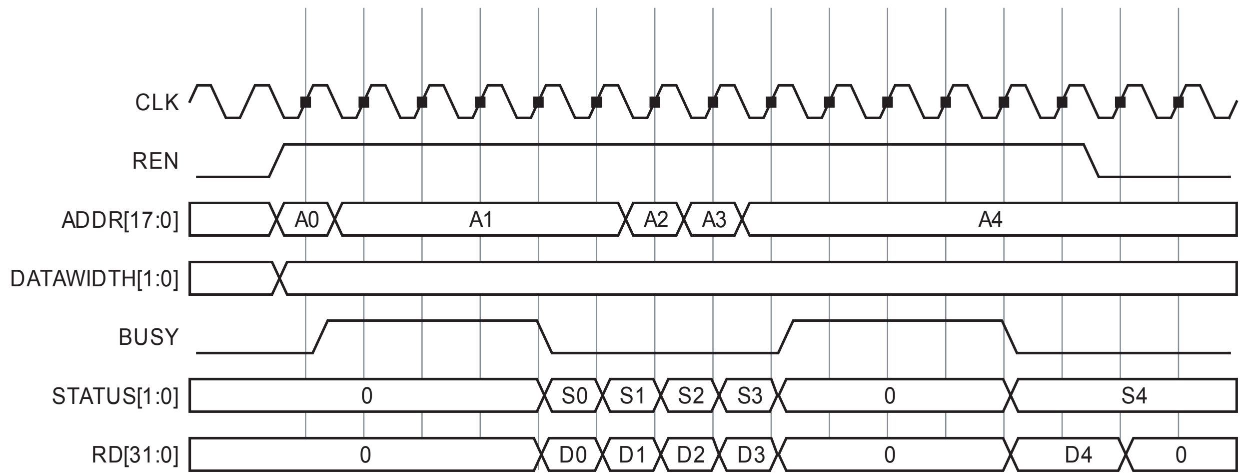


Figure 2-38 • Read Waveform (Non-Pipe Mode, 32-bit access)

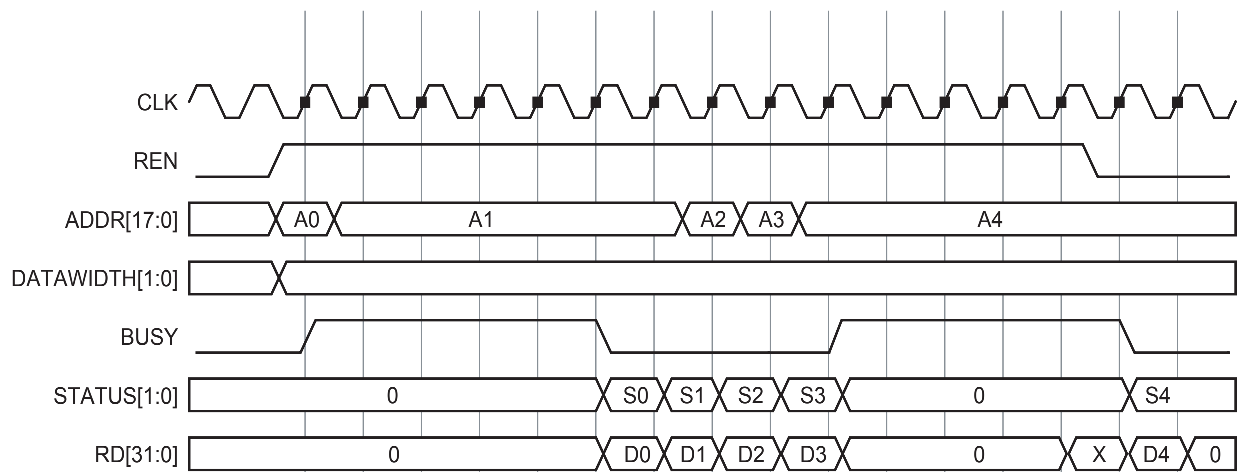


Figure 2-39 • Read Waveform (Pipe Mode, 32-bit access)

SRAM Characteristics

Timing Waveforms

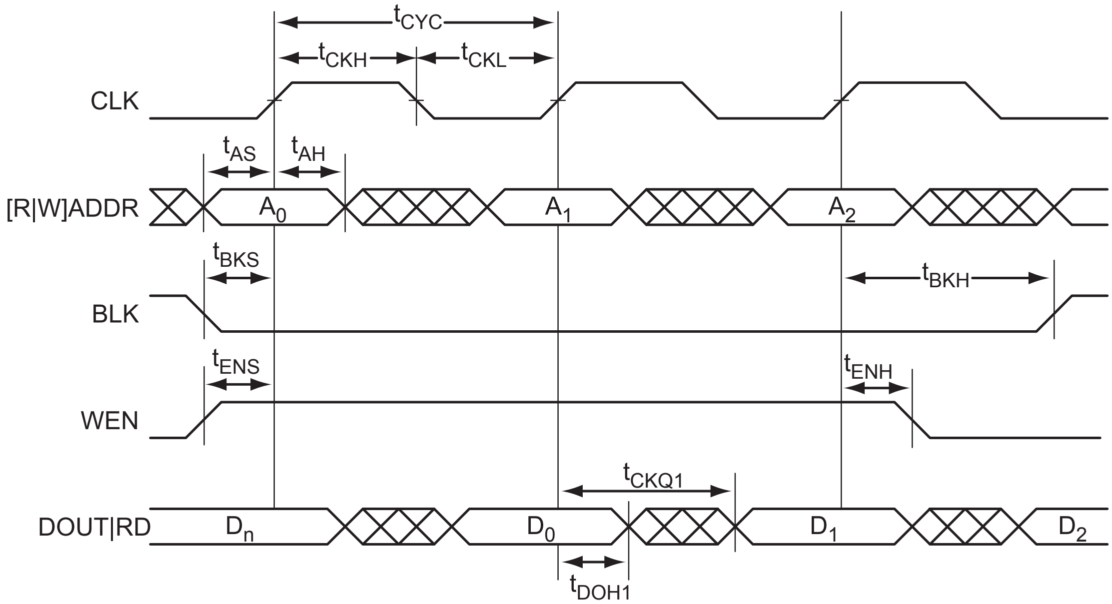


Figure 2-50 • **RAM Read for Flow-Through Output. Applicable to both RAM4K9 and RAM512x18.**

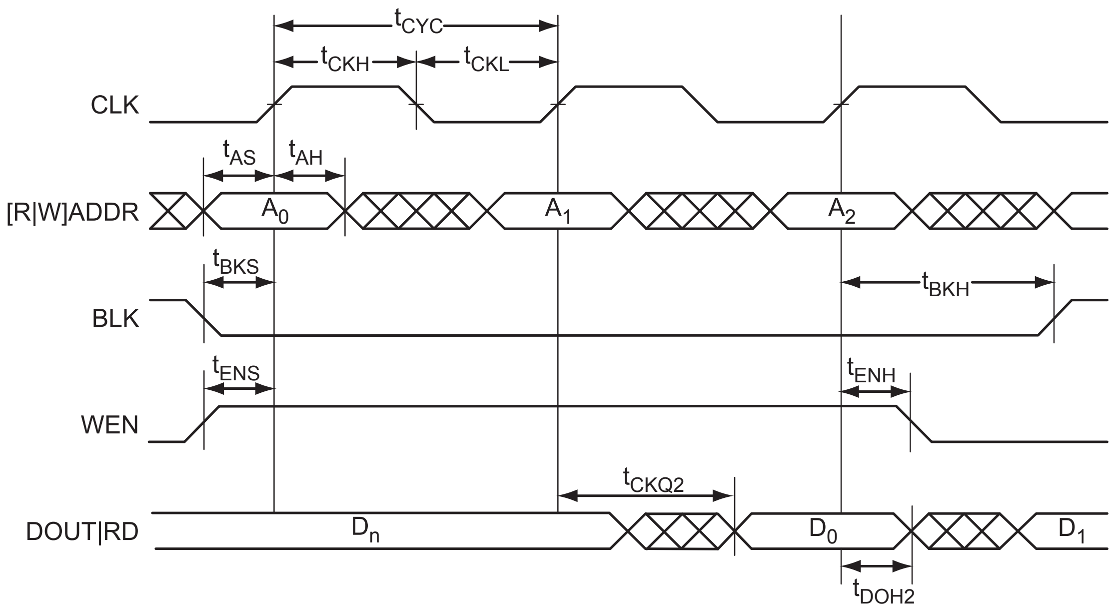


Figure 2-51 • **RAM Read for Pipelined Output. Applicable to both RAM4K9 and RAM512x18.**

Table 2-32 **• RAM512X18**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.09	0.10	0.12	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	0.08	ns
t_{DS}	Input data (WD) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.59	0.50	0.44	ns
t_{RSTBQ}[1]	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For the derating values at specific junction temperature and voltage supply levels, refer to* *Table 3-7 on page 3-9*.

ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode so the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V VCC supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of the MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-80). Table 2-40 defines which Analog Quad inputs are associated with which specific analog MUX channels. The number of Analog Quads present is device-dependent; refer to the family list in the "Fusion Family" table on page I of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both VCC and the internal temperature diode remain on Channels 0 and 31, respectively. To sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a five-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-39.

***Table 2-39* • Channel Selection**

Channel Number	CHNUMBER[4:0]
0	00000
1	00001
2	00010
3	00011
. . .	. . .
30	11110
31	11111

Table 2-40 shows the correlation between the analog MUX input channels and the analog input pins.

***Table 2-40* • Analog MUX Channels**

Analog MUX Channel	Signal	Analog Quad Number
0	Vcc_analog	
1	AV0	Analog Quad 0
2	AC0	
3	AT0	
4	AV1	Analog Quad 1
5	AC1	
6	AT1	
7	AV2	Analog Quad 2
8	AC2	
9	AT2	
10	AV3	Analog Quad 3
11	AC3	
12	AT3	
13	AV4	Analog Quad 4
14	AC4	
15	AT4	

Table 2-88 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions
Applicable to Standard I/Os

I/O Standard	Drive Strength	Slew Rate	VIL		VIH		VOL	VOH	IOL	IOH
			Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2

Note: Currents are measured at 85°C junction temperature.

Table 2-89 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions
Applicable to All I/O Bank Types

DC I/O Standards	Commercial[1]		Industrial[2]	
	IIL[3]	IIH[4]	IIL[3]	IIH[4]
	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15
3.3 V GTL	10	10	15	15
2.5 V GTL	10	10	15	15
3.3 V GTL+	10	10	15	15
2.5 V GTL+	10	10	15	15
HSTL (I)	10	10	15	15
HSTL (II)	10	10	15	15
SSTL2 (I)	10	10	15	15
SSTL2 (II)	10	10	15	15
SSTL3 (I)	10	10	15	15
SSTL3 (II)	10	10	15	15

Notes:

1. *Commercial range (0°C < T_J < 85°C)*
2. *Industrial range (–40°C < T_J < 100°C)*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

Table 2-105 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	–1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	–2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
8 mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	–1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	–2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	–1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	–2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	–1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	–2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	–1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	–2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

***Table 2-122* • 1.8 V LVCMOS Low Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	15.53	0.04	1.31	0.43	14.11	15.53	2.78	1.60	16.35	17.77	ns
	–1	0.56	13.21	0.04	1.11	0.36	12.01	13.21	2.36	1.36	13.91	15.11	ns
	–2[2]	0.49	11.60	0.03	0.98	0.32	10.54	11.60	2.07	1.19	12.21	13.27	ns
4 mA	Std.	0.66	10.48	0.04	1.31	0.43	10.41	10.48	3.23	2.73	12.65	12.71	ns
	–1	0.56	8.91	0.04	1.11	0.36	8.86	8.91	2.75	2.33	10.76	10.81	ns
	–2	0.49	7.82	0.03	0.98	0.32	7.77	7.82	2.41	2.04	9.44	9.49	ns
8 mA	Std.	0.66	8.05	0.04	1.31	0.43	8.20	7.84	3.54	3.27	10.43	10.08	ns
	–1	0.56	6.85	0.04	1.11	0.36	6.97	6.67	3.01	2.78	8.88	8.57	ns
	–2	0.49	6.01	0.03	0.98	0.32	6.12	5.86	2.64	2.44	7.79	7.53	ns
12 mA	Std.	0.66	7.50	0.04	1.31	0.43	7.64	7.30	3.61	3.41	9.88	9.53	ns
	–1	0.56	6.38	0.04	1.11	0.36	6.50	6.21	3.07	2.90	8.40	8.11	ns
	–2	0.49	5.60	0.03	0.98	0.32	5.71	5.45	2.69	2.55	7.38	7.12	ns
16 mA	Std.	0.66	7.29	0.04	1.31	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	–1	0.56	6.20	0.04	1.11	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	–2	0.49	5.45	0.03	0.98	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to *Table 3-7 on page 3-9.*

SSTL2 Class II

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-159 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class II	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
18 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.35	VCCI – 0.43	18	18	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

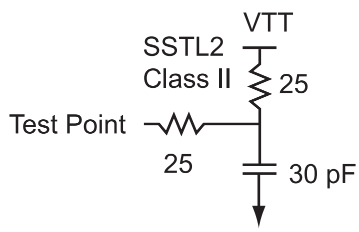


Figure 2-131 • AC Loading

Table 2-160 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-161 • SSTL 2 Class II
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.17	0.04	1.33	0.43	2.21	1.77			4.44	4.01	ns
–1	0.56	1.84	0.04	1.14	0.36	1.88	1.51			3.78	3.41	ns
–2	0.49	1.62	0.03	1.00	0.32	1.65	1.32			3.32	2.99	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Output DDR

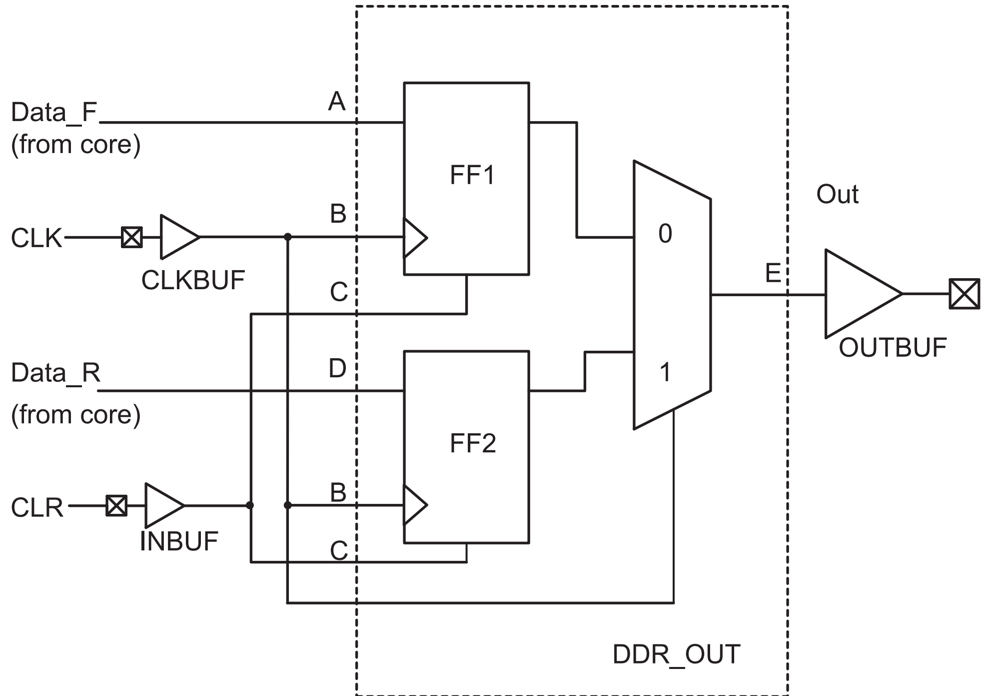


Figure 2-144 **• Output DDR Timing Model**

Table 2-181 **• Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF **Analog Reference Ground**

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA **Ground (analog)**

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDAQ **Ground (analog quiet)**

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDAQ and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables.

GNDNVM **Flash Memory Ground**

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC **Oscillator Ground**

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A **Analog Power Supply (1.5 V)**

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N **Negative 3.3 V Output**

This is the –3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to ground.

VCC33PMP **Analog Power Supply (3.3 V)**

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM **Flash Memory Block Power Supply (1.5 V)**

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with VCCNVM.

VCCOSC **Oscillator Power Supply (3.3 V)**

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33 pump, and eNVM operation. VCCOSC is off only when VCCA is off. VCCOSC must be powered whenever the Fusion device needs to function.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a Fusion device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the Fusion device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. B*x* is the I/O bank number. There are either four (AFS090 and AFS250) or five (AFS600 and AFS1500) I/O banks on the Fusion devices plus a dedicated VJTAG bank.

Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

VCCPLA/B **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V, where A and B refer to the PLL. AFS090 and AFS250 each have a single PLL. The AFS600 and AFS1500 devices each have two PLLs. Microsemi recommends tying VCCPLX to VCC and using proper filtering circuits to decouple VCC noise from PLL.

If unused, VCCPLA/B should be tied to GND.

VCOMPLA/B **Ground for West and East PLL**

VCOMPLA is the ground of the west PLL (CCC location F) and VCOMPLB is the ground of the east PLL (CCC location C).

VJTAG **JTAG Supply Voltage**

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a Fusion device is in a JTAG chain of interconnected boards and it is desired to power down the board containing the Fusion device, this may be done provided both VJTAG and VCC to the Fusion part remain powered; otherwise, JTAG signals will not be able to transition the Fusion device, even in bypass mode.

VPUMP **Programming Supply Voltage**

Fusion devices support single-voltage ISP programming of the configuration flash and FlashROM. For programming, VPUMP should be in the 3.3 V +/-5% range. During normal device operation, VPUMP can be left floating or can be tied to any voltage between 0 V and 3.6 V.

When the VPUMP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Table 3-3 • Input Resistance of Analog Pads

Pads	Pad Configuration	Prescaler Range	Input Resistance to Ground
AV, AC	Analog Input (direct input to ADC)	–	2 kΩ (typical)
		–	> 10 MΩ
	Analog Input (positive prescaler)	+16 V to +2 V	1 MΩ (typical)
		+1 V to +0.125 V	> 10 MΩ
	Analog Input (negative prescaler)	–16 V to –2 V	1 MΩ (typical)
		–1 V to –0.125 V	> 10 MΩ
	Digital input	+16 V to +2 V	1 MΩ (typical)
	Current monitor	+16 V to +2 V	1 MΩ (typical)
		–16 V to –2 V	1 MΩ (typical)
AT	Analog Input (direct input to ADC)	–	1 MΩ (typical)
	Analog Input (positive prescaler)	+16 V, +4 V	1 MΩ (typical)
	Digital input	+16 V, +4 V	1 MΩ (typical)
	Temperature monitor	+16 V, +4 V	> 10 MΩ

Table 3-4 • Overshoot and Undershoot Limits [1]

VCCI	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3.0 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at a junction temperature of 85°C.*
2. *The duration is allowed at one cycle out of six clock cycle. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*

Table 3-9 • **AFS600 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
ICC[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		13	25	mA
			T_J = 85°C		20	45	mA
			T_J=100°C		25	75	mA
		Standby mode[5] or Sleep mode[6], VCC = 0 V			0	0	µA
ICC33[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	13	mA
			T_J = 85°C		10.7	14	mA
			T_J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.31	2	mA
			T_J = 85°C		0.35	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63 V	T_J = 25°C		2.8	3.6	mA
			T_J = 85°C		2.9	4	mA
			T_J = 100°C		3.5	6	mA
		Sleep mode[6], V_{CC33} = 3.63 V	T_J = 25°C		17	19	µA
			T_J = 85°C		18	20	µA
			T_J = 100°C		24	25	µA
ICCI[3]	I/O quiescent current	Operational standby[4], VCCIx = 3.63 V	T_J = 25°C		417	648	µA
			T_J = 85°C		417	648	µA
			T_J = 100°C		417	649	µA
IJTAG	JTAG I/O quiescent current	Operational standby[4], VJTAG = 3.63 V	T_J = 25°C		80	100	µA
			T_J = 85°C		80	100	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VJTAG = 0 V			0	0	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

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Pin Number	AFS090 Function	AFS250 Function	AFS600 Function	AFS1500 Function
K9	VCC	VCC	VCC	VCC
K10	GND	GND	GND	GND
K11	NC	GDC2/IO57PPB1V0	GDC2/IO57PPB2V0	GDC2/IO84PPB2V0
K12	GND	GND	GND	GND
K13	NC	GDA0/IO54NDB1V0	GDA0/IO54NDB2V0	GDA0/IO81NDB2V0
K14	NC	GDA2/IO55PPB1V0	GDA2/IO55PPB2V0	GDA2/IO82PPB2V0
K15	VCCIB1	VCCIB1	VCCIB2	VCCIB2
K16	NC	GDB1/IO53PPB1V0	GDB1/IO53PPB2V0	GDB1/IO80PPB2V0
L1	NC	GEC1/IO63PDB3V0	GEC1/IO63PDB4V0	GEC1/IO90PDB4V0
L2	NC	GEC0/IO63NDB3V0	GEC0/IO63NDB4V0	GEC0/IO90NDB4V0
L3	NC	GEB1/IO62PDB3V0	GEB1/IO62PDB4V0	GEB1/IO89PDB4V0
L4	NC	GEB0/IO62NDB3V0	GEB0/IO62NDB4V0	GEB0/IO89NDB4V0
L5	NC	IO60NDB3V0	IO60NDB4V0	IO87NDB4V0
L6	NC	GEC2/IO60PDB3V0	GEC2/IO60PDB4V0	GEC2/IO87PDB4V0
L7	GNDA	GNDA	GNDA	GNDA
L8	AC0	AC0	AC2	AC2
L9	AV2	AV2	AV4	AV4
L10	AC3	AC3	AC5	AC5
L11	PTEM	PTEM	PTEM	PTEM
L12	TDO	TDO	TDO	TDO
L13	VJTAG	VJTAG	VJTAG	VJTAG
L14	NC	IO57NPB1V0	IO57NPB2V0	IO84NPB2V0
L15	GDB2/IO41PPB1V0	GDB2/IO56PPB1V0	GDB2/IO56PPB2V0	GDB2/IO83PPB2V0
L16	NC	IO55NPB1V0	IO55NPB2V0	IO82NPB2V0
M1	GND	GND	GND	GND
M2	NC	GEA1/IO61PDB3V0	GEA1/IO61PDB4V0	GEA1/IO88PDB4V0
M3	NC	GEA0/IO61NDB3V0	GEA0/IO61NDB4V0	GEA0/IO88NDB4V0
M4	VCCIB3	VCCIB3	VCCIB4	VCCIB4
M5	NC	IO58NPB3V0	IO58NPB4V0	IO85NPB4V0
M6	NC	NC	AV0	AV0
M7	NC	NC	AC1	AC1
M8	AG1	AG1	AG3	AG3
M9	AC2	AC2	AC4	AC4
M10	AC4	AC4	AC6	AC6
M11	NC	AG5	AG7	AG7
M12	VPUMP	VPUMP	VPUMP	VPUMP
M13	VCCIB1	VCCIB1	VCCIB2	VCCIB2
M14	TMS	TMS	TMS	TMS

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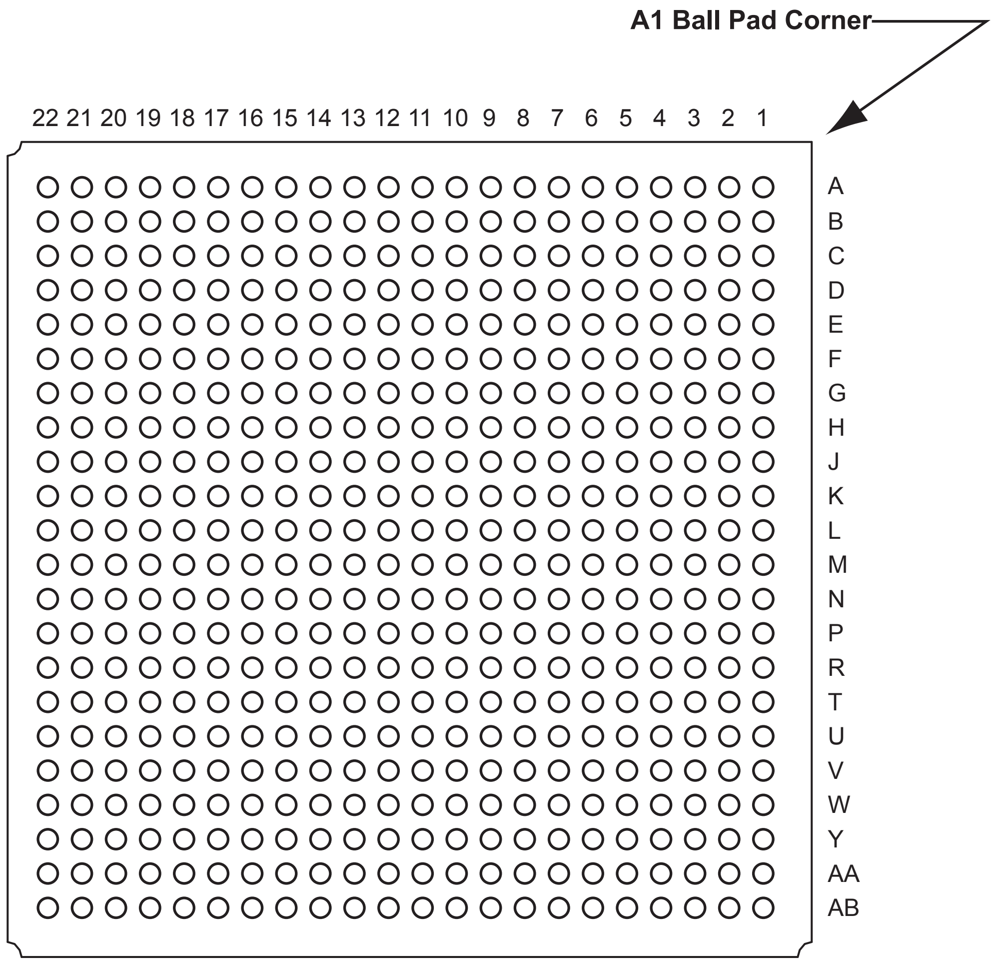

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.

Revision	Changes	Page
Advance v0.3 (continued)	The "Temperature Monitor" section was updated.	2-96
	EQ 2 is new.	2-103
	The "ADC Description" section was updated.	2-102
	Figure 2-16 • Fusion Clocking Options was updated.	2-20
	Table 2-46 · Analog Channel Specifications was updated.	2-118
	The notes in Table 2-72 • Fusion Standard and Advanced I/O – Hot-Swap and 5 V Input Tolerance Capabilities were updated.	2-144
	The "Simultaneously Switching Outputs and PCB Layout" section is new.	2-149
	LVPECL and LVDS were updated in Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications.	2-157
	LVPECL and LVDS were updated in Table 2-82 • Fusion Pro I/O Attributes vs. I/O Standard Applications.	2-158
	The "Timing Model" was updated.	2-161
	All voltage-referenced Minimum and Maximum DC Input and Output Level tables were updated.	N/A
	All Timing Characteristic tables were updated	N/A
	Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated.	2-165
	Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated.	2-134
	Table 2-93 • I/O Output Buffer Maximum Resistances [1] was updated.	2-171
	The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet.	2-211
	The "CoreMP7 and Cortex-M1 Software Tools" section is new.	2-257
	Table 2-83 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions was updated.	2-165
	Table 2-79 • Summary of I/O Timing Characteristics – Software Default Settings was updated.	2-134
	Table 2-93 • I/O Output Buffer Maximum Resistances [1] was updated.	2-171
	The "BLVDS/M-LVDS" section is new. BLVDS and M-LVDS are two new I/O standards included in the datasheet.	2-211
	The "108-Pin QFN" table for the AFS090 device is new.	3-2
	The "180-Pin QFN" table for the AFS090 device is new.	3-4
	The "208-Pin PQFP" table for the AFS090 device is new.	3-8
	The "256-Pin FBGA" table for the AFS090 device is new.	3-12
	The "256-Pin FBGA" table for the AFS250 device is new.	3-12