Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	27648
Number of I/O	60
Number of Gates	90000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	180-WFQFN Dual Rows, Exposed Pad
Supplier Device Package	180-QFN (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/afs090-2qng180i

Product Ordering Codes

M1AFS600 – 1 FG G 256 Y I

I — Application (junction temperature range)
- Blank = Commercial (0 to +85°C)
- I = Industrial (–40 to +100°C)
- PP = Pre-Production
- ES = Engineering Silicon (room temperature only)

Y — Security Feature
- Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
- Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

256 — Package Lead Count

G — Lead-Free Packaging Options
- Blank = Standard Packaging
- G = RoHS-Compliant (green) Packaging

FG — Package Type
- QN = Quad Flat No Lead (0.5 mm pitch)[1]
- PQ = Plastic Quad Flat Pack (0.5 mm pitch)
- FG = Fine Pitch Ball Grid Array (1.0 mm pitch)[2]

1 — Speed Grade
- Blank = Standard
- 1 = 15% Faster than Standard
- 2 = 25% Faster than Standard

M1AFS600 — Part Number

Fusion Devices
- AFS090 = 90,000 System Gates
- AFS250 = 250,000 System Gates
- AFS600 = 600,000 System Gates
- AFS1500 = 1,500,000 System Gates

ARM-Enabled Fusion Devices
- M1AFS250 = 250,000 System Gates
- M1AFS600 = 600,000 System Gates
- M1AFS1500 = 1,500,000 System Gates

Pigeon Point Devices
- P1AFS600 = 600,000 System Gates
- P1AFS1500 = 1,500,000 System Gates

MicroBlade Devices
- U1AFS250 = 250,000 System Gates
- U1AFS600 = 600,000 System Gates
- U1AFS1500 = 1,500,000 System Gates

Notes:
1. *For Fusion devices, Quad Flat No Lead packages are only offered as RoHS compliant, QNG packages.*
2. *MicroBlade and Pigeon Point devices only support FG packages.*

Fusion Device Status

Fusion	Status	Cortex-M1	Status	Pigeon Point	Status	MicroBlade	Status
AFS090	Production						
AFS250	Production	M1AFS250	Production			U1AFS250	Production
AFS600	Production	M1AFS600	Production	P1AFS600	Production	U1AFS600	Production
AFS1500	Production	M1AFS1500	Production	P1AFS1500	Production	U1AFS1500	Production

Global Resource Characteristics

AFS600 VersaNet Topology

Clock delays are device-specific. Figure 2-15 is an example of a global tree used for clock routing. The global tree presented in Figure 2-15 is driven by a CCC located on the west side of the AFS600 device. It is used to drive all D-flip-flops in the device.

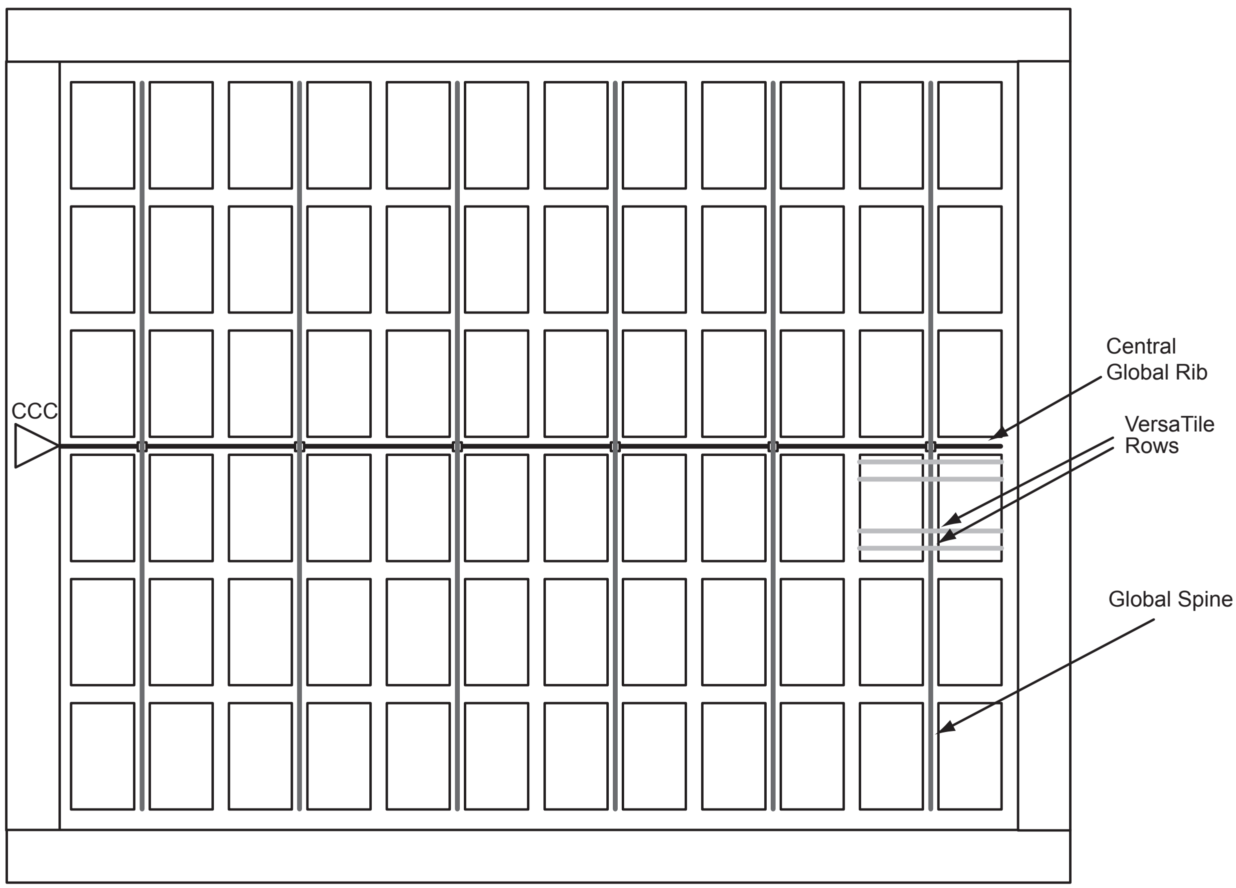


Figure 2-15 • **Example of Global Tree Use in an AFS600 Device for Clock Routing**

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS macros are composite macros that include an I/O macro driving a global buffer, hardwired together (Figure 2-20).

The CLKINT macro provides a global buffer function driven by the FPGA core.

The CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by Fusion devices. The available CLKBUF macros are described in the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide*.

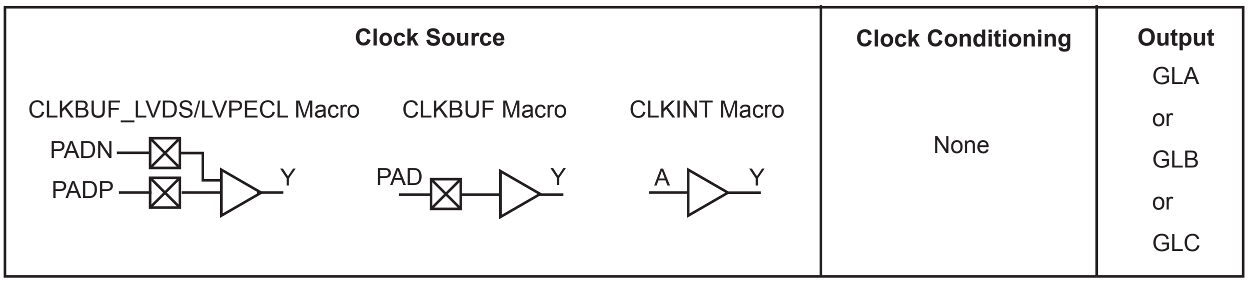


***Figure 2-20* • Global Buffers with No Programmable Delay**

Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-21 on page 2-25). The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the Fusion family. The available INBUF macros are described in the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide.*

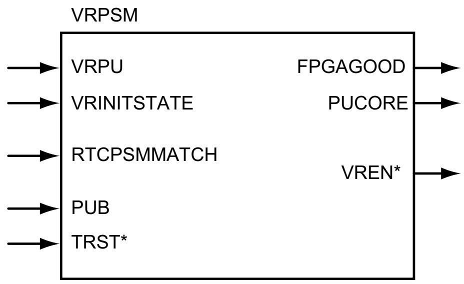
The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero SoC and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

Voltage Regulator and Power System Monitor (VRPSM)

The VRPSM macro controls the power-up state of the FPGA. The power-up bar (PUB) pin can turn on the voltage regulator when set to 0. TRST can enable the voltage regulator when deasserted, allowing the FPGA to power-up when user want access to JTAG ports. The inputs VRINITSTATE and RTCPSMMATCH come from the flash bits and RTC, and can also power up the FPGA.



Note: **Signals are hardwired internally and do not exist in the macro core.*

***Figure 2-30 •* VRPSM Macro**

***Table 2-17 •* VRPSM Signal Descriptions**

Signal Name	Width	Direction	Function
VRPU	1	In	Voltage Regulator Power-Up 0 – Voltage regulator disabled. PUB must be floated or pulled up, and the TRST pin must be grounded to disable the voltage regulator. 1 – Voltage regulator enabled
VRINITSTATE	1	In	Voltage Regulator Initial State Defines the voltage Regulator status upon power-up of the 3.3 V. The signal is configured by Libero SoC when the VRPSM macro is generated. Tie off to 1 – Voltage regulator enables when 3.3 V is powered. Tie off to 0 – Voltage regulator disables when 3.3 V is powered.
RTCPSMMATCH	1	In	RTC Power System Management Match Connect from RTCPSMATCH signal from RTC in AB 0 transition to 1 turns on the voltage regulator
PUB	1	In	External pin, built-in weak pull-up Power-Up Bar 0 – Enables voltage regulator at all times
TRST*	1	In	External pin, JTAG Test Reset 1 – Enables voltage regulator at all times
FPGAGOOD	1	Out	Indicator that the FPGA is powered and functional No need to connect if it is not used. 1 – Indicates that the FPGA is powered up and functional. 0 – Not possible to read by FPGA since it has already powered off.
PUCORE	1	Out	Power-Up Core Inverted signal of PUB. No need to connect if it is not used.
VREN*	1	Out	Voltage Regulator Enable Connected to 1.5 V voltage regulator in Fusion device internally. 0 – Voltage regulator disables 1 – Voltage regulator enables

Note: **Signals are hardwired internally and do not exist in the macro core.*

1.5 V Voltage Regulator

The 1.5 V voltage regulator uses an external pass transistor to generate 1.5 V from a 3.3 V supply. The base of the pass transistor is tied to PTBASE, the collector is tied to 3.3 V, and an emitter is tied to PTBASE and the 1.5 V supplies of the Fusion device. Figure 2-27 on page 2-31 shows the hook-up of the 1.5 V voltage regulator to an external pass transistor.

Microsemi recommends using a PN2222A or 2N2222A transistor. The gain of such a transistor is approximately 25, with a maximum base current of 20 mA. The maximum current that can be supported is 0.5 A. Transistors with different gain can also be used for different current requirements.

***Table 2-18* • Electrical Characteristics**
VCC33A = 3.3 V

Symbol	Parameter	Condition		Min	Typical	Max	Units
VOUT	Output Voltage	Tj = 25ºC		1.425	1.5	1.575	V
ICC33A	Operation Current	Tj = 25ºC	ILOAD = 1 mA ILOAD = 100 mA ILOAD = 0.5 A		11 11 30		mA mA mA
ΔVOUT	Load Regulation	Tj = 25ºC	ILOAD = 1 mA to 0.5 A		90		mV
ΔVOUT	Line Regulation	Tj = 25ºC	VCC33A = 2.97 V to 3.63 V ILOAD = 1 mA VCC33A = 2.97 V to 3.63 V ILOAD = 100 mA VCC33A = 2.97 V to 3.63 V ILOAD = 500 mA		10.6 12.1 10.6		mV/V mV/V mV/V
	Dropout Voltage*	Tj = 25ºC	ILOAD = 1 mA ILOAD = 100 mA ILOAD = 0.5 A		0.63 0.84 1.35		V V V
IPTBASE	PTBase Current	Tj = 25ºC	ILOAD = 1 mA ILOAD = 100 mA ILOAD = 0.5 A		48 736 12	 20	µA µA mA

*Note: *Data collected with 2N2222A.*

Access to the FB is controlled by the BUSY signal. The BUSY output is synchronous to the CLK signal. FB operations are only accepted in cycles where BUSY is logic 0.

Write Operation

Write operations are initiated with the assertion of the WEN signal. Figure 2-35 on page 2-45 illustrates the multiple Write operations.

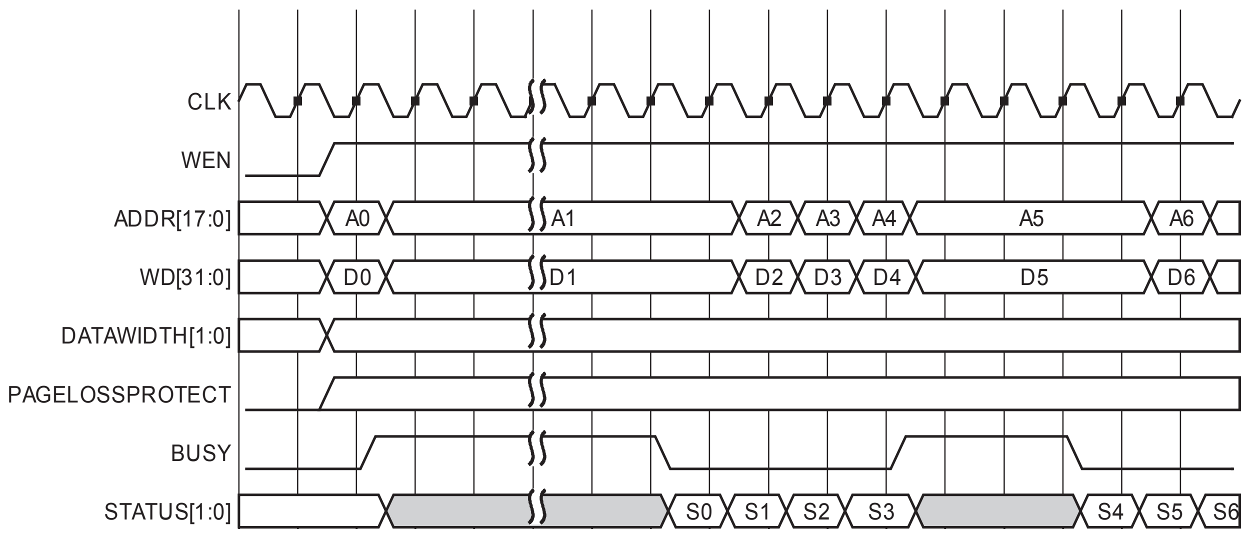


***Figure 2-35* • FB Write Waveform**

When a Write operation is initiated to a page that is currently not in the Page Buffer, the FB control logic will issue a BUSY signal to the user interface while the page is loaded from the FB Array into the Page Buffer. A Copy Page operation takes no less than 55 cycles and could take more if a Write or Unprotect Page operation is started while the NVM is busy pre-fetching a block. The basic operation is to read a block from the array into the block register (5 cycles) and then write the block register to the page buffer (1 cycle) and if necessary, when the copy is complete, reading the block being written from the page buffer into the block buffer (1 cycle). A page contains 9 blocks, so 9 blocks multiplied by 6 cycles to read/write each block, plus 1 is 55 cycles total. Subsequent writes to the same block of the page will incur no busy cycles. A write to another block in the page will assert BUSY for four cycles (five cycles when PIPE is asserted), to allow the data to be written to the Page Buffer and have the current block loaded into the Block Buffer.

Write operations are considered successful as long as the STATUS output is '00'. A non-zero STATUS indicates that an error was detected during the operation and the write was not performed. Note that the STATUS output is "sticky"; it is unchanged until another operation is started.

Only one word can be written at a time. Write word width is controlled by the DATAWIDTH bus. Users are responsible for keeping track of the contents of the Page Buffer and when to program it to the array. Just like a regular RAM, writing to random addresses is possible. Users can write into the Page Buffer in any order but will incur additional BUSY cycles. It is not necessary to modify the entire Page Buffer before saving it to nonvolatile memory.

Write errors include the following:

1. Attempting to write a page that is Overwrite Protected (STATUS = '01'). The write is not performed.
2. Attempting to write to a page that is not in the Page Buffer when Page Loss Protection is enabled (STATUS = '11'). The write is not performed.

RAM512X18 Description

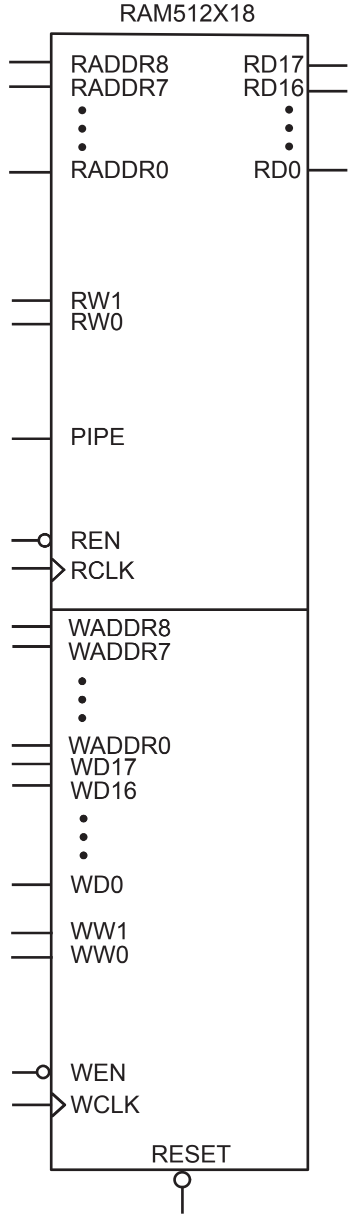


Figure 2-49 • **RAM512X18**

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

Current Monitor

The Fusion Analog Quad is an excellent element for voltage- and current-monitoring applications. In addition to supporting the same functionality offered by the AV pad, the AC pad can be configured to monitor current across an external sense resistor (Figure 2-70). To support this current monitor function, a differential amplifier with 10x gain passes the amplified voltage drop between the AV and AC pads to the ADC. The amplifier enables the user to use very small resistor values, thereby limiting any impact on the circuit. This function of the AC pad does not limit AV pad operation. The AV pad can still be configured for use as a direct voltage input or scaled through the AV prescaler independently of it's use as an input to the AC pad's differential amplifier.

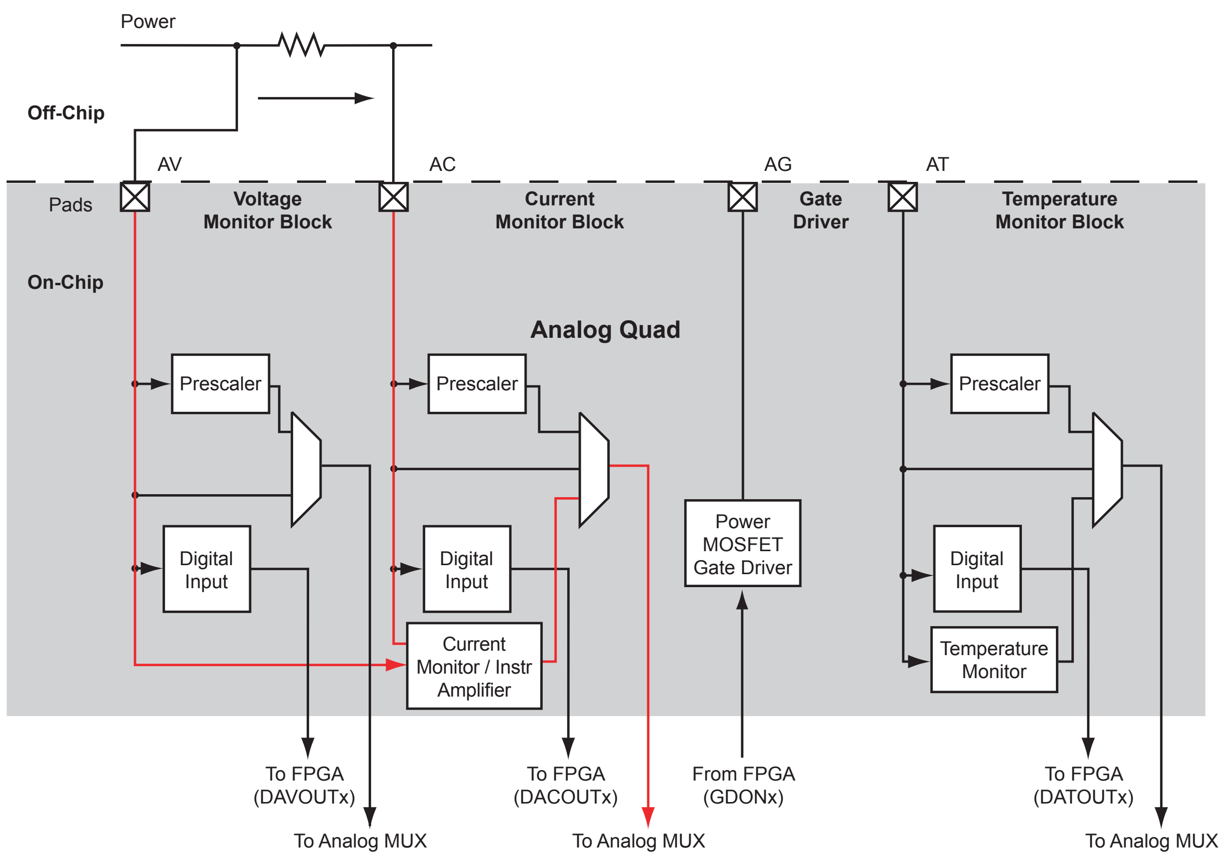


Figure 2-70 • **Analog Quad Current Monitor Configuration**

The diode's voltage is measured at each current level and the temperature is calculated based on EQ 7.

$$V_{TMSLO} - V_{TMSHI} = n\frac{kT}{q}\left(\ln\frac{I_{TMSLO}}{I_{TMSHI}}\right)$$

EQ 7

where

I_{TMSLO} is the current when the Temperature Strobe is Low, typically 100 µA

I_{TMSHI} is the current when the Temperature Strobe is High, typically 10 µA

V_{TMSLO} is diode voltage while Temperature Strobe is Low

V_{TMSHI} is diode voltage while Temperature Strobe is High

n is the non-ideality factor of the diode-connected transistor. It is typically 1.004 for the Microsemi-recommended transistor type 2N3904.

$K = 1.3806 \times 10^{-23}$ J/K is the Boltzman constant

$Q = 1.602 \times 10^{-19}$ C is the charge of a proton

When $I_{TMSLO} / I_{TMSHI} = 10$, the equation can be simplified as shown in EQ 8.

$$\Delta V = V_{TMSLO} - V_{TMSHI} = 1.986 \times 10^{-4} nT$$

EQ 8

In the Fusion TMB, the ideality factor *n* for 2N3904 is 1.004 and ΔV is amplified 12.5 times by an internal amplifier; hence the voltage before entering the ADC is as given in EQ 9.

$$V_{ADC} = \Delta V \times 12.5 = 2.5\ \text{mV} / (K \times T)$$

EQ 9

This means the temperature to voltage relationship is 2.5 mV per degree Kelvin. The unique design of Fusion has made the Temperature Monitor System simple for the user. When the 10-bit mode ADC is used, each LSB represents 1 degree Kelvin, as shown in EQ 10. That is, e. 25°C is equal to 293°K and is represented by decimal 293 counts from the ADC.

$$1K = 2.5\ \text{mV} \times \frac{2^{10}}{2.56\ \text{V}} = 1\ \text{LSB}$$

EQ 10

If 8-bit mode is used for the ADC resolution, each LSB represents 4 degrees Kelvin; however, the resolution remains as 1 degree Kelvin per LSB, even for 12-bit mode, due to the Temperature Monitor design. An example of the temperature data format for 10-bit mode is shown in Table 2-38.

***Table 2-38* • Temperature Data Format**

Temperature	Temperature (K)	Digital Output (ADC 10-bit mode)
–40°C	233	00 1110 1001
–20°C	253	00 1111 1101
0°C	273	01 0001 0001
1°C	274	01 0001 0010
10 °C	283	01 0001 1011
25°C	298	01 0010 1010
50 °C	323	01 0100 0011
85 °C	358	01 0110 0110

ADC Input Multiplexer

At the input to the Fusion ADC is a 32:1 multiplexer. Of the 32 input channels, up to 30 are user definable. Two of these channels are hardwired internally. Channel 31 connects to an internal temperature diode so the temperature of the Fusion device itself can be monitored. Channel 0 is wired to the FPGA's 1.5 V VCC supply, enabling the Fusion device to monitor its own power supply. Doing this internally makes it unnecessary to use an analog I/O to support these functions. The balance of the MUX inputs are connected to Analog Quads (see the "Analog Quad" section on page 2-80). Table 2-40 defines which Analog Quad inputs are associated with which specific analog MUX channels. The number of Analog Quads present is device-dependent; refer to the family list in the "Fusion Family" table on page I of this datasheet for the number of quads per device. Regardless of the number of quads populated in a device, the internal connections to both VCC and the internal temperature diode remain on Channels 0 and 31, respectively. To sample the internal temperature monitor, it must be strobed (similar to the AT pads). The TMSTBINT pin on the Analog Block macro is the control for strobing the internal temperature measurement diode.

To determine which channel is selected for conversion, there is a five-pin interface on the Analog Block, CHNUMBER[4:0], defined in Table 2-39.

***Table 2-39* • Channel Selection**

Channel Number	CHNUMBER[4:0]
0	00000
1	00001
2	00010
3	00011
. . .	. . .
30	11110
31	11111

Table 2-40 shows the correlation between the analog MUX input channels and the analog input pins.

***Table 2-40* • Analog MUX Channels**

Analog MUX Channel	Signal	Analog Quad Number
0	Vcc_analog	
1	AV0	Analog Quad 0
2	AC0	
3	AT0	
4	AV1	Analog Quad 1
5	AC1	
6	AT1	
7	AV2	Analog Quad 2
8	AC2	
9	AT2	
10	AV3	Analog Quad 3
11	AC3	
12	AT3	
13	AV4	Analog Quad 4
14	AC4	
15	AT4	

Table 2-53 • Analog Channel Accuracy: Monitoring Standard Positive Voltages
Typical Conditions, T_A = 25°C

Input Voltage (V)	Calibrated Typical Error per Positive Prescaler Setting [1] (%FSR)							Direct ADC [2,3] (%FSR)
	16 V (AT)	16 V (12 V) (AV/AC)	8 V (AV/AC)	4 V (AT)	4 V (AV/AC)	2 V (AV/AC)	1 V (AV/AC)	VAREF = 2.56 V
15	1							
14	1							
12	1	1						
5	2	2	1					
3.3	2	2	1	1	1			
2.5	3	2	1	1	1			1
1.8	4	4	1	1	1	1		1
1.5	5	5	2	2	2	1		1
1.2	7	6	2	2	2	1		1
0.9	9	9	4	3	3	1	1	1

Notes:

1. *Requires enabling Analog Calibration using SmartGen Analog System Builder. For further details, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the Fusion FPGA Fabric User Guide.*
2. *Direct ADC mode using an external VAREF of 2.56V±4.6mV, without Analog Calibration macro.*
3. *For input greater than 2.56 V, the ADC output will saturate. A higher VAREF or prescaler usage is recommended.*

Examples

Calculating Accuracy for an Uncalibrated Analog Channel

Formula

For a given prescaler range, EQ 30 gives the output voltage.

Output Voltage = (Channel Output Offset in V) + (Input Voltage x Channel Gain)

EQ 30

where

Channel Output offset in V = Channel Input offset in LSBs x Equivalent voltage per LSB

Channel Gain Factor = 1+ (% Channel Gain / 100)

Example

Input Voltage = 5 V

Chosen Prescaler range = 8 V range

Refer to Table 2-51 on page 2-122.

Max. Output Voltage = (Max Positive input offset) + (Input Voltage x Max Positive Channel Gain)

Max. Positive input offset = (21 LSB) x (8 mV per LSB in 10-bit mode)

Max. Positive input offset = 166 mV

Max. Positive Gain Error = +3%

Max. Positive Channel Gain = 1 + (+3% / 100)

Max. Positive Channel Gain = 1.03

Max. Output Voltage = (166 mV) + (5 V x 1.03)

Max. Output Voltage = **5.316 V**

***Table 2-68* • I/O Bank Support by Device**

I/O Bank	AFS090	AFS250	AFS600	AFS1500
Standard I/O	N	N	–	–
Advanced I/O	E, W	E, W	E, W	E, W
Pro I/O	–	–	N	N
Analog Quad	S	S	S	S

Note: E = East side of the device
W = West side of the device
N = North side of the device
S = South side of the device

***Table 2-69* • Fusion VCCI Voltages and Compatible Standards**

VCCI (typical)	Compatible Standards
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II),* GTL+ 3.3, GTL 3.3,* LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II),* GTL+ 2.5,* GTL 2.5,* LVDS, BLVDS, M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I),* HSTL (Class II)*

*Note: *I/O standard supported by Pro I/O banks.*

Table 2-70* • Fusion VREF Voltages and Compatible Standards

VREF (typical)	Compatible Standards
1.5 V	SSTL3 (Class I and II)
1.25 V	SSTL2 (Class I and II)
1.0 V	GTL+ 2.5, GTL+ 3.3
0.8 V	GTL 2.5, GTL 3.3
0.75 V	HSTL (Class I), HSTL (Class II)

*Note: *I/O standards supported by Pro I/O banks.*

Table 2-77 • **Comparison Table for 5 V–Compliant Receiver Scheme**

Scheme	Board Components	Speed	Current Limitations
1	Two resistors	Low to high[1]	Limited by transmitter's drive strength
2	Resistor and Zener 3.3 V	Medium	Limited by transmitter's drive strength
3	Bus switch	High	N/A
4	Minimum resistor value[2] R = 47 Ω at T_J = 70°C R = 150 Ω at T_J = 85°C R = 420 Ω at T_J = 100°C	Medium	Maximum diode current at 100% duty cycle, signal constantly at '1' 52.7 mA at T_J =70°C / 10-year lifetime 16.5 mA at T_J = 85°C / 10-year lifetime 5.9 mA at T_J = 100°C / 10-year lifetime For duty cycles other than 100%, the currents can be increased by a factor = 1 / (duty cycle). Example: 20% duty cycle at 70°C Maximum current = (1 / 0.2) * 52.7 mA = 5 * 52.7 mA = 263.5 mA

Notes:

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long-term reliability.*

Table 3-2 • **Recommended Operating Conditions**[1]

Symbol	Parameter[2]		Commercial	Industrial	Units
T_J	Junction temperature		0 to +85	–40 to +100	°C
VCC	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming mode[3]	3.15 to 3.45	3.15 to 3.45	V
		Operation[4]	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V
VCC33A	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VCC33PMP	+3.3 V power supply		2.97 to 3.63	2.97 to 3.63	V
VAREF	Voltage reference for ADC		2.527 to 2.593	2.527 to 2.593	V
VCC15A [5]	Digital power supply for the analog system		1.425 to 1.575	1.425 to 1.575	V
VCCNVM	Embedded flash power supply		1.425 to 1.575	1.425 to 1.575	V
VCCOSC	Oscillator power supply		2.97 to 3.63	2.97 to 3.63	V
AV, AC [6]	Unpowered, ADC reset asserted or unconfigured		–10.5 to 12.0	–10.5 to 11.6	V
	Analog input (+16 V to +2 V prescaler range)		–0.3 to 12.0	–0.3 to 11.6	V
	Analog input (+1 V to + 0.125 V prescaler range)		–0.3 to 3.6	–0.3 to 3.6	V
	Analog input (–16 V to –2 V prescaler range)		–10.5 to 0.3	–10.5 to 0.3	V
	Analog input (–1 V to –0.125 V prescaler range)		–3.6 to 0.3	–3.6 to 0.3	V
	Analog input (direct input to ADC)		–0.3 to 3.6	–0.3 to 3.6	V
	Digital input		–0.3 to 12.0	–0.3 to 11.6	V
AG [6]	Unpowered, ADC reset asserted or unconfigured		–10.5 to 12.0	–10.5 to 11.6	V
	Low Current Mode (1 µA, 3 µA, 10 µA, 30 µA)		–0.3 to 12.0	–0.3 to 11.6	V
	Low Current Mode (–1 µA, –3 µA, –10 µA, –30 µA)		–10.5 to 0.3	–10.5 to 0.3	V
	High Current Mode [7]		–10.5 to 12.0	–10.5 to 11.6	V
AT [6]	Unpowered, ADC reset asserted or unconfigured		–0.3 to 15.5	–0.3 to 14.5	V
	Analog input (+16 V, +4 V prescaler range)		–0.3 to 15.5	–0.3 to 14.5	V
	Analog input (direct input to ADC)		–0.3 to 3.6	–0.3 to 3.6	V
	Digital input		–0.3 to 15.5	–0.3 to 14.5	V

Notes:

1. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-85 on page 2-157.*
2. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
3. *The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.*
4. *VPUMP can be left floating during normal operation (not programming mode).*
5. *Violating the V_{CC15A} recommended voltage supply during an embedded flash program cycle can corrupt the page being programmed.*
6. *The input voltage may overshoot by up to 500 mV above the Recommended Maximum (150 mV in Direct mode), provided the duration of the overshoot is less than 50% of the operating lifetime of the device.*
7. *The AG pad should also conform to the limits as specified in Table 2-48 on page 2-114.*

Table 3-9 • **AFS600 Quiescent Supply Current Characteristics**

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
ICC[1]	1.5 V quiescent current	Operational standby[4], VCC = 1.575 V	T_J = 25°C		13	25	mA
			T_J = 85°C		20	45	mA
			T_J=100°C		25	75	mA
		Standby mode[5] or Sleep mode[6], VCC = 0 V			0	0	µA
ICC33[2]	3.3 V analog supplies current	Operational standby[4], VCC33 = 3.63 V	T_J = 25°C		9.8	13	mA
			T_J = 85°C		10.7	14	mA
			T_J = 100°C		10.8	15	mA
		Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V	T_J = 25°C		0.31	2	mA
			T_J = 85°C		0.35	2	mA
			T_J = 100°C		0.45	2	mA
		Standby mode[5], VCC33 = 3.63 V	T_J = 25°C		2.8	3.6	mA
			T_J = 85°C		2.9	4	mA
			T_J = 100°C		3.5	6	mA
		Sleep mode[6], V_{CC33} = 3.63 V	T_J = 25°C		17	19	µA
			T_J = 85°C		18	20	µA
			T_J = 100°C		24	25	µA
ICCI[3]	I/O quiescent current	Operational standby[4], VCCIx = 3.63 V	T_J = 25°C		417	648	µA
			T_J = 85°C		417	648	µA
			T_J = 100°C		417	649	µA
IJTAG	JTAG I/O quiescent current	Operational standby[4], VJTAG = 3.63 V	T_J = 25°C		80	100	µA
			T_J = 85°C		80	100	µA
			T_J = 100°C		80	100	µA
		Standby mode[5] or Sleep mode[6], VJTAG = 0 V			0	0	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

PQ208		
Pin Number	AFS250 Function	AFS600 Function
74	AV2	AV4
75	AC2	AC4
76	AG2	AG4
77	AT2	AT4
78	ATRTN1	ATRTN2
79	AT3	AT5
80	AG3	AG5
81	AC3	AC5
82	AV3	AV5
83	AV4	AV6
84	AC4	AC6
85	AG4	AG6
86	AT4	AT6
87	ATRTN2	ATRTN3
88	AT5	AT7
89	AG5	AG7
90	AC5	AC7
91	AV5	AV7
92	NC	AV8
93	NC	AC8
94	NC	AG8
95	NC	AT8
96	NC	ATRTN4
97	NC	AT9
98	NC	AG9
99	NC	AC9
100	NC	AV9
101	GNDAQ	GNDAQ
102	VCC33A	VCC33A
103	ADCGNDREF	ADCGNDREF
104	VAREF	VAREF
105	PUB	PUB
106	VCC33A	VCC33A
107	GNDA	GNDA
108	PTEM	PTEM
109	PTBASE	PTBASE
110	GNDNVM	GNDNVM

PQ208		
Pin Number	AFS250 Function	AFS600 Function
111	VCCNVM	VCCNVM
112	VCC	VCC
112	VCC	VCC
113	VPUMP	VPUMP
114	GNDQ	NC
115	VCCIB1	TCK
116	TCK	TDI
117	TDI	TMS
118	TMS	TDO
119	TDO	TRST
120	TRST	VJTAG
121	VJTAG	IO57NDB2V0
122	IO57NDB1V0	GDC2/IO57PDB2V0
123	GDC2/IO57PDB1V0	IO56NDB2V0
124	IO56NDB1V0	GDB2/IO56PDB2V0
125	GDB2/IO56PDB1V0	IO55NDB2V0
126	VCCIB1	GDA2/IO55PDB2V0
127	GND	GDA0/IO54NDB2V0
128	IO55NDB1V0	GDA1/IO54PDB2V0
129	GDA2/IO55PDB1V0	VCCIB2
130	GDA0/IO54NDB1V0	GND
131	GDA1/IO54PDB1V0	VCC
132	GDB0/IO53NDB1V0	GCA0/IO45NDB2V0
133	GDB1/IO53PDB1V0	GCA1/IO45PDB2V0
134	GDC0/IO52NDB1V0	GCB0/IO44NDB2V0
135	GDC1/IO52PDB1V0	GCB1/IO44PDB2V0
136	IO51NSB1V0	GCC0/IO43NDB2V0
137	VCCIB1	GCC1/IO43PDB2V0
138	GND	IO42NDB2V0
139	VCC	IO42PDB2V0
140	IO50NDB1V0	IO41NDB2V0
141	IO50PDB1V0	GCC2/IO41PDB2V0
142	GCA0/IO49NDB1V0	VCCIB2
143	GCA1/IO49PDB1V0	GND
144	GCB0/IO48NDB1V0	VCC
145	GCB1/IO48PDB1V0	IO40NDB2V0
146	GCC0/IO47NDB1V0	GCB2/IO40PDB2V0

FG256				
Pin Number	**AFS090 Function**	**AFS250 Function**	**AFS600 Function**	**AFS1500 Function**
R5	AV0	AV0	AV2	AV2
R6	AT0	AT0	AT2	AT2
R7	AV1	AV1	AV3	AV3
R8	AT3	AT3	AT5	AT5
R9	AV4	AV4	AV6	AV6
R10	NC	AT5	AT7	AT7
R11	NC	AV5	AV7	AV7
R12	NC	NC	AT9	AT9
R13	NC	NC	AG9	AG9
R14	NC	NC	AC9	AC9
R15	PUB	PUB	PUB	PUB
R16	VCCIB1	VCCIB1	VCCIB2	VCCIB2
T1	GND	GND	GND	GND
T2	NCAP	NCAP	NCAP	NCAP
T3	VCC33N	VCC33N	VCC33N	VCC33N
T4	NC	NC	ATRTN0	ATRTN0
T5	AT1	AT1	AT3	AT3
T6	ATRTN0	ATRTN0	ATRTN1	ATRTN1
T7	AT2	AT2	AT4	AT4
T8	ATRTN1	ATRTN1	ATRTN2	ATRTN2
T9	AT4	AT4	AT6	AT6
T10	ATRTN2	ATRTN2	ATRTN3	ATRTN3
T11	NC	NC	AT8	AT8
T12	NC	NC	ATRTN4	ATRTN4
T13	GNDA	GNDA	GNDA	GNDA
T14	VCC33A	VCC33A	VCC33A	VCC33A
T15	VAREF	VAREF	VAREF	VAREF
T16	GND	GND	GND	GND

FG484		
Pin Number	AFS600 Function	AFS1500 Function
P21	IO51PDB2V0	IO73PDB2V0
P22	IO49NDB2V0	IO71NDB2V0
R1	IO69PDB4V0	IO102PDB4V0
R2	IO69NDB4V0	IO102NDB4V0
R3	VCCIB4	VCCIB4
R4	IO64PDB4V0	IO91PDB4V0
R5	IO64NDB4V0	IO91NDB4V0
R6	NC	IO92PDB4V0
R7	GND	GND
R8	GND	GND
R9	VCC33A	VCC33A
R10	GNDA	GNDA
R11	VCC33A	VCC33A
R12	GNDA	GNDA
R13	VCC33A	VCC33A
R14	GNDA	GNDA
R15	VCC	VCC
R16	GND	GND
R17	NC	IO74NDB2V0
R18	GDA0/IO54NDB2V0	GDA0/IO81NDB2V0
R19	GDB0/IO53NDB2V0	GDB0/IO80NDB2V0
R20	VCCIB2	VCCIB2
R21	IO50NDB2V0	IO75NDB2V0
R22	IO50PDB2V0	IO75PDB2V0
T1	NC	IO100PPB4V0
T2	GND	GND
T3	IO66PDB4V0	IO95PDB4V0
T4	IO66NDB4V0	IO95NDB4V0
T5	VCCIB4	VCCIB4
T6	NC	IO92NDB4V0
T7	GNDNVM	GNDNVM
T8	GNDA	GNDA
T9	NC	NC
T10	AV4	AV4
T11	NC	NC

FG484		
Pin Number	AFS600 Function	AFS1500 Function
T12	AV5	AV5
T13	AC5	AC5
T14	NC	NC
T15	GNDA	GNDA
T16	NC	IO77PPB2V0
T17	NC	IO74PDB2V0
T18	VCCIB2	VCCIB2
T19	IO55NDB2V0	IO82NDB2V0
T20	GDA2/IO55PDB2V0	GDA2/IO82PDB2V0
T21	GND	GND
T22	GDC1/IO52PDB2V0	GDC1/IO79PDB2V0
U1	IO67PDB4V0	IO98PDB4V0
U2	IO67NDB4V0	IO98NDB4V0
U3	GEC1/IO63PDB4V0	GEC1/IO90PDB4V0
U4	GEC0/IO63NDB4V0	GEC0/IO90NDB4V0
U5	GND	GND
U6	VCCNVM	VCCNVM
U7	VCCIB4	VCCIB4
U8	VCC15A	VCC15A
U9	GNDA	GNDA
U10	AC4	AC4
U11	VCC33A	VCC33A
U12	GNDA	GNDA
U13	AG5	AG5
U14	GNDA	GNDA
U15	PUB	PUB
U16	VCCIB2	VCCIB2
U17	TDI	TDI
U18	GND	GND
U19	IO57NDB2V0	IO84NDB2V0
U20	GDC2/IO57PDB2V0	GDC2/IO84PDB2V0
U21	NC	IO77NPB2V0
U22	GDC0/IO52NDB2V0	GDC0/IO79NDB2V0
V1	GEB1/IO62PDB4V0	GEB1/IO89PDB4V0
V2	GEB0/IO62NDB4V0	GEB0/IO89NDB4V0

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