Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	27648
Number of I/O	60
Number of Gates	90000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	180-WFQFN Dual Rows, Exposed Pad
Supplier Device Package	180-QFN (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/afs090-qng180

Table of Contents

Fusion Device Family Overview

Device Architecture

DC and Power Characteristics

Package Pin Assignments

Datasheet Information

VersaNet Global Networks and Spine Access

The Fusion architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM, and I/O tiles on the Fusion device. There are 6 chip (main) global networks that access the entire device and 12 quadrant networks (3 in each quadrant). Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 180 internal/external clocks (in an AFS1500 device) or other high-fanout nets in Fusion devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on Fusion devices.

The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device. There are four quadrant global network regions per device (Figure 2-12 on page 2-12).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-11. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the Fusion device (the "scope" of the spine; see Figure 2-11 on page 2-11). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or another net defined by the user (Figure 2-13). Quadrant spines can be driven from user I/Os on the north and south sides of the die, via analog I/Os configured as direct digital inputs. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

Details of the chip (main) global network spine-selection MUX are presented in Figure 2-13. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device. For details on using spines in Fusion devices, see the application note *Using Global Resources in Actel Fusion Devices*.

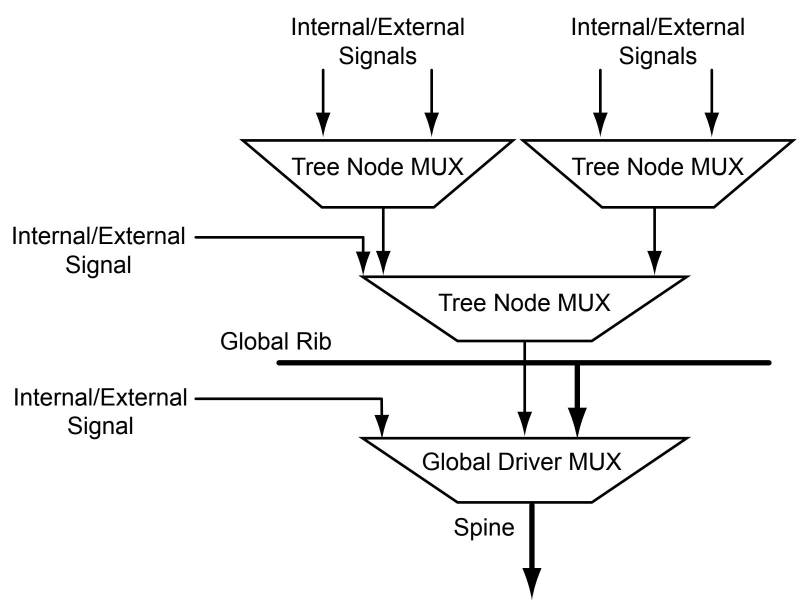
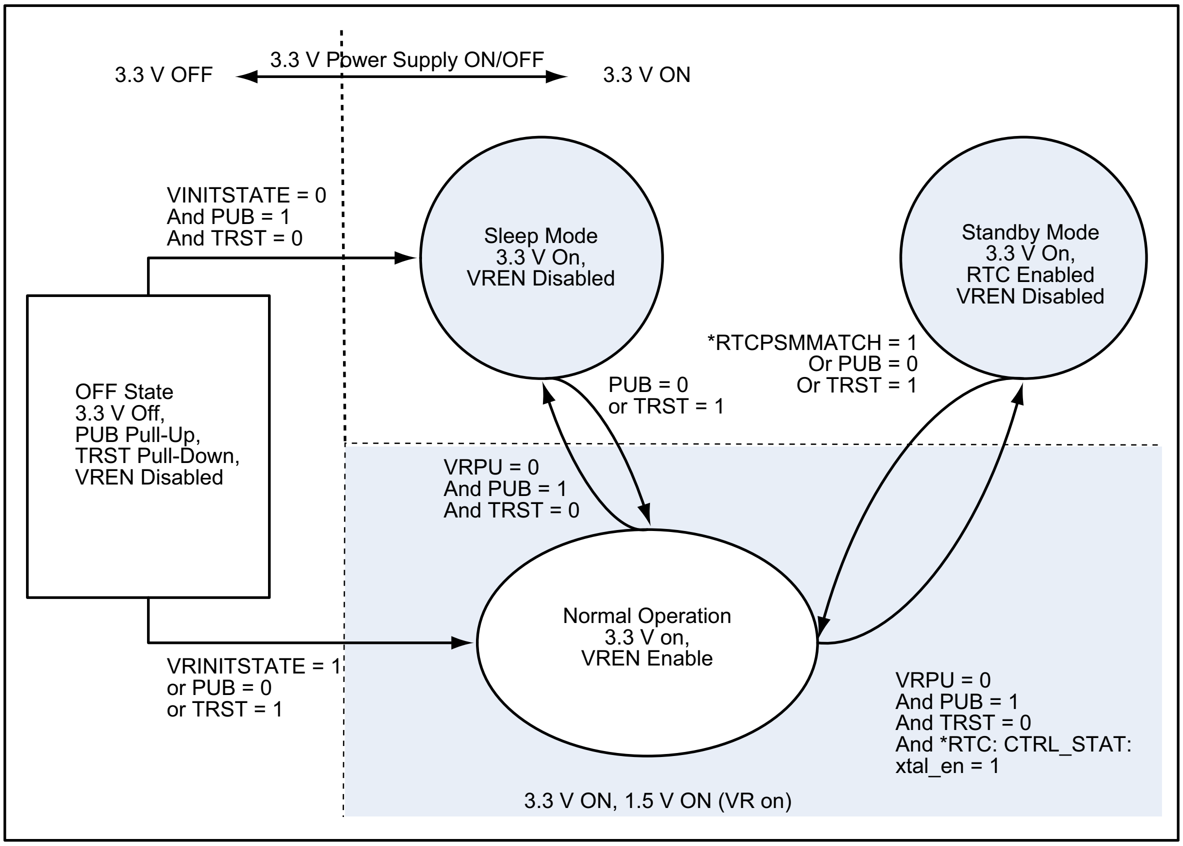


Figure 2-13 **• Spine-Selection MUX of Global Tree**



Note: ** To enter and exit standby mode without any external stimulus on PUB or TRST, the vr_en_mat in the CTRL_STAT register must also be set to 1, so that RTCPSMMATCH will assert when a match occurs; hence the device exits standby mode.*

***Figure 2-31* • State Diagram for All Different Power Modes**

When TRST is 1 or PUB is 0, the 1.5 V voltage regulator is always ON, putting the Fusion device in normal operation at all times. Therefore, when the JTAG port is not in reset, the Fusion device cannot enter sleep mode or standby mode.

To enter standby mode, the Fusion device must first power-up into normal operation. The RTC is enabled through the RTC Control/Status Register described in the "Real-Time Counter (part of AB macro)" section on page 2-33. A match value corresponding to the wake-up time is loaded into the Match Register. The 1.5 V voltage regulator is disabled by setting VRPU to 0 to allow the Fusion device to enter standby mode, when the 1.5 V supply is off but the RTC remains on.

Embedded Memories

Fusion devices include four types of embedded memory: flash block, FlashROM, SRAM, and FIFO.

Flash Memory Block

Fusion is the first FPGA that offers a flash memory block (FB). Each FB block stores 2 Mbits of data. The flash memory block macro is illustrated in Figure 2-32. The port pin name and descriptions are detailed on Table 2-19 on page 2-40. All flash memory block signals are active high, except for CLK and active low RESET. All flash memory operations are synchronous to the rising edge of CLK.

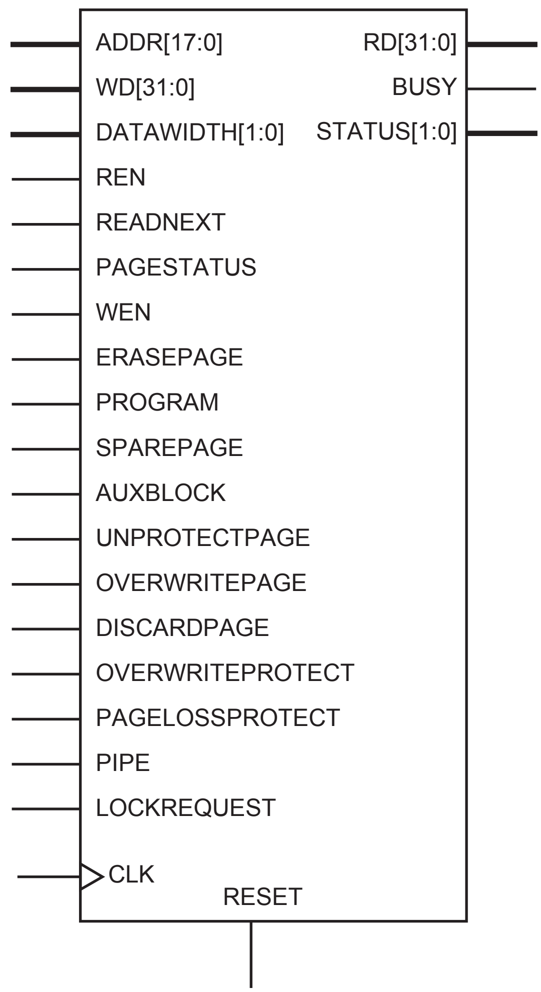


***Figure 2-32* • Flash Memory Block**

Access to the FB is controlled by the BUSY signal. The BUSY output is synchronous to the CLK signal. FB operations are only accepted in cycles where BUSY is logic 0.

Write Operation

Write operations are initiated with the assertion of the WEN signal. Figure 2-35 on page 2-45 illustrates the multiple Write operations.

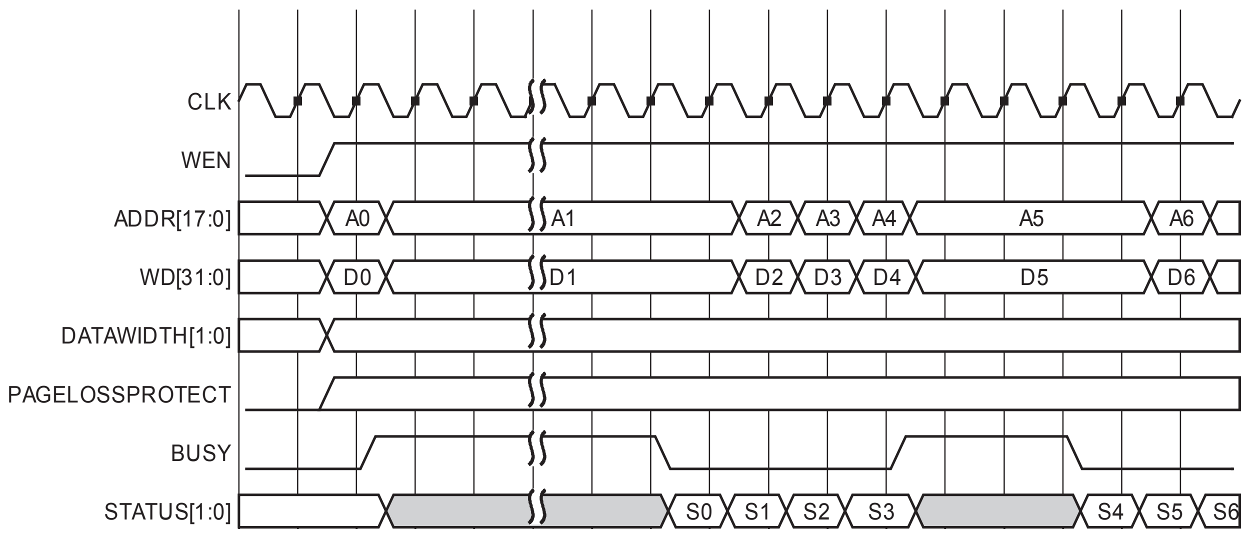


***Figure 2-35* • FB Write Waveform**

When a Write operation is initiated to a page that is currently not in the Page Buffer, the FB control logic will issue a BUSY signal to the user interface while the page is loaded from the FB Array into the Page Buffer. A Copy Page operation takes no less than 55 cycles and could take more if a Write or Unprotect Page operation is started while the NVM is busy pre-fetching a block. The basic operation is to read a block from the array into the block register (5 cycles) and then write the block register to the page buffer (1 cycle) and if necessary, when the copy is complete, reading the block being written from the page buffer into the block buffer (1 cycle). A page contains 9 blocks, so 9 blocks multiplied by 6 cycles to read/write each block, plus 1 is 55 cycles total. Subsequent writes to the same block of the page will incur no busy cycles. A write to another block in the page will assert BUSY for four cycles (five cycles when PIPE is asserted), to allow the data to be written to the Page Buffer and have the current block loaded into the Block Buffer.

Write operations are considered successful as long as the STATUS output is '00'. A non-zero STATUS indicates that an error was detected during the operation and the write was not performed. Note that the STATUS output is "sticky"; it is unchanged until another operation is started.

Only one word can be written at a time. Write word width is controlled by the DATAWIDTH bus. Users are responsible for keeping track of the contents of the Page Buffer and when to program it to the array. Just like a regular RAM, writing to random addresses is possible. Users can write into the Page Buffer in any order but will incur additional BUSY cycles. It is not necessary to modify the entire Page Buffer before saving it to nonvolatile memory.

Write errors include the following:

1. Attempting to write a page that is Overwrite Protected (STATUS = '01'). The write is not performed.
2. Attempting to write to a page that is not in the Page Buffer when Page Loss Protection is enabled (STATUS = '11'). The write is not performed.

The rate at which the gate voltage of the external MOSFET slews is determined by the current, I_g, sourced or sunk by the AG pin and the gate-to-source capacitance, C_{GS}, of the external MOSFET. As an approximation, the slew rate is given by EQ 6.

$$dv/dt = I_g / C_{GS}$$

EQ 6

C_{GS} is not a fixed capacitance but, depending on the circuitry connected to its drain terminal, can vary significantly during the course of a turn-on or turn-off transient. Thus, EQ 6 on page 2-91 can only be used for a first-order estimate of the switching speed of the external MOSFET.

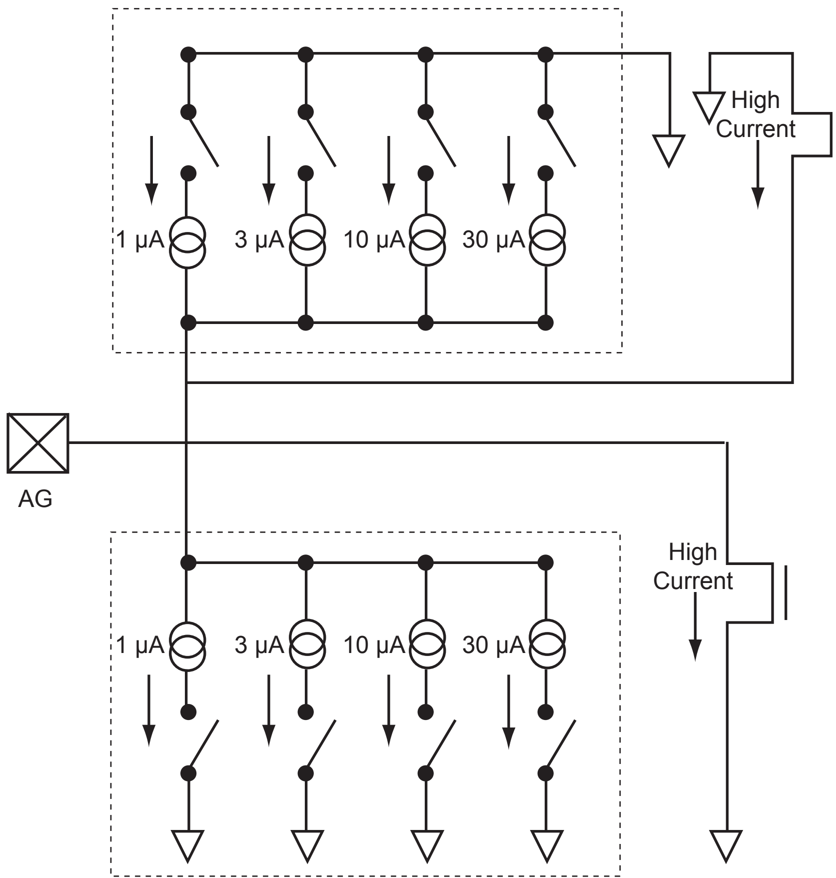


Figure 2-75 • **Gate Driver Example**

***Table 2-49* • Analog Channel Specifications (continued)**
Commercial Temperature Range Conditions, T_J = 85°C (unless noted otherwise),
Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Typ.	Max.	Units
Temperature Monitor Using Analog Pad AT						
External Temperature Monitor (external diode 2N3904, T_J = 25°C)[4]	Resolution	8-bit ADC	4			°C
		10-bit ADC	1			°C
		12-bit ADC	0.25			°C
	Systematic Offset[5]	AFS090, AFS250, AFS600, AFS1500, uncalibrated[7]	5			°C
		AFS090, AFS250, AFS600, AFS1500, calibrated[7]	±5			°C
	Accuracy			±3	±5	°C
	External Sensor Source Current	High level, TMSTBx = 0		10		µA
		Low level, TMSTBx = 1		100		µA
	Max Capacitance on AT pad				1.3	nF
Internal Temperature Monitor	Resolution	8-bit ADC	4			°C
		10-bit ADC	1			°C
		12-bit ADC	0.25			°C
	Systematic Offset[5]	AFS090[7]	5			°C
		AFS250, AFS600, AFS1500[7]	11			°C
	Accuracy			±3	±5	°C
t_{TMSHI}	Strobe High time		10		105	µs
t_{TMSLO}	Strobe Low time		5			µs
t_{TMSSET}	Settling time		5			µs

Notes:

1. *VRSM is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.*
3. *VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User Guide.

Table 2-51* • Uncalibrated Analog Channel Accuracy
Worst-Case Industrial Conditions, T_J = 85°C

		Total Channel Error (LSB)			Channel Input Offset Error (LSB)			Channel Input Offset Error (mV)			Channel Gain Error (%FSR)		
Analog Pad	**Prescaler Range (V)**	**Neg. Max.**	**Med.**	**Pos. Max.**	**Neg Max**	**Med.**	**Pos. Max.**	**Neg. Max.**	**Med.**	**Pos. Max.**	**Min.**	**Typ.**	**Max.**
Positive Range		**ADC in 10-Bit Mode**											
AV, AC	16	–22	–2	12	–11	–2	14	–169	–32	224	3	0	–3
	8	–40	–5	17	–11	–5	21	–87	–40	166	2	0	–4
	4	–45	–9	24	–16	–11	36	–63	–43	144	2	0	–4
	2	–70	–19	33	–33	–20	66	–66	–39	131	2	0	–4
	1	–25	–7	5	–11	–3	26	–11	–3	26	3	–1	–3
	0.5	–41	–12	8	–12	–7	38	–6	–4	19	3	–1	–3
	0.25	–53	–14	19	–20	–14	40	–5	–3	10	5	0	–4
	0.125	–89	–29	24	–40	–28	88	–5	–4	11	7	0	–5
AT	16	–3	9	15	–4	0	4	–64	5	64	1	0	–1
	4	–10	2	15	–11	–2	11	–44	–8	44	1	0	–1
Negative Range		**ADC in 10-Bit Mode**											
AV, AC	16	–35	–10	9	–24	–6	9	–383	–96	148	5	–1	–6
	8	–65	–19	12	–34	–12	9	–268	–99	75	5	–1	–5
	4	–86	–28	21	–64	–24	19	–254	–96	76	5	–1	–6
	2	–136	–53	37	–115	–42	39	–230	–83	78	6	–2	–7
	1	–98	–35	8	–39	–8	15	–39	–8	15	10	–3	–10
	0.5	–121	–46	7	–54	–14	18	–27	–7	9	10	–4	–11
	0.25	–149	–49	19	–72	–16	40	–18	–4	10	14	–4	–12
	0.125	–188	–67	38	–112	–27	56	–14	–3	7	16	–5	–14

*Note: *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Gain remains the same.*

Table 2-54 • ACM Address Decode Table for Analog Quad (continued)

ACMADDR [7:0] in Decimal	Name	Description	Associated Peripheral
73	MATCHREG1	Match register bits 15:8	RTC
74	MATCHREG2	Match register bits 23:16	RTC
75	MATCHREG3	Match register bits 31:24	RTC
76	MATCHREG4	Match register bits 39:32	RTC
80	MATCHBITS0	Individual match bits 7:0	RTC
81	MATCHBITS1	Individual match bits 15:8	RTC
82	MATCHBITS2	Individual match bits 23:16	RTC
83	MATCHBITS3	Individual match bits 31:24	RTC
84	MATCHBITS4	Individual match bits 39:32	RTC
88	CTRL_STAT	Control (write) / Status (read) register bits 7:0	RTC

Note: ACMADDR bytes 1 to 40 pertain to the Analog Quads; bytes 64 to 89 pertain to the RTC.

ACM Characteristics[1]

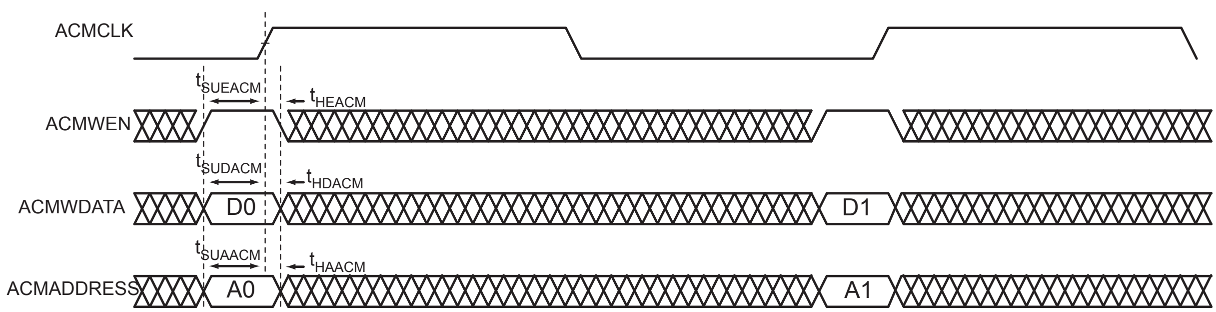


Figure 2-97 • ACM Write Waveform

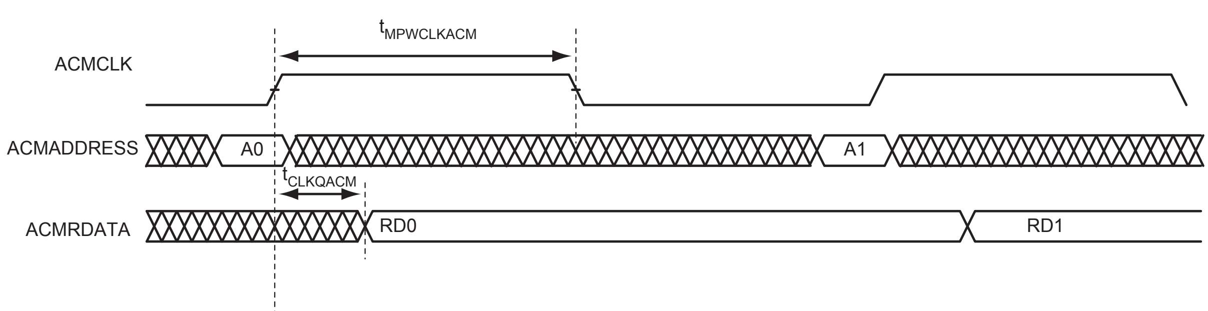


Figure 2-98 • ACM Read Waveform

1. When addressing the RTC addresses (i.e., ACMADDR 64 to 89), there is no timing generator, and the rc_osc, byte_en, and aq_wen signals have no impact.

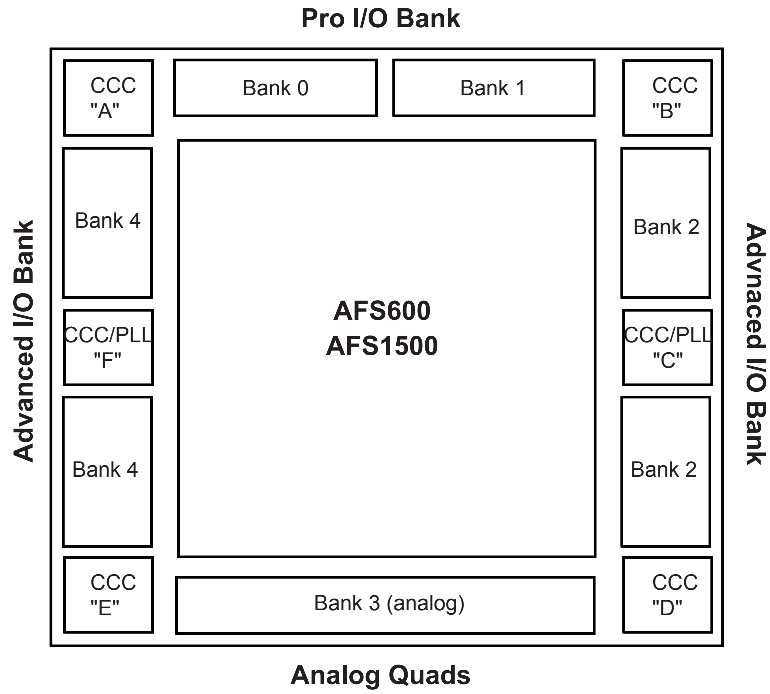


Figure 2-114 **• Naming Conventions of Fusion Devices with Four I/O Banks**

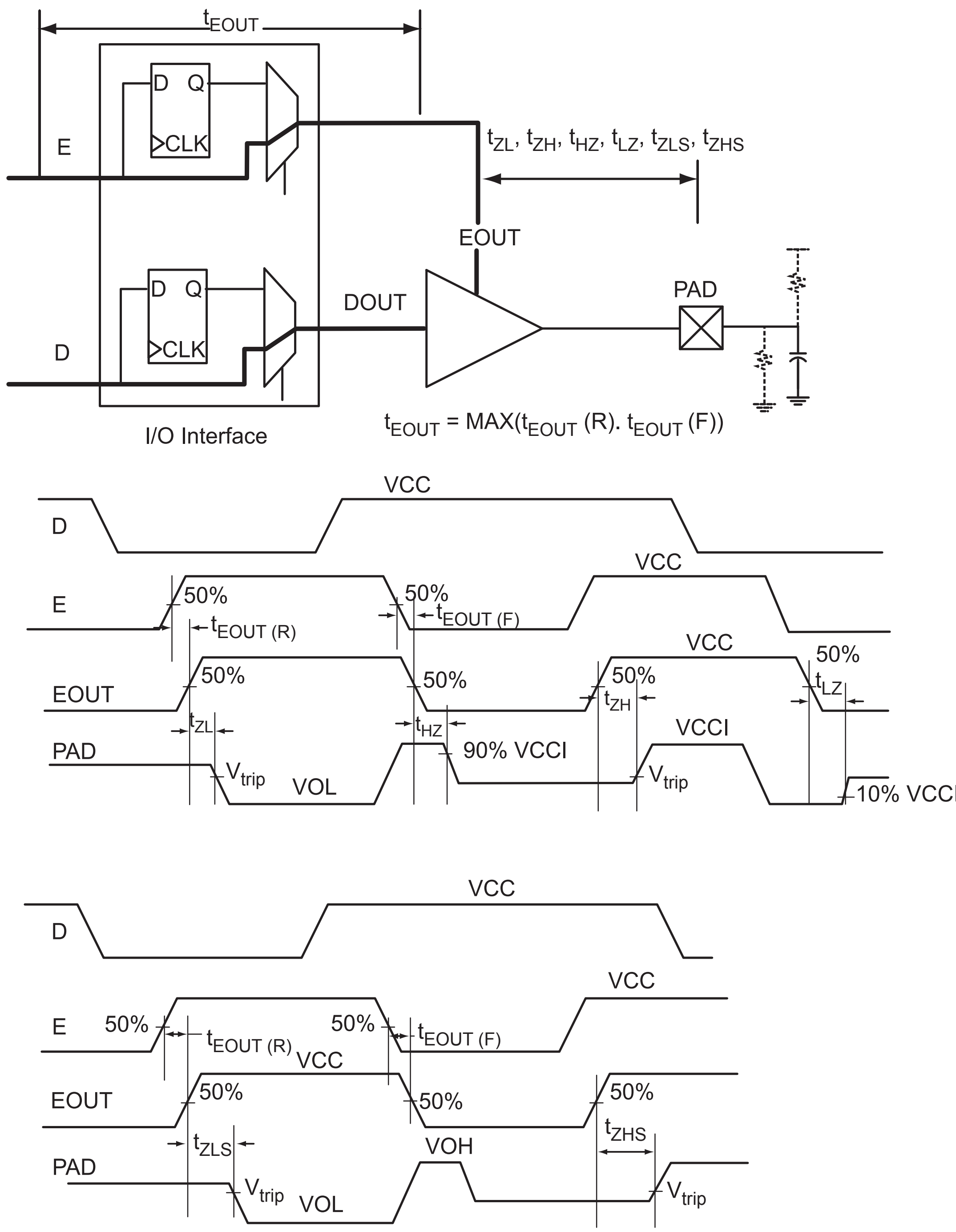


Figure 2-118 • **Tristate Output Buffer Timing Model and Delays (example)**

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-110 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	μA[4]	μA[4]
Applicable to Pro I/O Banks												
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	10	10
Applicable to Standard I/O Banks												
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

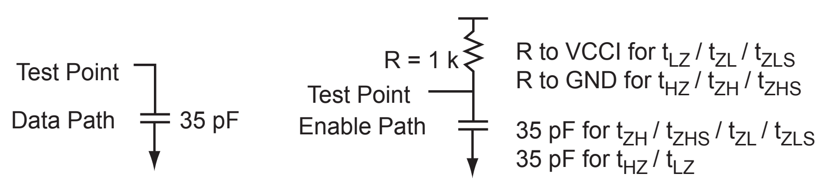


Figure 2-120 • AC Loading

Table 2-111 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

***Table 2-120* • 1.8 V LVCMOS Low Slew**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Pro I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	15.84	0.04	1.45	1.91	0.43	15.65	15.84	2.78	1.58	17.89	18.07	ns
	–1	0.56	13.47	0.04	1.23	1.62	0.36	13.31	13.47	2.37	1.35	15.22	15.37	ns
	–2	0.49	11.83	0.03	1.08	1.42	0.32	11.69	11.83	2.08	1.18	13.36	13.50	ns
4 mA	Std.	0.66	11.39	0.04	1.45	1.91	0.43	11.60	10.76	3.26	2.77	13.84	12.99	ns
	–1	0.56	9.69	0.04	1.23	1.62	0.36	9.87	9.15	2.77	2.36	11.77	11.05	ns
	–2	0.49	8.51	0.03	1.08	1.42	0.32	8.66	8.03	2.43	2.07	10.33	9.70	ns
8 mA	Std.	0.66	8.97	0.04	1.45	1.91	0.43	9.14	8.10	3.57	3.36	11.37	10.33	ns
	–1	0.56	7.63	0.04	1.23	1.62	0.36	7.77	6.89	3.04	2.86	9.67	8.79	ns
	–2	0.49	6.70	0.03	1.08	1.42	0.32	6.82	6.05	2.66	2.51	8.49	7.72	ns
12 mA	Std.	0.66	8.35	0.04	1.45	1.91	0.43	8.50	7.59	3.64	3.52	10.74	9.82	ns
	–1	0.56	7.10	0.04	1.23	1.62	0.36	7.23	6.45	3.10	3.00	9.14	8.35	ns
	–2	0.49	6.24	0.03	1.08	1.42	0.32	6.35	5.66	2.72	2.63	8.02	7.33	ns
16 mA	Std.	0.66	7.94	0.04	1.45	1.91	0.43	8.09	7.56	3.74	4.11	10.32	9.80	ns
	–1	0.56	6.75	0.04	1.23	1.62	0.36	6.88	6.43	3.18	3.49	8.78	8.33	ns
	–2	0.49	5.93	0.03	1.08	1.42	0.32	6.04	5.65	2.79	3.07	7.71	7.32	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Timing Characteristics

Table 2-136 **• 3.3 V PCI/PCI-X**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V
Applicable to Pro I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.81	0.04	1.05	1.67	0.43	2.86	2.00	3.28	3.61	5.09	4.23	ns
–1	0.56	2.39	0.04	0.89	1.42	0.36	2.43	1.70	2.79	3.07	4.33	3.60	ns
–2	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-137 **• 3.3 V PCI/PCI-X**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = 3.0 V
Applicable to Advanced I/Os

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.68	0.04	0.86	0.43	2.73	1.95	3.21	3.58	4.97	4.19	0.66	ns
–1	0.56	2.28	0.04	0.73	0.36	2.32	1.66	2.73	3.05	4.22	3.56	0.56	ns
–2	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	0.49	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

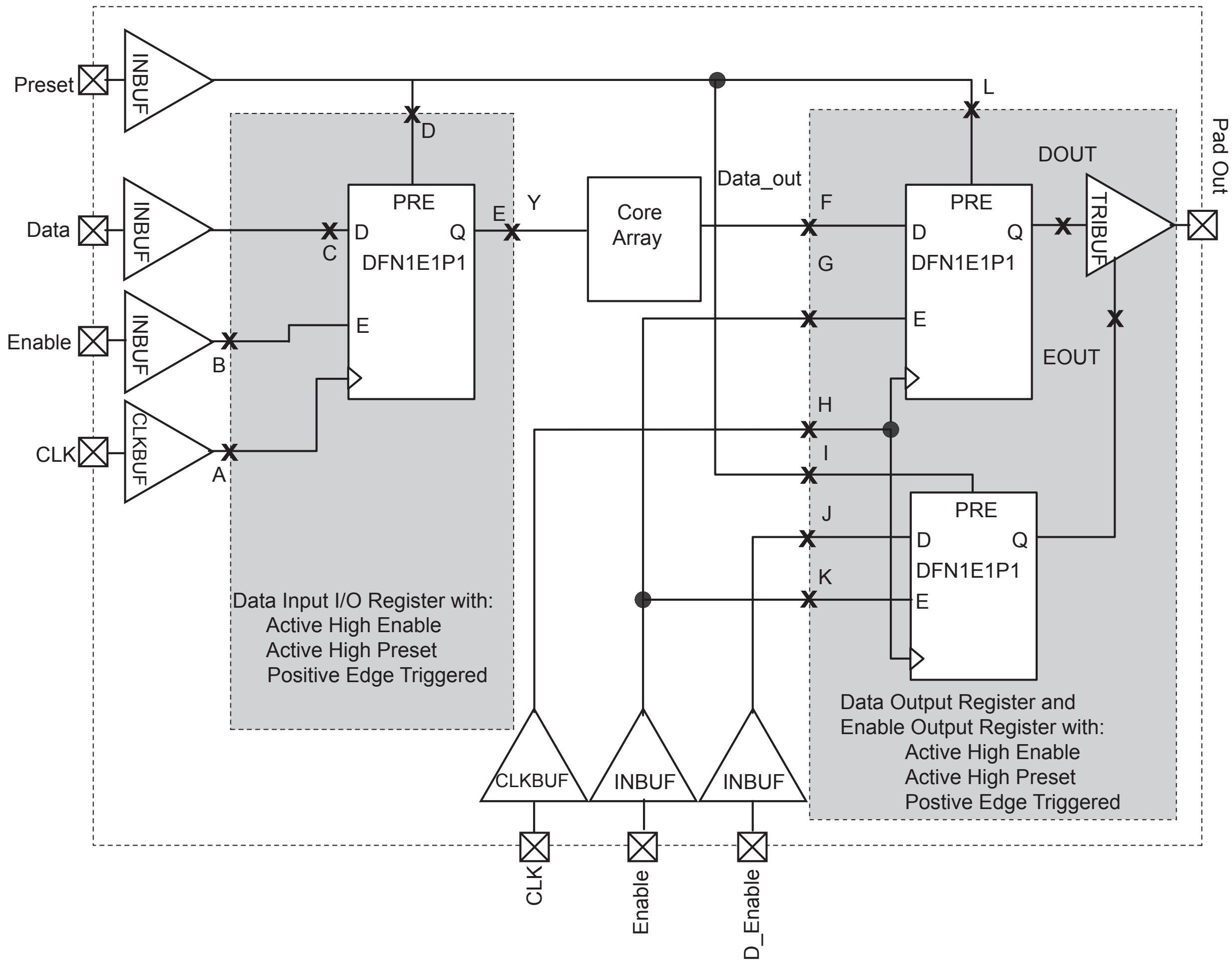


Figure 2-137 **• Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 3-11 **• AFS090 Quiescent Supply Current Characteristics (continued)**

Parameter	Description	Conditions	Temp.	Min	Typ	Max	Unit
ICCNVM	Embedded NVM current	Reset asserted, VCCNVM = 1.575 V	T_J = 25°C		10	40	µA
			T_J = 85°C		14	40	µA
			T_J = 100°C		14	40	µA
ICCPLL	1.5 V PLL quiescent current	Operational standby, VCCPLL = 1.575 V	T_J = 25°C		65	100	µA
			T_J = 85°C		65	100	µA
			T_J = 100°C		65	100	µA

Notes:

1. *ICC is the 1.5 V power supplies, ICC, ICCPLL, ICC15A, ICCNVM.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, and ICCI2.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

QN180		
Pin Number	AFS090 Function	AFS250 Function
A1	GNDQ	GNDQ
A2	VCCIB3	VCCIB3
A3	GAB2/IO52NDB3V0	IO74NDB3V0
A4	GFA2/IO51NDB3V0	IO71NDB3V0
A5	GFC2/IO50NDB3V0	IO69NPB3V0
A6	VCCIB3	VCCIB3
A7	GFA1/IO47PPB3V0	GFB1/IO67PPB3V0
A8	GEB0/IO45NDB3V0	NC
A9	XTAL1	XTAL1
A10	GNDOSC	GNDOSC
A11	GEC2/IO43PPB3V0	GEA1/IO61PPB3V0
A12	IO43NPB3V0	GEA0/IO61NPB3V0
A13	NC	VCCIB3
A14	GNDNVM	GNDNVM
A15	PCAP	PCAP
A16	VCC33PMP	VCC33PMP
A17	NC	NC
A18	AV0	AV0
A19	AG0	AG0
A20	ATRTN0	ATRTN0
A21	AG1	AG1
A22	AC1	AC1
A23	AV2	AV2
A24	AT2	AT2
A25	AT3	AT3
A26	AC3	AC3
A27	AV4	AV4
A28	AC4	AC4
A29	AT4	AT4
A30	NC	AG5
A31	NC	AV5
A32	ADCGNDREF	ADCGNDREF
A33	VCC33A	VCC33A
A34	GNDA	GNDA
A35	PTBASE	PTBASE
A36	VCCNVM	VCCNVM

QN180		
Pin Number	AFS090 Function	AFS250 Function
A37	VPUMP	VPUMP
A38	TDI	TDI
A39	TDO	TDO
A40	VJTAG	VJTAG
A41	GDB1/IO39PPB1V0	GDA1/IO54PPB1V0
A42	GDC1/IO38PDB1V0	GDB1/IO53PDB1V0
A43	VCC	VCC
A44	GCB0/IO35NPB1V0	GCB0/IO48NPB1V0
A45	GCC1/IO34PDB1V0	GCC1/IO47PDB1V0
A46	VCCIB1	VCCIB1
A47	GBC2/IO32PPB1V0	GBB2/IO41PPB1V0
A48	VCCIB1	VCCIB1
A49	NC	NC
A50	GBA0/IO29RSB0V0	GBB1/IO37RSB0V0
A51	VCCIB0	VCCIB0
A52	GBB0/IO27RSB0V0	GBC0/IO34RSB0V0
A53	GBC1/IO26RSB0V0	IO33RSB0V0
A54	IO24RSB0V0	IO29RSB0V0
A55	IO21RSB0V0	IO26RSB0V0
A56	VCCIB0	VCCIB0
A57	IO15RSB0V0	IO21RSB0V0
A58	IO10RSB0V0	IO13RSB0V0
A59	IO07RSB0V0	IO10RSB0V0
A60	GAC0/IO04RSB0V0	IO06RSB0V0
A61	GAB1/IO03RSB0V0	GAC1/IO05RSB0V0
A62	VCC	VCC
A63	GAA1/IO01RSB0V0	GAB0/IO02RSB0V0
A64	NC	NC
B1	VCOMPLA	VCOMPLA
B2	GAA2/IO52PDB3V0	GAC2/IO74PDB3V0
B3	GAC2/IO51PDB3V0	GFA2/IO71PDB3V0
B4	GFB2/IO50PDB3V0	GFB2/IO70PSB3V0
B5	VCC	VCC
B6	GFC0/IO49NDB3V0	GFC0/IO68NDB3V0
B7	GEB1/IO45PDB3V0	NC
B8	VCCOSC	VCCOSC

QN180		
Pin Number	AFS090 Function	AFS250 Function
C21	AG2	AG2
C22	NC	NC
C23	NC	NC
C24	NC	NC
C25	NC	AT5
C26	GNDAQ	GNDAQ
C27	NC	NC
C28	NC	NC
C29	NC	NC
C30	NC	NC
C31	GND	GND
C32	NC	NC
C33	NC	NC
C34	NC	NC
C35	GND	GND
C36	GDB0/IO39NPB1V0	GDA0/IO54NPB1V0
C37	GDA1/IO37NSB1V0	GDC0/IO52NSB1V0
C38	GCA0/IO36NDB1V0	GCA0/IO49NDB1V0
C39	GCB1/IO35PPB1V0	GCB1/IO48PPB1V0
C40	GND	GND
C41	GCA2/IO32NPB1V0	IO41NPB1V0
C42	GBB2/IO31NDB1V0	IO40NDB1V0
C43	NC	NC
C44	NC	GBA1/IO39RSB0V0
C45	NC	GBB0/IO36RSB0V0
C46	GND	GND
C47	NC	IO30RSB0V0
C48	IO22RSB0V0	IO27RSB0V0
C49	GND	GND
C50	IO13RSB0V0	IO16RSB0V0
C51	IO09RSB0V0	IO12RSB0V0
C52	IO06RSB0V0	IO09RSB0V0
C53	GND	GND
C54	NC	GAB1/IO03RSB0V0
C55	NC	GAA0/IO00RSB0V0
C56	NC	NC

QN180		
Pin Number	AFS090 Function	AFS250 Function
D1	NC	NC
D2	NC	NC
D3	NC	NC
D4	NC	NC

PQ208		
Pin Number	AFS250 Function	AFS600 Function
147	GCC1/IO47PDB1V0	IO39NDB2V0
148	IO42NDB1V0	GCA2/IO39PDB2V0
149	GBC2/IO42PDB1V0	IO31NDB2V0
150	VCCIB1	GBB2/IO31PDB2V0
151	GND	IO30NDB2V0
152	VCC	GBA2/IO30PDB2V0
153	IO41NDB1V0	VCCIB2
154	GBB2/IO41PDB1V0	GNDQ
155	IO40NDB1V0	VCOMPLB
156	GBA2/IO40PDB1V0	VCCPLB
157	GBA1/IO39RSB0V0	VCCIB1
158	GBA0/IO38RSB0V0	GNDQ
159	GBB1/IO37RSB0V0	GBB1/IO27PPB1V1
160	GBB0/IO36RSB0V0	GBA1/IO28PPB1V1
161	GBC1/IO35RSB0V0	GBB0/IO27NPB1V1
162	VCCIB0	GBA0/IO28NPB1V1
163	GND	VCCIB1
164	VCC	GND
165	GBC0/IO34RSB0V0	VCC
166	IO33RSB0V0	GBC1/IO26PDB1V1
167	IO32RSB0V0	GBC0/IO26NDB1V1
168	IO31RSB0V0	IO24PPB1V1
169	IO30RSB0V0	IO23PPB1V1
170	IO29RSB0V0	IO24NPB1V1
171	IO28RSB0V0	IO23NPB1V1
172	IO27RSB0V0	IO22PPB1V0
173	IO26RSB0V0	IO21PPB1V0
174	IO25RSB0V0	IO22NPB1V0
175	VCCIB0	IO21NPB1V0
176	GND	IO20PSB1V0
177	VCC	IO19PSB1V0
178	IO24RSB0V0	IO14NSB0V1
179	IO23RSB0V0	IO12PDB0V1
180	IO22RSB0V0	IO12NDB0V1
181	IO21RSB0V0	VCCIB0
182	IO20RSB0V0	GND
183	IO19RSB0V0	VCC

PQ208		
Pin Number	AFS250 Function	AFS600 Function
184	IO18RSB0V0	IO10PPB0V1
185	IO17RSB0V0	IO09PPB0V1
186	IO16RSB0V0	IO10NPB0V1
187	IO15RSB0V0	IO09NPB0V1
188	VCCIB0	IO08PPB0V1
189	GND	IO07PPB0V1
190	VCC	IO08NPB0V1
191	IO14RSB0V0	IO07NPB0V1
192	IO13RSB0V0	IO06PPB0V0
193	IO12RSB0V0	IO05PPB0V0
194	IO11RSB0V0	IO06NPB0V0
195	IO10RSB0V0	IO04PPB0V0
196	IO09RSB0V0	IO05NPB0V0
197	IO08RSB0V0	IO04NPB0V0
198	IO07RSB0V0	GAC1/IO03PDB0V0
199	IO06RSB0V0	GAC0/IO03NDB0V0
200	GAC1/IO05RSB0V0	VCCIB0
201	VCCIB0	GND
202	GND	VCC
203	VCC	GAB1/IO02PDB0V0
204	GAC0/IO04RSB0V0	GAB0/IO02NDB0V0
205	GAB1/IO03RSB0V0	GAA1/IO01PDB0V0
206	GAB0/IO02RSB0V0	GAA0/IO01NDB0V0
207	GAA1/IO01RSB0V0	GNDQ
208	GAA0/IO00RSB0V0	VCCIB0

Revision	Changes	Page
Advance v0.8 (continued)	This sentence was updated in the "No-Glitch MUX (NGMUX)" section to delete GLA: The GLMUXCFG[1:0] configuration bits determine the source of the CLK inputs (i.e., internal signal or GLC).	2-32
	In Table 2-13 • NGMUX Configuration and Selection Table, 10 and 11 were deleted.	2-32
	The method to enable sleep mode was updated for bit 0 in Table 2-16 • RTC Control/Status Register.	2-38
	S2 was changed to D2 in Figure 2-39 • Read Waveform (Pipe Mode, 32-bit access) for RD[31:0] was updated.	2-51
	The definitions for bits 2 and 3 were updated in Table 2-24 • Page Status Bit Definition.	2-52
	Figure 2-46 • FlashROM Timing Diagram was updated.	2-58
	Table 2-26 • FlashROM Access Time is new.	2-58
	Figure 2-55 • Write Access After Write onto Same Address, Figure 2-56 • Read Access After Write onto Same Address, and Figure 2-57 • Write Access After Read onto Same Address are new.	2-68–2-70
	Table 2-31 • RAM4K9 and Table 2-32 • RAM512X18 were updated.	2-71, 2-72
	The VAREF and SAMPLE functions were updated in Table 2-36 • Analog Block Pin Description.	2-82
	The title of Figure 2-72 • Timing Diagram for Current Monitor Strobe was updated to add the word "positive."	2-91
	The "Gate Driver" section was updated to give information about the switching rate in High Current Drive mode.	2-94
	The "ADC Description" section was updated to include information about the SAMPLE and BUSY signals and the maximum frequencies for SYSCLK and ADCCLK. EQ 2 was updated to add parentheses around the entire expression in the denominator.	2-102
	Table 2-46 · Analog Channel Specifications and Table 2-47 · ADC Characteristics in Direct Input Mode were updated.	2-118, 2-121
	The note was removed from Table 2-55 • Analog Multiplexer Truth Table—AV (x = 0), AC (x = 1), and AT (x = 3).	2-131
	Table 2-63 • Internal Temperature Monitor Control Truth Table is new.	2-132
	The "Cold-Sparing Support" section was updated to add information about cases where current draw can occur.	2-143
	Figure 2-104 • Solution 4 was updated.	2-147
	Table 2-75 • Fusion Standard I/O Standards—OUT_DRIVE Settings was updated.	2-153
	The "GNDA Ground (analog)" section and "GNDAQ Ground (analog quiet)" section were updated to add information about maximum differential voltage.	2-224
	The "V_{AREF} Analog Reference Voltage" section and "VPUMP Programming Supply Voltage" section were updated.	2-226
	The "$V_{CCPLA/B}$ PLL Supply Voltage" section was updated to include information about the east and west PLLs.	2-225
	The V_{COMPLF} pin description was deleted.	N/A
	The "Axy Analog Input/Output" section was updated with information about grounding and floating the pin.	2-226