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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 27648 |
| Number of I/O | 60 |
| Number of Gates | 90000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 180-WFQFN Dual Rows, Exposed Pad |
| Supplier Device Package | 180-QFN (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/afs090-qng180i |

# Product Ordering Codes

M1AFS600 – 1 FG G 256 Y I

- I: Application (junction temperature range)
  - Blank = Commercial (0 to +85°C)
  - I = Industrial (–40 to +100°C)
  - PP = Pre-Production
  - ES = Engineering Silicon (room temperature only)
- Y: Security Feature
  - Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
  - Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
- 256: Package Lead Count
- G: Lead-Free Packaging Options
  - Blank = Standard Packaging
  - G = RoHS-Compliant (green) Packaging
- FG: Package Type
  - QN = Quad Flat No Lead (0.5 mm pitch)[1]
  - PQ = Plastic Quad Flat Pack (0.5 mm pitch)
  - FG = Fine Pitch Ball Grid Array (1.0 mm pitch)[2]
- 1: Speed Grade
  - Blank = Standard
  - 1 = 15% Faster than Standard
  - 2 = 25% Faster than Standard
- M1AFS600: Part Number

**Fusion Devices**

AFS090 = 90,000 System Gates
AFS250 = 250,000 System Gates
AFS600 = 600,000 System Gates
AFS1500 = 1,500,000 System Gates

**ARM-Enabled Fusion Devices**

M1AFS250 = 250,000 System Gates
M1AFS600 = 600,000 System Gates
M1AFS1500 = 1,500,000 System Gates

**Pigeon Point Devices**

P1AFS600 = 600,000 System Gates
P1AFS1500 = 1,500,000 System Gates

**MicroBlade Devices**

U1AFS250 = 250,000 System Gates
U1AFS600 = 600,000 System Gates
U1AFS1500 = 1,500,000 System Gates

*Notes:*

1. *For Fusion devices, Quad Flat No Lead packages are only offered as RoHS compliant, QNG packages.*
2. *MicroBlade and Pigeon Point devices only support FG packages.*

# Fusion Device Status

| Fusion | Status | Cortex-M1 | Status | Pigeon Point | Status | MicroBlade | Status |
|---|---|---|---|---|---|---|---|
| AFS090 | Production | | | | | | |
| AFS250 | Production | M1AFS250 | Production | | | U1AFS250 | Production |
| AFS600 | Production | M1AFS600 | Production | P1AFS600 | Production | U1AFS600 | Production |
| AFS1500 | Production | M1AFS1500 | Production | P1AFS1500 | Production | U1AFS1500 | Production |

## VersaTile Characteristics

### Sample VersaTile Specifications—Combinatorial Module

The Fusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library (Figure 2-3). For more details, refer to the *IGLOO, ProASIC3, SmartFusion, and Fusion Macro Library Guide*.

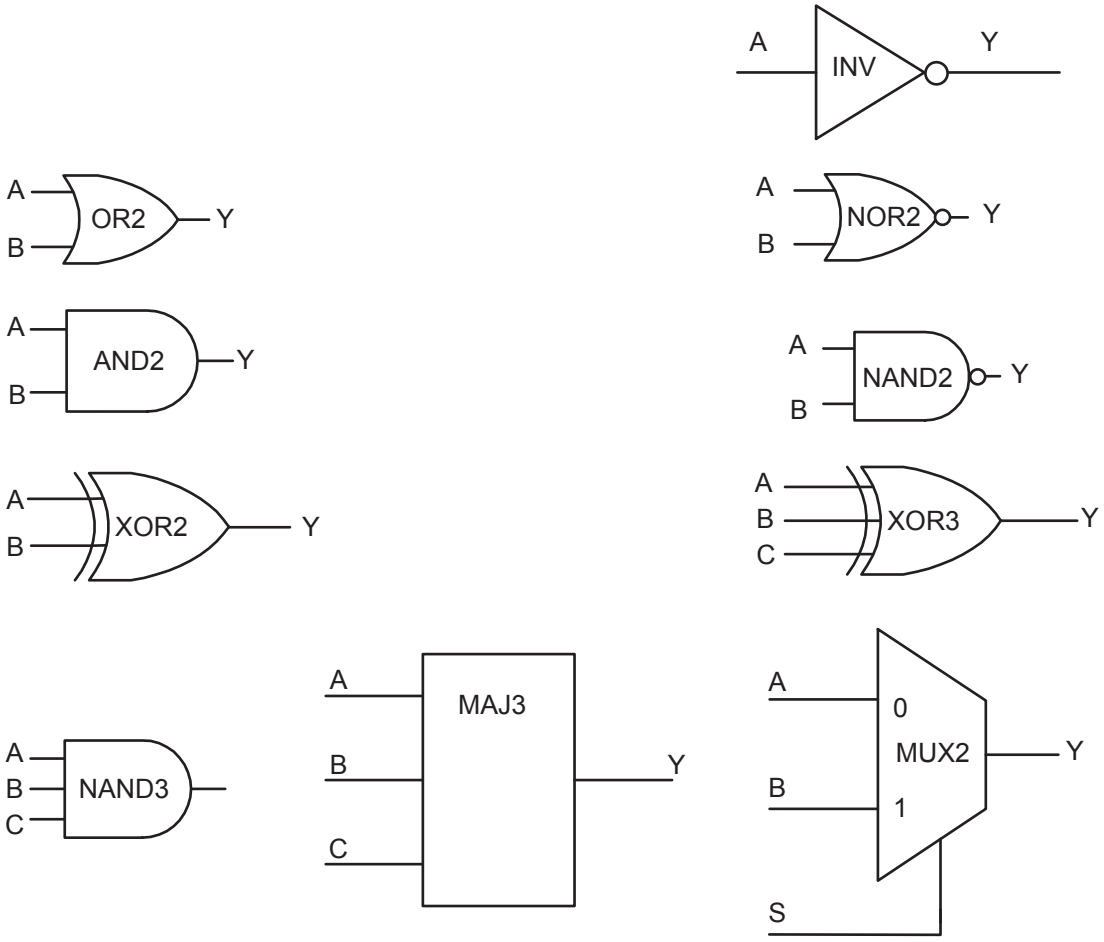



***Figure 2-3 •*** **Sample of Combinatorial Cells**

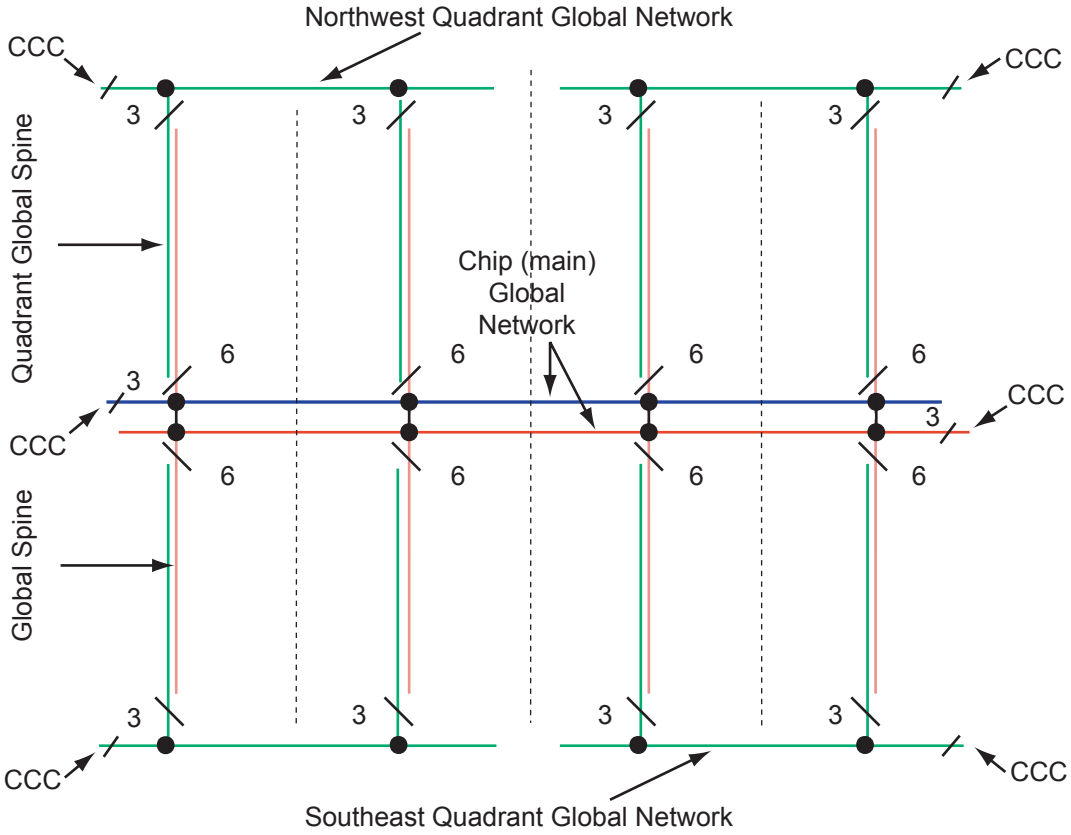



***Figure 2-12 •*** **Global Network Architecture**

***Table 2-4 •*** **Globals/Spines/Rows by Device**

| | AFS090 | AFS250 | AFS600 | AFS1500 |
|---|---|---|---|---|
| Global VersaNets (trees)* | 9 | 9 | 9 | 9 |
| VersaNet Spines/Tree | 4 | 8 | 12 | 20 |
| Total Spines | 36 | 72 | 108 | 180 |
| VersaTiles in Each Top or Bottom Spine | 384 | 768 | 1,152 | 1,920 |
| Total VersaTiles | 2,304 | 6,144 | 13,824 | 38,400 |

*Note: *There are six chip (main) globals and three globals per quadrant.*

## Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-14 indicates, this access system is contiguous.

There is no break in the middle of the chip for north and south I/O VersaNet access. This is different from the quadrant clocks, located in these ribs, which only reach the middle of the rib. Refer to the *Using Global Resources in Actel Fusion Devices* application note.

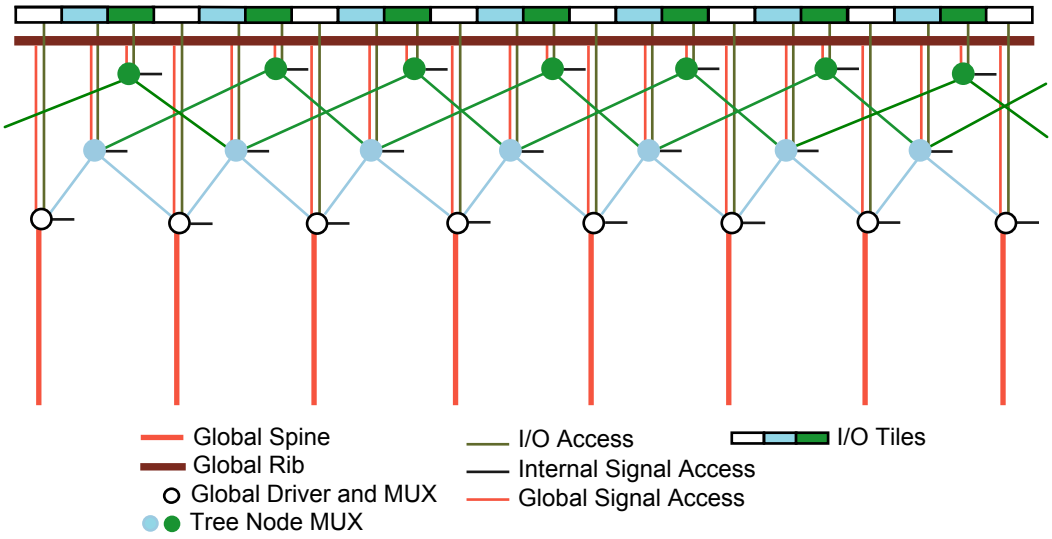



***Figure 2-14 •*** **Clock Aggregation Tree Architecture**

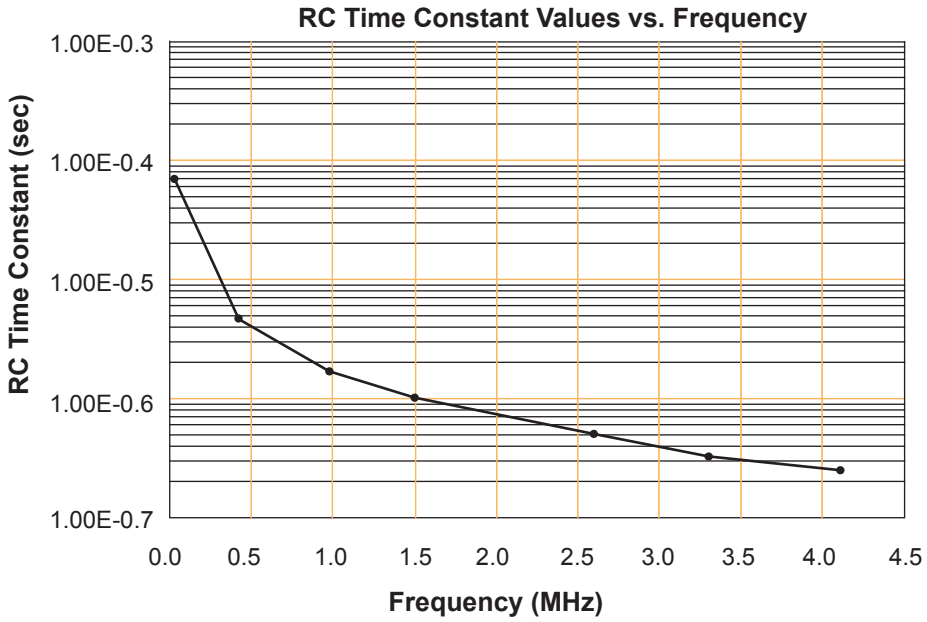
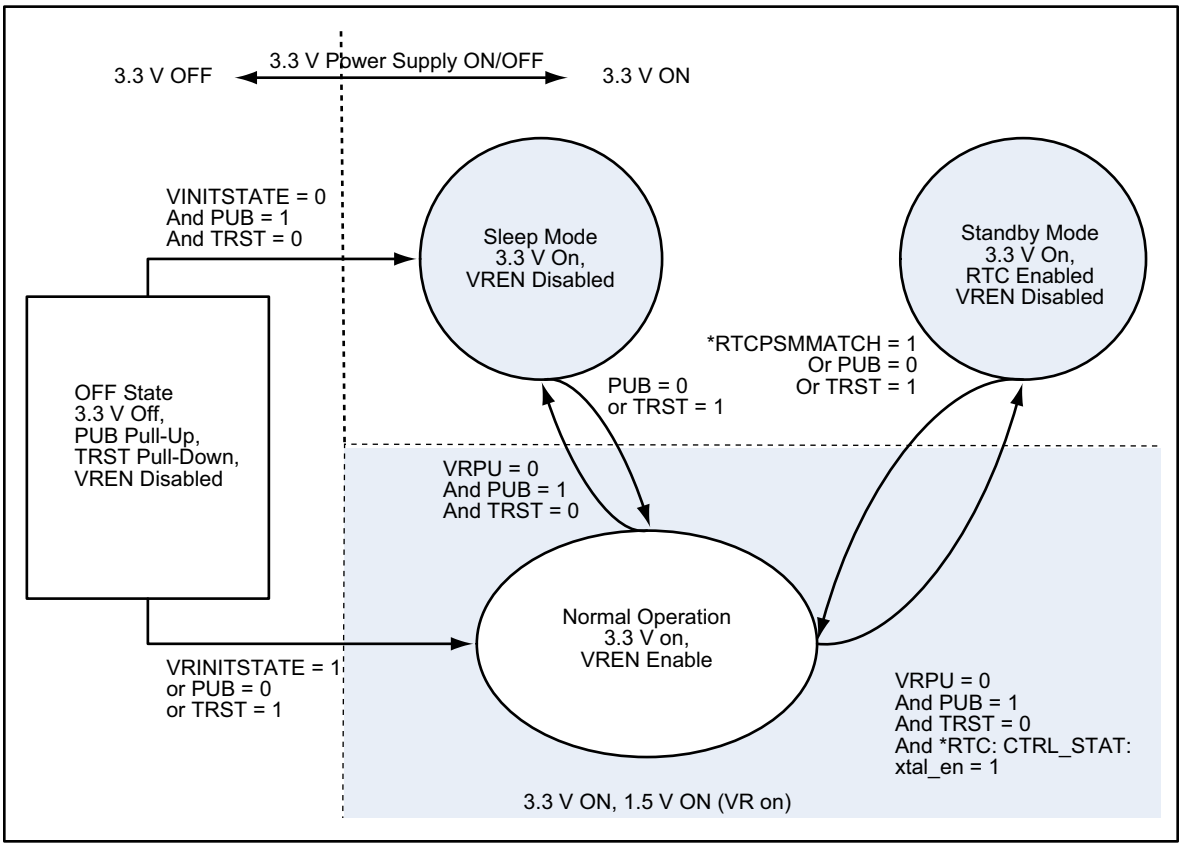



***Figure 2-18 •*** **Crystal Oscillator: RC Time Constant Values vs. Frequency (typical)**

***Table 2-10 •*** **XTLOSC Signals Descriptions**

| Signal Name | Width | Direction | Function | | |
|---|---|---|---|---|---|
| XTL_EN* | 1 | | Enables the crystal. Active high. | | |
| XTL_MODE* | 2 | | Settings for the crystal clock for different frequency. | | |
| | | | **Value** | **Modes** | **Frequency Range** |
| | | | b'00 | RC network | 32 KHz to 4 MHz |
| | | | b'01 | Low gain | 32 to 200 KHz |
| | | | b'10 | Medium gain | 0.20 to 2.0 MHz |
| | | | b'11 | High gain | 2.0 to 20.0 MHz |
| SELMODE | 1 | IN | Selects the source of XTL_MODE and also enables the XTL_EN. Connect from RTCXTLSEL from AB. | | |
| | | | 0 | For normal operation or sleep mode, XTL_EN depends on FPGA_EN, XTL_MODE depends on MODE | |
| | | | 1 | For Standby mode, XTL_EN is enabled, XTL_MODE depends on RTC_MODE | |
| RTC_MODE[1:0] | 2 | IN | Settings for the crystal clock for different frequency ranges. XTL_MODE uses RTC_MODE when SELMODE is '1'. | | |
| MODE[1:0] | 2 | IN | Settings for the crystal clock for different frequency ranges. XTL_MODE uses MODE when SELMODE is '0'. In Standby, MODE inputs will be 0's. | | |
| FPGA_EN* | 1 | IN | 0 when 1.5 V is not present for VCC 1 when 1.5 V is present for VCC | | |
| XTL | 1 | IN | Crystal Clock source | | |
| CLKOUT | 1 | OUT | Crystal Clock output | | |

*Note: *Internal signal—does not exist in macro.*




*Note: * To enter and exit standby mode without any external stimulus on PUB or TRST, the vr_en_mat in the CTRL_STAT register must also be set to 1, so that RTCPSMMATCH will assert when a match occurs; hence the device exits standby mode.*

***Figure 2-31 •*** **State Diagram for All Different Power Modes**

When TRST is 1 or PUB is 0, the 1.5 V voltage regulator is always ON, putting the Fusion device in normal operation at all times. Therefore, when the JTAG port is not in reset, the Fusion device cannot enter sleep mode or standby mode.

To enter standby mode, the Fusion device must first power-up into normal operation. The RTC is enabled through the RTC Control/Status Register described in the "Real-Time Counter (part of AB macro)" section on page 2-33. A match value corresponding to the wake-up time is loaded into the Match Register. The 1.5 V voltage regulator is disabled by setting VRPU to 0 to allow the Fusion device to enter standby mode, when the 1.5 V supply is off but the RTC remains on.

## SRAM Characteristics

### Timing Waveforms

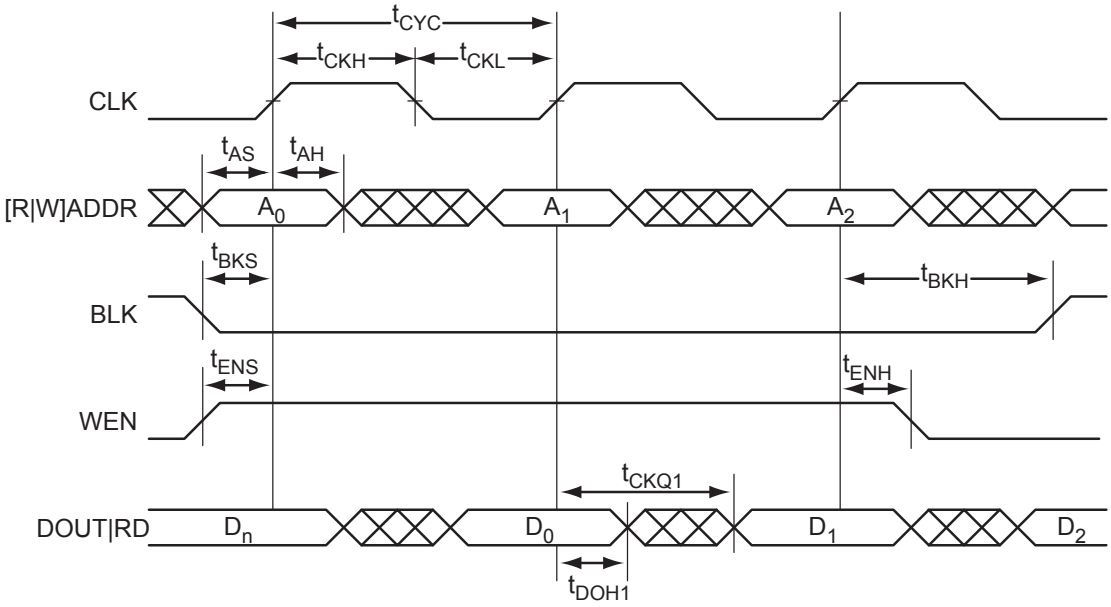



***Figure 2-50 •*** **RAM Read for Flow-Through Output. Applicable to both RAM4K9 and RAM512x18.**

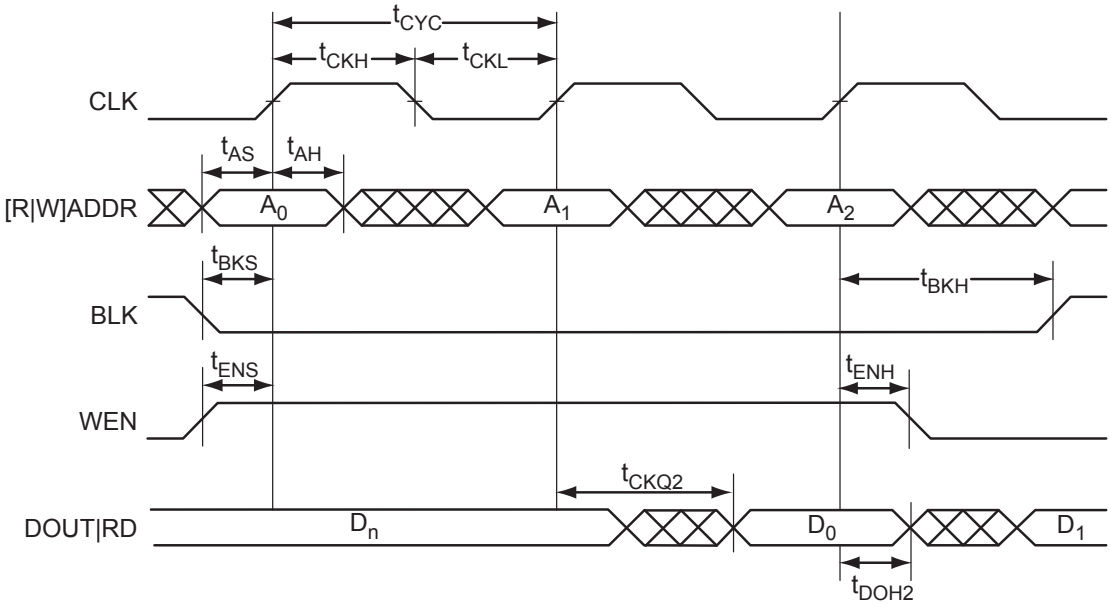



***Figure 2-51 •*** **RAM Read for Pipelined Output. Applicable to both RAM4K9 and RAM512x18.**

### Timing Characteristics

**Table 2-35 • FIFO**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup time | 1.34 | 1.52 | 1.79 | ns |
| $t_{ENH}$ | REN, WEN Hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{BKS}$ | BLK Setup time | 0.19 | 0.22 | 0.26 | ns |
| $t_{BKH}$ | BLK Hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{DS}$ | Input data (WD) Setup time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input data (WD) Hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 2.17 | 2.47 | 2.90 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 0.94 | 1.07 | 1.26 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| $t_{RSTAF}$ | RESET Low to Almost-Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| $t_{RSTBQ}$ | RESET Low to Data out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock Cycle time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 310 | 272 | 231 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### *Channel Input Offset Error*

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to ½ of LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

### *Total Channel Error*

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-68 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-68, the Total Channel Error would be a negative number.

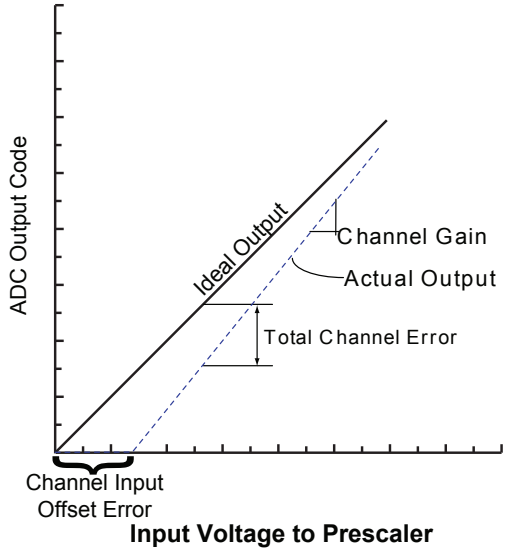



***Figure 2-68 •*** **Total Channel Error Example**

## Analog Quad ACM Description

Table 2-56 maps out the ACM space associated with configuration of the Analog Quads within the Analog Block. Table 2-56 shows the byte assignment within each quad and the function of each bit within each byte. Subsequent tables will explain each bit setting and how it corresponds to a particular configuration. After 3.3 V and 1.5 V are applied to Fusion, Analog Quad configuration registers are loaded with default settings until the initialization and configuration state machine changes them to user-defined settings.

***Table 2-56* • Analog Quad ACM Byte Assignment**

| Byte | Bit | Signal (Bx) | Function | Default Setting |
|---|---|---|---|---|
| Byte 0 (AV) | 0 | B0[0] | Scaling factor control – prescaler | Highest voltage range |
| | 1 | B0[1] | | |
| | 2 | B0[2] | | |
| | 3 | B0[3] | Analog MUX select | Prescaler |
| | 4 | B0[4] | Current monitor switch | Off |
| | 5 | B0[5] | Direct analog input switch | Off |
| | 6 | B0[6] | Selects V-pad polarity | Positive |
| | 7 | B0[7] | Prescaler op amp mode | Power-down |
| Byte 1 (AC) | 0 | B1[0] | Scaling factor control – prescaler | Highest voltage range |
| | 1 | B1[1] | | |
| | 2 | B1[2] | | |
| | 3 | B1[3] | Analog MUX select | Prescaler |
| | 4 | B1[4] | | |
| | 5 | B1[5] | Direct analog input switch | Off |
| | 6 | B1[6] | Selects C-pad polarity | Positive |
| | 7 | B1[7] | Prescaler op amp mode | Power-down |
| Byte 2 (AG) | 0 | B2[0] | Internal chip temperature monitor * | Off |
| | 1 | B2[1] | Spare | – |
| | 2 | B2[2] | Current drive control | Lowest current |
| | 3 | B2[3] | | |
| | 4 | B2[4] | Spare | – |
| | 5 | B2[5] | Spare | – |
| | 6 | B2[6] | Selects G-pad polarity | Positive |
| | 7 | B2[7] | Selects low/high drive | Low drive |
| Byte 3 (AT) | 0 | B3[0] | Scaling factor control – prescaler | Highest voltage range |
| | 1 | B3[1] | | |
| | 2 | B3[2] | | |
| | 3 | B3[3] | Analog MUX select | Prescaler |
| | 4 | B3[4] | | |
| | 5 | B3[5] | Direct analog input switch | Off |
| | 6 | B3[6] | – | – |
| | 7 | B3[7] | Prescaler op amp mode | Power-down |

*Note: *For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.*

***Table 2-73* • Maximum I/O Frequency for Single-Ended, Voltage-Referenced, and Differential I/Os; All I/O Bank Types (maximum drive strength and high slew selected)**

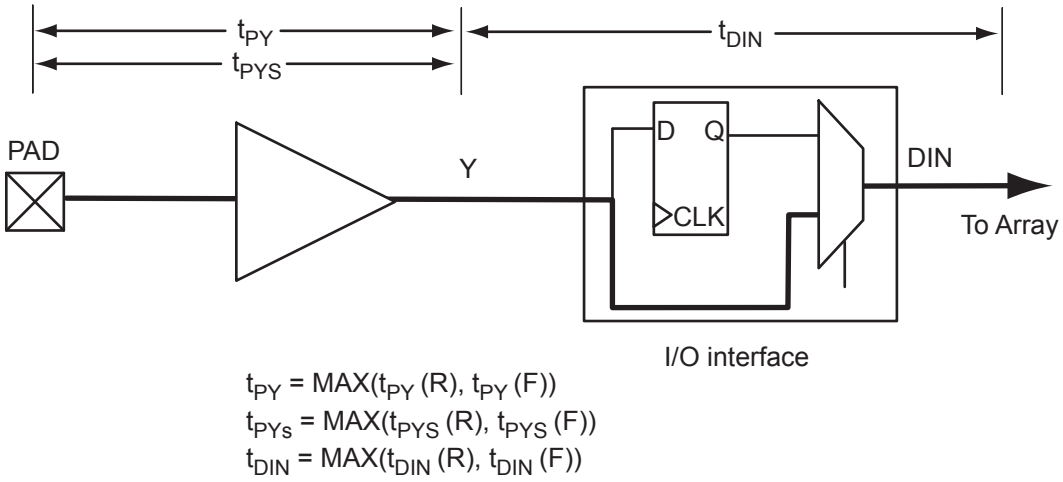
| Specification | Performance Up To |
|---|---|
| LVTTL/LVCMOS 3.3 V | 200 MHz |
| LVCMOS 2.5 V | 250 MHz |
| LVCMOS 1.8 V | 200 MHz |
| LVCMOS 1.5 V | 130 MHz |
| PCI | 200 MHz |
| PCI-X | 200 MHz |
| HSTL-I | 300 MHz |
| HSTL-II | 300 MHz |
| SSTL2-I | 300 MHz |
| SSTL2-II | 300 MHz |
| SSTL3-I | 300 MHz |
| SSTL3-II | 300 MHz |
| GTL+ 3.3 V | 300 MHz |
| GTL+ 2.5 V | 300 MHz |
| GTL 3.3 V | 300 MHz |
| GTL 2.5 V | 300 MHz |
| LVDS | 350 MHz |
| LVPECL | 300 MHz |

***Table 2-77* • Comparison Table for 5 V–Compliant Receiver Scheme**

| Scheme | Board Components | Speed | Current Limitations |
|---|---|---|---|
| 1 | Two resistors | Low to high[1] | Limited by transmitter's drive strength |
| 2 | Resistor and Zener 3.3 V | Medium | Limited by transmitter's drive strength |
| 3 | Bus switch | High | N/A |
| 4 | Minimum resistor value[2]<br>R = 47 Ω at $T_J$ = 70°C<br>R = 150 Ω at $T_J$ = 85°C<br>R = 420 Ω at $T_J$ = 100°C | Medium | Maximum diode current at 100% duty cycle, signal constantly at '1'<br>52.7 mA at $T_J$ =70°C / 10-year lifetime<br>16.5 mA at $T_J$ = 85°C / 10-year lifetime<br>5.9 mA at $T_J$ = 100°C / 10-year lifetime<br>For duty cycles other than 100%, the currents can be increased by a factor = 1 / (duty cycle).<br>Example: 20% duty cycle at 70°C<br>Maximum current = (1 / 0.2) * 52.7 mA = 5 * 52.7 mA = 263.5 mA |

*Notes:*

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long-term reliability.*




$t_{PY} = MAX(t_{PY}(R), t_{PY}(F))$
$t_{PYs} = MAX(t_{PYS}(R), t_{PYS}(F))$
$t_{DIN} = MAX(t_{DIN}(R), t_{DIN}(F))$

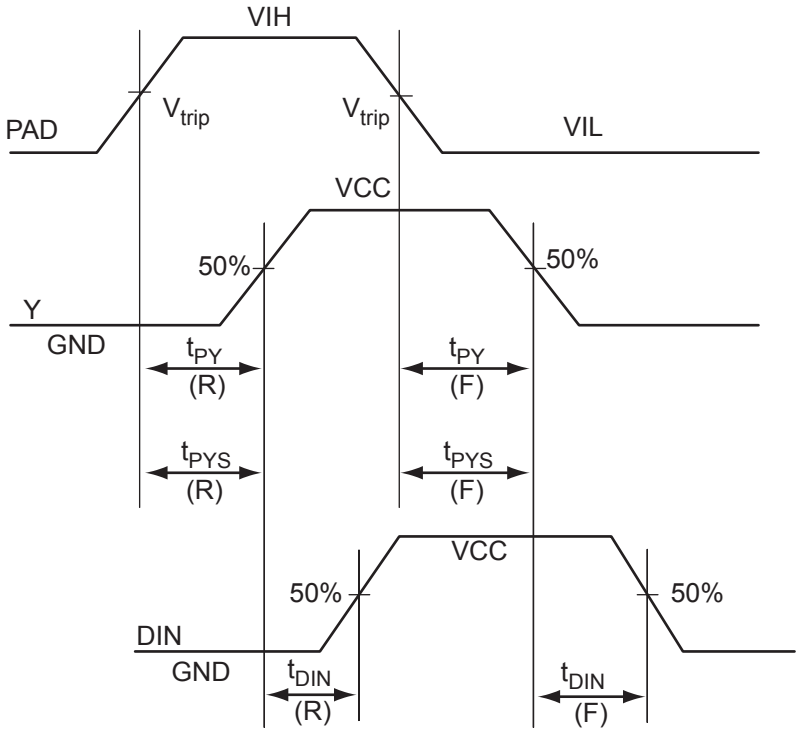



***Figure 2-116* • Input Buffer Timing Model and Delays (example)**

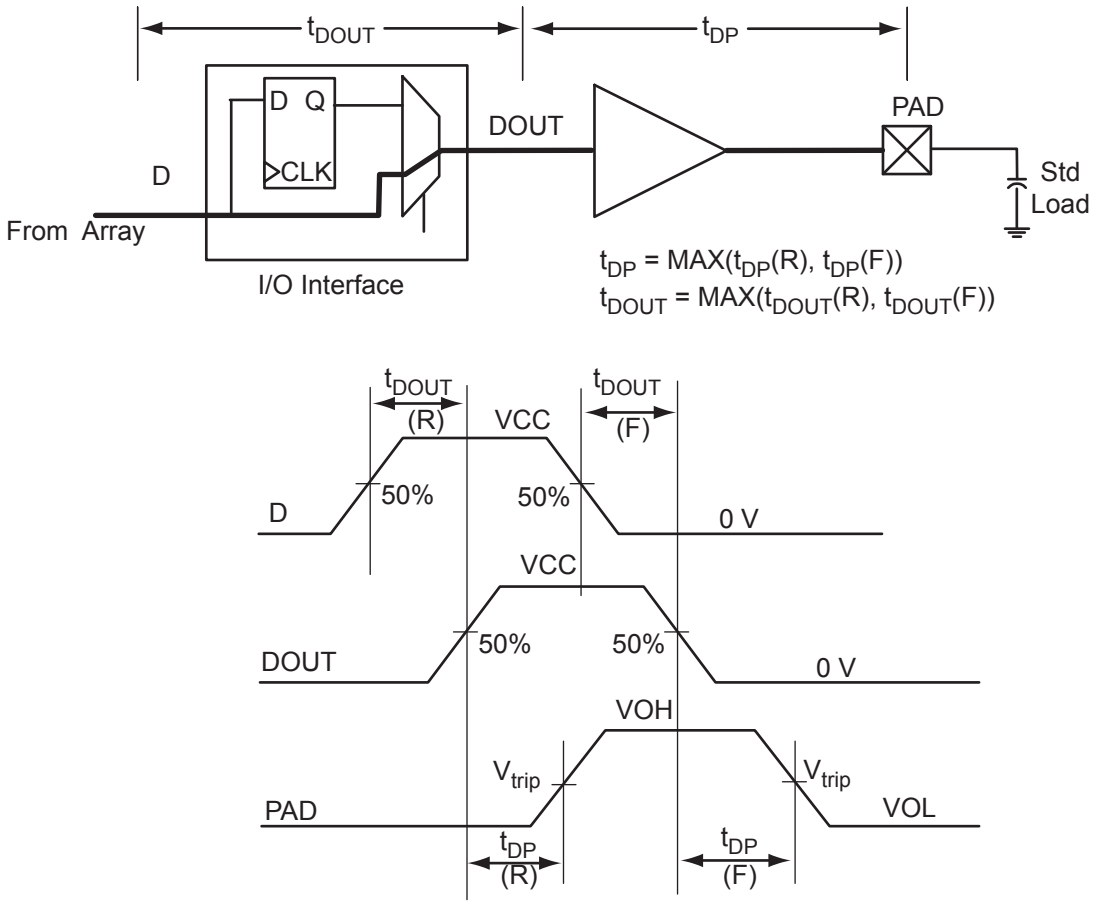



***Figure 2-117* • Output Buffer Model and Delays (example)**

## Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

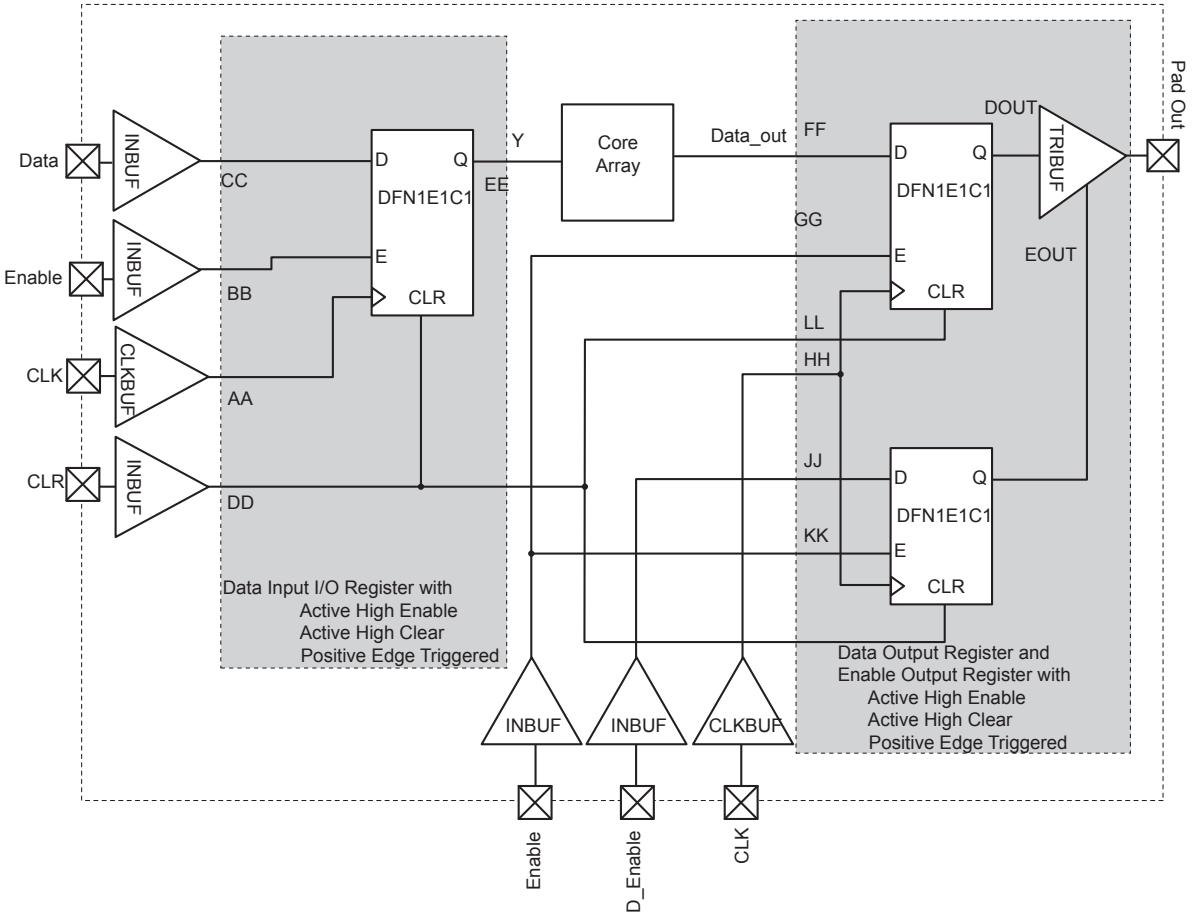



***Figure 2-138 •*** **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

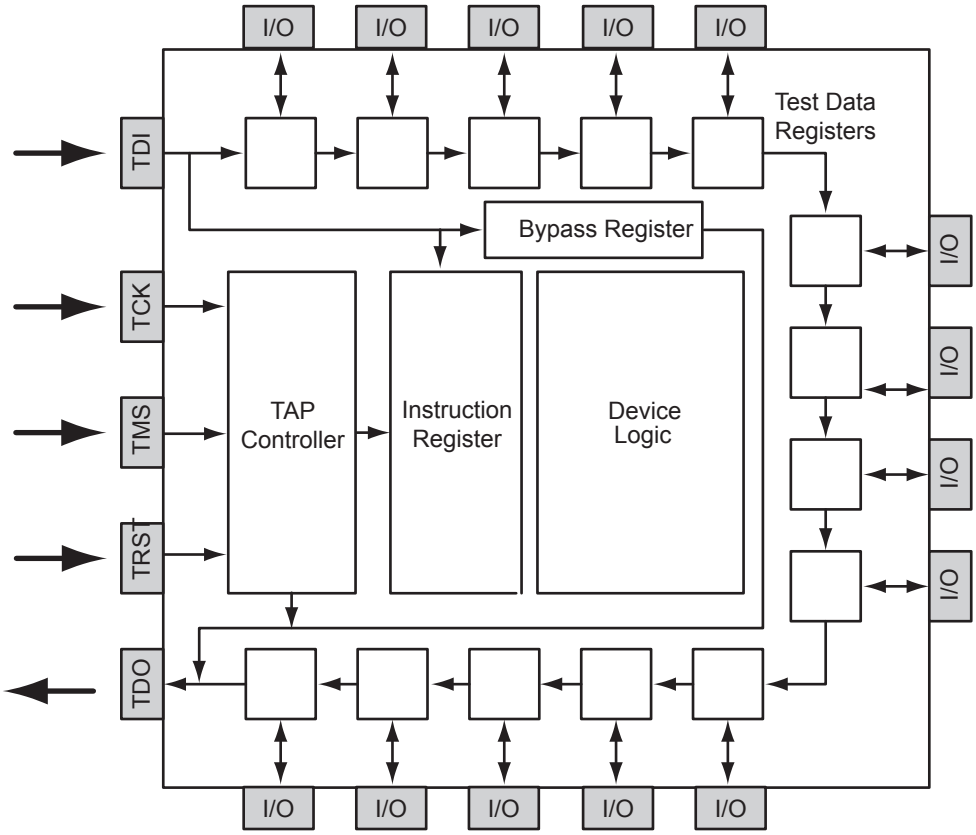



***Figure 2-146* • Boundary Scan Chain in Fusion**

***Table 2-185* • Boundary Scan Opcodes**

| | Hex Opcode |
|---|---|
| EXTEST | 00 |
| HIGHZ | 07 |
| USERCODE | 0E |
| SAMPLE/PRELOAD | 01 |
| IDCODE | 0F |
| CLAMP | 05 |
| BYPASS | FF |

# Calculating Power Dissipation

## Quiescent Supply Current

***Table 3-8 •*** **AFS1500 Quiescent Supply Current Characteristics**

| Parameter | Description | Conditions | Temp. | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| ICC[1] | 1.5 V quiescent current | Operational standby[4], VCC = 1.575 V | $T_J$ = 25°C | | 20 | 40 | mA |
| | | | $T_J$ = 85°C | | 32 | 65 | mA |
| | | | $T_J$ = 100°C | | 59 | 120 | mA |
| | | Standby mode[5] or Sleep mode[6], VCC = 0 V | | | 0 | 0 | µA |
| ICC33[2] | 3.3 V analog supplies current | Operational standby[4], VCC33 = 3.63 V | $T_J$ = 25°C | | 9.8 | 13 | mA |
| | | | $T_J$ = 85°C | | 10.7 | 14 | mA |
| | | | $T_J$ = 100°C | | 10.8 | 15 | mA |
| | | Operational standby, only Analog Quad and –3.3 V output ON, VCC33 = 3.63 V | $T_J$ = 25°C | | 0.31 | 2 | mA |
| | | | $T_J$ = 85°C | | 0.35 | 2 | mA |
| | | | $T_J$ = 100°C | | 0.45 | 2 | mA |
| | | Standby mode[5], VCC33 = 3.63 V | $T_J$ = 25°C | | 2.9 | 3.6 | mA |
| | | | $T_J$ = 85°C | | 2.9 | 4 | mA |
| | | | $T_J$ = 100°C | | 3.3 | 6 | mA |
| | | Sleep mode[6], VCC33 = 3.63 V | $T_J$ = 25°C | | 17 | 19 | µA |
| | | | $T_J$ = 85°C | | 18 | 20 | µA |
| | | | $T_J$ = 100°C | | 24 | 25 | µA |
| ICCI[3] | I/O quiescent current | Operational standby[4], Standby mode, and Sleep Mode[6], VCCIx = 3.63 V | $T_J$ = 25°C | | 417 | 649 | µA |
| | | | $T_J$ = 85°C | | 417 | 649 | µA |
| | | | $T_J$ = 100°C | | 417 | 649 | µA |

*Notes:*

1. *ICC is the 1.5 V power supplies, ICC and ICC15A.*
2. *ICC33A includes ICC33A, ICC33PMP, and ICCOSC.*
3. *ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.*
4. *Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.*
5. *XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.*
6. *Sleep Mode, VCC = VJTAG = VPUMP = 0 V.*

### Total Static Power Consumption—$P_{STAT}$

Number of Quads used: $N_{QUADS}$ = 4

Number of NVM blocks available (AFS600): $N_{NVM\text{-}BLOCKS}$ = 2

Number of input pins used: $N_{INPUTS}$ = 30

Number of output pins used: $N_{OUTPUTS}$ = 40

#### Operating Mode

$P_{STAT}$ = PDC1 + ($N_{NVM\text{-}BLOCKS}$ * PDC4) + PDC5 + ($N_{QUADS}$ * PDC6) + ($N_{INPUTS}$ * PDC7) + ($N_{OUTPUTS}$ * PDC8)

$P_{STAT}$ = 7.50 mW + (2 * 1.19 mW) + 8.25 mW + (4 * 3.30 mW) + (30 * 0.00) + (40 * 0.00)

$P_{STAT}$ = 31.33 mW

#### Standby Mode

$P_{STAT}$ = PDC2

$P_{STAT}$ = 0.03 mW

#### Sleep Mode

$P_{STAT}$ = PDC3

$P_{STAT}$ = 0.03 mW

### Total Power Consumption—$P_{TOTAL}$

In operating mode, the total power consumption of the device is 174.39 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{TOTAL}$ = 143.06 mW + 31.33 mW

$P_{TOTAL}$ = 174.39 mW

In standby mode, the total power consumption of the device is limited to 0.66 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{TOTAL}$ = 0.03 mW + 0.63 mW

$P_{TOTAL}$ = 0.66 mW

In sleep mode, the total power consumption of the device drops as low as 0.03 mW:

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{TOTAL}$ = 0.03 mW

| FG484 | | |
|---|---|---|
| Pin Number | AFS600 Function | AFS1500 Function |
| H13 | GND | GND |
| H14 | VCCIB1 | VCCIB1 |
| H15 | GND | GND |
| H16 | GND | GND |
| H17 | NC | IO53NDB2V0 |
| H18 | IO38PDB2V0 | IO57PDB2V0 |
| H19 | GCA2/IO39PDB2V0 | GCA2/IO59PDB2V0 |
| H20 | VCCIB2 | VCCIB2 |
| H21 | IO37NDB2V0 | IO54NDB2V0 |
| H22 | IO37PDB2V0 | IO54PDB2V0 |
| J1 | NC | IO112PPB4V0 |
| J2 | IO76NDB4V0 | IO113NDB4V0 |
| J3 | GFB2/IO74PDB4V0 | GFB2/IO109PDB4V0 |
| J4 | GFA2/IO75PDB4V0 | GFA2/IO110PDB4V0 |
| J5 | NC | IO112NPB4V0 |
| J6 | NC | IO104PDB4V0 |
| J7 | NC | IO111PDB4V0 |
| J8 | VCCIB4 | VCCIB4 |
| J9 | GND | GND |
| J10 | VCC | VCC |
| J11 | GND | GND |
| J12 | VCC | VCC |
| J13 | GND | GND |
| J14 | VCC | VCC |
| J15 | VCCIB2 | VCCIB2 |
| J16 | GCB2/IO40PDB2V0 | GCB2/IO60PDB2V0 |
| J17 | NC | IO58NDB2V0 |
| J18 | IO38NDB2V0 | IO57NDB2V0 |
| J19 | IO39NDB2V0 | IO59NDB2V0 |
| J20 | GCC2/IO41PDB2V0 | GCC2/IO61PDB2V0 |
| J21 | NC | IO55PSB2V0 |
| J22 | IO42PDB2V0 | IO56PDB2V0 |
| K1 | GFC2/IO73PDB4V0 | GFC2/IO108PDB4V0 |
| K2 | GND | GND |
| K3 | IO74NDB4V0 | IO109NDB4V0 |

| FG484 | | |
|---|---|---|
| Pin Number | AFS600 Function | AFS1500 Function |
| K4 | IO75NDB4V0 | IO110NDB4V0 |
| K5 | GND | GND |
| K6 | NC | IO104NDB4V0 |
| K7 | NC | IO111NDB4V0 |
| K8 | GND | GND |
| K9 | VCC | VCC |
| K10 | GND | GND |
| K11 | VCC | VCC |
| K12 | GND | GND |
| K13 | VCC | VCC |
| K14 | GND | GND |
| K15 | GND | GND |
| K16 | IO40NDB2V0 | IO60NDB2V0 |
| K17 | NC | IO58PDB2V0 |
| K18 | GND | GND |
| K19 | NC | IO68NPB2V0 |
| K20 | IO41NDB2V0 | IO61NDB2V0 |
| K21 | GND | GND |
| K22 | IO42NDB2V0 | IO56NDB2V0 |
| L1 | IO73NDB4V0 | IO108NDB4V0 |
| L2 | VCCOSC | VCCOSC |
| L3 | VCCIB4 | VCCIB4 |
| L4 | XTAL2 | XTAL2 |
| L5 | GFC1/IO72PDB4V0 | GFC1/IO107PDB4V0 |
| L6 | VCCIB4 | VCCIB4 |
| L7 | GFB1/IO71PDB4V0 | GFB1/IO106PDB4V0 |
| L8 | VCCIB4 | VCCIB4 |
| L9 | GND | GND |
| L10 | VCC | VCC |
| L11 | GND | GND |
| L12 | VCC | VCC |
| L13 | GND | GND |
| L14 | VCC | VCC |
| L15 | VCCIB2 | VCCIB2 |
| L16 | IO48PDB2V0 | IO70PDB2V0 |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| R21 | IO72NDB2V0 |
| R22 | IO72PDB2V0 |
| R23 | GND |
| R24 | IO71PDB2V0 |
| R25 | VCCIB2 |
| R26 | IO67NDB2V0 |
| T1 | GND |
| T2 | NC |
| T3 | GFA1/IO105PDB4V0 |
| T4 | GFA0/IO105NDB4V0 |
| T5 | IO101NDB4V0 |
| T6 | IO96PDB4V0 |
| T7 | IO96NDB4V0 |
| T8 | IO99NDB4V0 |
| T9 | IO97NDB4V0 |
| T10 | VCCIB4 |
| T11 | VCC |
| T12 | GND |
| T13 | VCC |
| T14 | GND |
| T15 | VCC |
| T16 | GND |
| T17 | VCCIB2 |
| T18 | IO83NDB2V0 |
| T19 | IO78NDB2V0 |
| T20 | GDA1/IO81PDB2V0 |
| T21 | GDB1/IO80PDB2V0 |
| T22 | IO73NDB2V0 |
| T23 | IO73PDB2V0 |
| T24 | IO71NDB2V0 |
| T25 | NC |
| T26 | GND |
| U1 | NC |
| U2 | NC |
| U3 | IO102PDB4V0 |
| U4 | IO102NDB4V0 |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| U5 | VCCIB4 |
| U6 | IO91PDB4V0 |
| U7 | IO91NDB4V0 |
| U8 | IO92PDB4V0 |
| U9 | GND |
| U10 | GND |
| U11 | VCC33A |
| U12 | GNDA |
| U13 | VCC33A |
| U14 | GNDA |
| U15 | VCC33A |
| U16 | GNDA |
| U17 | VCC |
| U18 | GND |
| U19 | IO74NDB2V0 |
| U20 | GDA0/IO81NDB2V0 |
| U21 | GDB0/IO80NDB2V0 |
| U22 | VCCIB2 |
| U23 | IO75NDB2V0 |
| U24 | IO75PDB2V0 |
| U25 | NC |
| U26 | NC |
| V1 | NC |
| V2 | VCCIB4 |
| V3 | IO100PPB4V0 |
| V4 | GND |
| V5 | IO95PDB4V0 |
| V6 | IO95NDB4V0 |
| V7 | VCCIB4 |
| V8 | IO92NDB4V0 |
| V9 | GNDNVM |
| V10 | GNDA |
| V11 | NC |
| V12 | AV4 |
| V13 | NC |
| V14 | AV5 |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| V15 | AC5 |
| V16 | NC |
| V17 | GNDA |
| V18 | IO77PPB2V0 |
| V19 | IO74PDB2V0 |
| V20 | VCCIB2 |
| V21 | IO82NDB2V0 |
| V22 | GDA2/IO82PDB2V0 |
| V23 | GND |
| V24 | GDC1/IO79PDB2V0 |
| V25 | VCCIB2 |
| V26 | NC |
| W1 | GND |
| W2 | IO94PPB4V0 |
| W3 | IO98PDB4V0 |
| W4 | IO98NDB4V0 |
| W5 | GEC1/IO90PDB4V0 |
| W6 | GEC0/IO90NDB4V0 |
| W7 | GND |
| W8 | VCCNVM |
| W9 | VCCIB4 |
| W10 | VCC15A |
| W11 | GNDA |
| W12 | AC4 |
| W13 | VCC33A |
| W14 | GNDA |
| W15 | AG5 |
| W16 | GNDA |
| W17 | PUB |
| W18 | VCCIB2 |
| W19 | TDI |
| W20 | GND |
| W21 | IO84NDB2V0 |
| W22 | GDC2/IO84PDB2V0 |
| W23 | IO77NPB2V0 |
| W24 | GDC0/IO79NDB2V0 |