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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 36864 |
| Number of I/O | 65 |
| Number of Gates | 250000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 180-WFQFN Dual Rows, Exposed Pad |
| Supplier Device Package | 180-QFN (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microsemi/afs250-1qng180 |

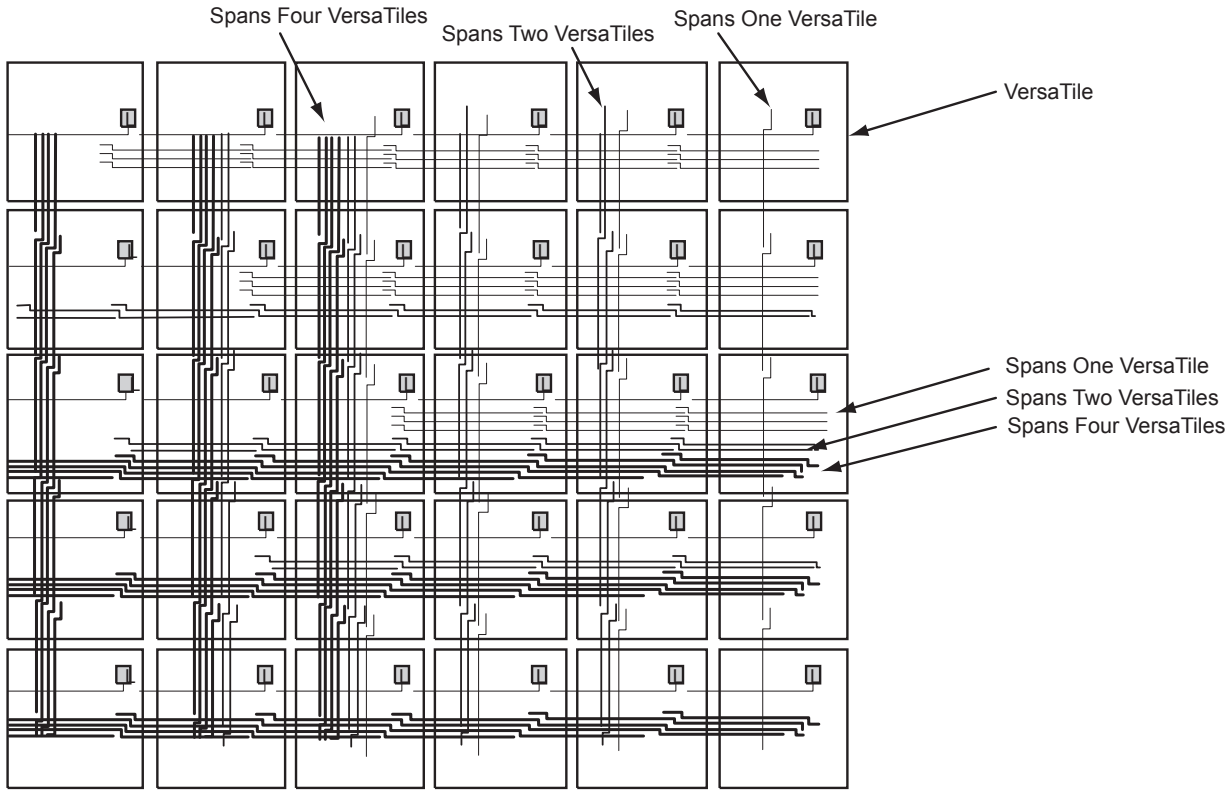


***Figure 2-9 •*** **Efficient Long-Line Resources**

***Table 2-19* • Flash Memory Block Pin Names (continued)**

| Interface Name | Width | Direction | Description |
|---|---|---|---|
| STATUS[1:0] | 2 | Out | Status of the last operation completed:<br>00: Successful completion<br>01: Read-/Unprotect-Page: single error detected and corrected<br>Write: operation addressed a write-protected page<br>Erase-Page: protection violation<br>Program: Page Buffer is unmodified<br>Protection violation<br>10: Read-/Unprotect-Page: two or more errors detected<br>11: Write: attempt to write to another page before programming current page<br>Erase-Page/Program: page write count has exceeded the 10-year retention threshold |
| UNPROTECTPAGE | 1 | In | When asserted, the page addressed is copied into the Page Buffer and the Page Buffer is made writable. |
| WD[31:0] | 32 | In | Write data |
| WEN | 1 | In | When asserted, stores WD in the page buffer. |

All flash memory block input signals are active high, except for RESET.

*Table 2-25* • **Flash Memory Block Timing (continued)**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{SUPGLOSSPRO}$ | Page Loss Protect Setup Time for the Control Logic | 1.69 | 1.93 | 2.27 | ns |
| $t_{HDPGLOSSPRO}$ | Page Loss Protect Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUPGSTAT}$ | Page Status Setup Time for the Control Logic | 2.49 | 2.83 | 3.33 | ns |
| $t_{HDPGSTAT}$ | Page Status Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUOVERWRPG}$ | Over Write Page Setup Time for the Control Logic | 1.88 | 2.14 | 2.52 | ns |
| $t_{HDOVERWRPG}$ | Over Write Page Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{SULOCKREQUEST}$ | Lock Request Setup Time for the Control Logic | 0.87 | 0.99 | 1.16 | ns |
| $t_{HDLOCKREQUEST}$ | Lock Request Hold Time for the Control Logic | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECARNVM}$ | Reset Recovery Time | 0.94 | 1.07 | 1.25 | ns |
| $t_{REMARNVM}$ | Reset Removal Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{MPWARNVM}$ | Asynchronous Reset Minimum Pulse Width for the Control Logic | 10.00 | 12.50 | 12.50 | ns |
| $t_{MPWCLKNVM}$ | Clock Minimum Pulse Width for the Control Logic | 4.00 | 5.00 | 5.00 | ns |
| $t_{FMAXCLKNVM}$ | Maximum Frequency for Clock for the Control Logic – for AFS1500/AFS600 | 80.00 | 80.00 | 80.00 | MHz |
| | Maximum Frequency for Clock for the Control Logic – for AFS250/AFS090 | 100.00 | 80.00 | 80.00 | MHz |

## FlashROM

Fusion devices have 1 kbit of on-chip nonvolatile flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in eight banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read-back of the FlashROM from the FPGA core (Figure 2-45).

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports a synchronous read and can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank that is being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

The maximum FlashROM access clock is given in Table 2-26 on page 2-54. Figure 2-46 shows the timing behavior of the FlashROM access cycle—the address has to be set up on the rising edge of the clock for DOUT to be valid on the next falling edge of the clock.

If the address is unchanged for two cycles:

- D0 becomes invalid $t_{CK2Q}$ ns after the second rising edge of the clock.
- D0 becomes valid again $t_{CK2Q}$ ns after the second falling edge.

If the address unchanged for three cycles:

- D0 becomes invalid $t_{CK2Q}$ ns after the second rising edge of the clock.
- D0 becomes valid again $t_{CK2Q}$ ns after the second falling edge.
- D0 becomes invalid $t_{CK2Q}$ ns after the third rising edge of the clock.
- D0 becomes valid again $t_{CK2Q}$ ns after the third falling edge.

Conversely, when writing 4-bit values and reading 9-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

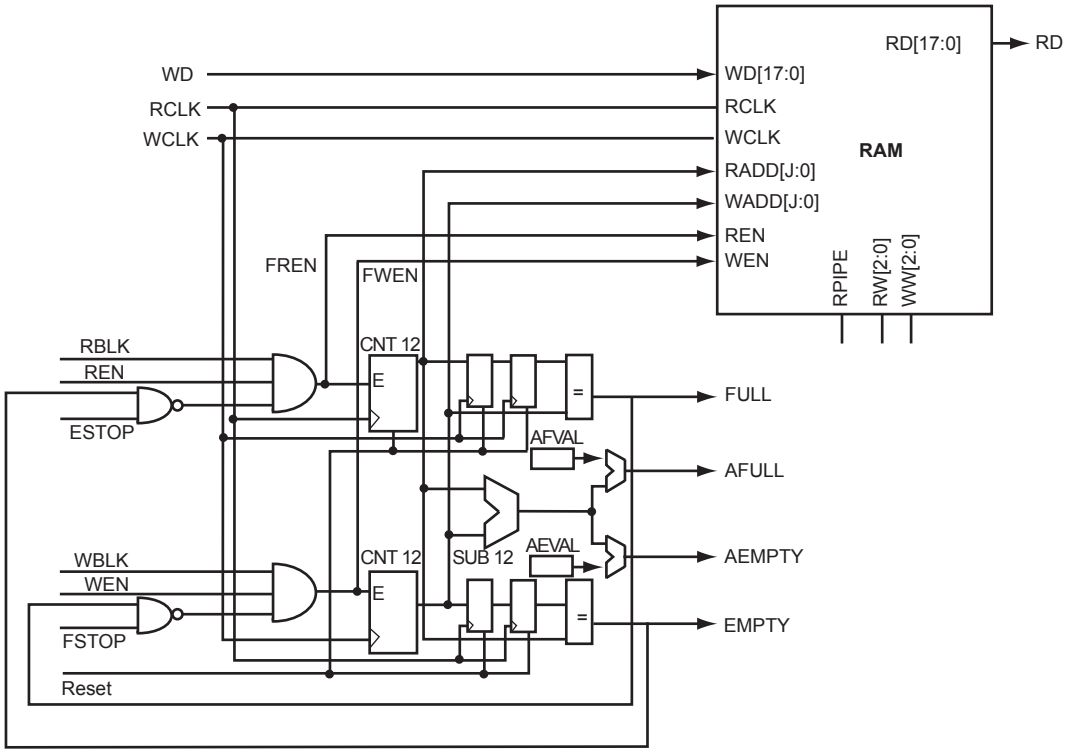


***Figure 2-47 •*** **Fusion RAM Block with Embedded FIFO Controller**

## Timing Characteristics

**Table 2-31 • RAM4K9**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.14 | 0.16 | 0.19 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| $t_{BKS}$ | BLK setup time | 0.23 | 0.27 | 0.31 | ns |
| $t_{BKH}$ | BL hold time | 0.02 | 0.02 | 0.02 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 1.79 | 2.03 | 2.39 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 2.36 | 2.68 | 3.15 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{C2CWWH}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge | 0.30 | 0.26 | 0.23 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.45 | 0.38 | 0.34 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge | 0.49 | 0.42 | 0.37 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum frequency | 310 | 272 | 231 | MHz |

*Notes:*

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### *Channel Input Offset Error*

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to ½ of LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

### *Total Channel Error*

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-68 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-68, the Total Channel Error would be a negative number.

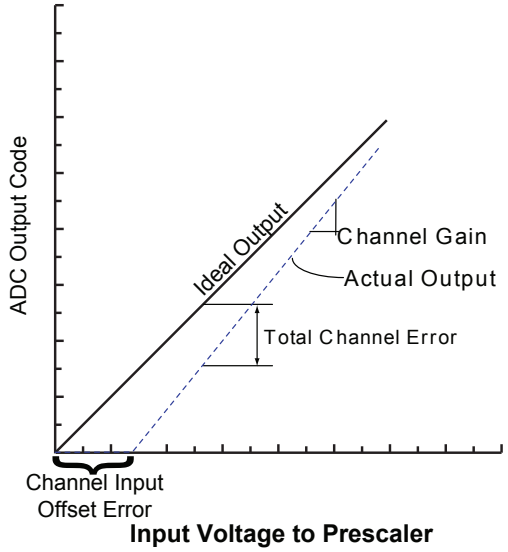


***Figure 2-68 •*** **Total Channel Error Example**

**Table 2-49 • Analog Channel Specifications (continued)**
**Commercial Temperature Range Conditions, $T_J$ = 85°C (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V**

| Parameter | Description | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Temperature Monitor Using Analog Pad AT** | | | | | | |
| External Temperature Monitor (external diode 2N3904, $T_J$ = 25°C)[4] | Resolution | 8-bit ADC | | 4 | | °C |
| | | 10-bit ADC | | 1 | | °C |
| | | 12-bit ADC | | 0.25 | | °C |
| | Systematic Offset[5] | AFS090, AFS250, AFS600, AFS1500, uncalibrated[7] | | 5 | | °C |
| | | AFS090, AFS250, AFS600, AFS1500, calibrated[7] | | ±5 | | °C |
| | Accuracy | | | ±3 | ±5 | °C |
| | External Sensor Source Current | High level, TMSTBx = 0 | | 10 | | µA |
| | | Low level, TMSTBx = 1 | | 100 | | µA |
| | Max Capacitance on AT pad | | | | 1.3 | nF |
| Internal Temperature Monitor | Resolution | 8-bit ADC | 4 | | | °C |
| | | 10-bit ADC | 1 | | | °C |
| | | 12-bit ADC | 0.25 | | | °C |
| | Systematic Offset[5] | AFS090[7] | | 5 | | °C |
| | | AFS250, AFS600, AFS1500[7] | | 11 | | °C |
| | Accuracy | | | ±3 | ±5 | °C |
| $t_{TMSHI}$ | Strobe High time | | 10 | | 105 | µs |
| $t_{TMSLO}$ | Strobe Low time | | 5 | | | µs |
| $t_{TMSSET}$ | Settling time | | 5 | | | µs |

*Notes:*

1. *VRSM is the maximum voltage drop across the current sense resistor.*
2. *Analog inputs used as digital inputs can tolerate the same voltage limits as the corresponding analog pad. There is no reliability concern on digital inputs as long as VIND does not exceed these limits.*
3. *VIND is limited to VCC33A + 0.2 to allow reaching 10 MHz input frequency.*
4. *An averaging of 1,024 samples (LPF setting in Analog System Builder) is required and the maximum capacitance allowed across the AT pins is 500 pF.*
5. *The temperature offset is a fixed positive value.*
6. *The high current mode has a maximum power limit of 20 mW. Appropriate current limit resistors must be used, based on voltage on the pad.*
7. *When using SmartGen Analog System Builder, CalibIP is required to obtain specified offset. For further details on CalibIP, refer to the "Temperature, Voltage, and Current Calibration in Fusion FPGAs" chapter of the* Fusion FPGA Fabric User Guide.

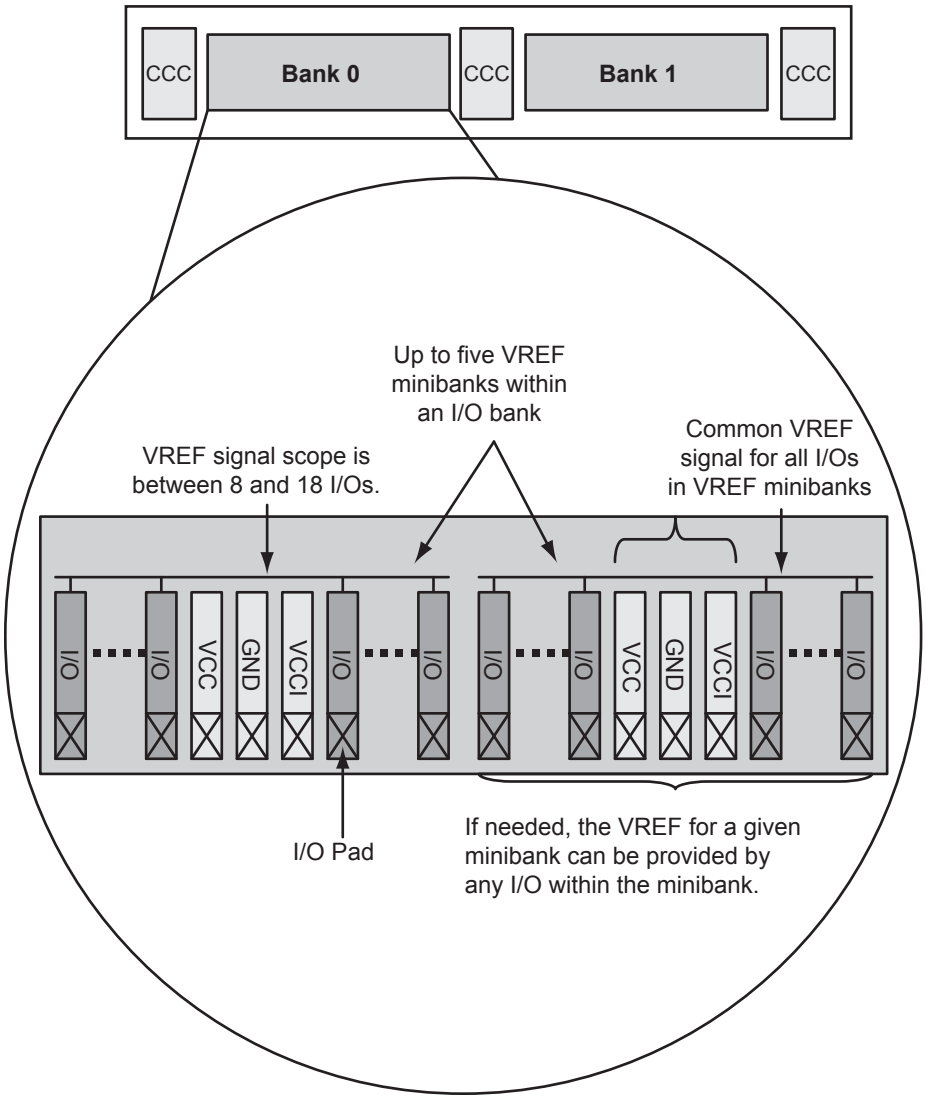


***Figure 2-99 •*** **Fusion Pro I/O Bank Detail Showing VREF Minibanks (north side ofAFS600 and AFS1500)**

***Table 2-67 •*** **I/O Standards Supported by Bank Type**

| I/O Bank | Single-Ended I/O Standards | Differential I/O Standards | Voltage-Referenced | Hot-Swap |
|---|---|---|---|---|
| Standard I/O | LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V | – | – | Yes |
| Advanced I/O | LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X | LVPECL and LVDS | – | – |
| Pro I/O | LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X | LVPECL and LVDS | GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II | Yes |

## Hot-Swap Support

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in (or from) a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-74. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required.

***Table 2-74* • Levels of Hot-Swap Support**

| Hot Swapping Level | Description | Power Applied to Device | Bus State | Card Ground Connection | Device Circuitry Connected to Bus Pins | Example of Application with Cards that Contain Fusion Devices | Compliance of Fusion Devices |
|---|---|---|---|---|---|---|---|
| 1 | Cold-swap | No | – | – | – | System and card with Microsemi FPGA chip are powered down, then card gets plugged into system, then power supplies are turned on for system but not for FPGA on card. | Compliant I/Os can but do not have to be set to hot insertion mode. |
| 2 | Hot-swap while reset | Yes | Held in reset state | Must be made and maintained for 1 ms before, during, and after insertion/removal | – | In PCI hot plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable. | Compliant I/Os can but do not have to be set to hot insertion mode. |
| 3 | Hot-swap while bus idle | Yes | Held idle (no ongoing I/O processes during insertion/removal) | Same as Level 2 | Must remain glitch-free during power-up or power-down | Board bus shared with card bus is "frozen," and there is no toggling activity on bus. It is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal. | Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode. |
| 4 | Hot-swap on an active bus | Yes | Bus may have active I/O processes ongoing, but device being inserted or removed must be idle. | Same as Level 2 | Same as Level 3 | There is activity on the system bus, and it is critical that the logic states set on the bus signal do not get disturbed during card insertion/removal. | Compliant with cards with two levels of staging. I/Os have to be set to hot insertion mode. |

## I/O Software Support

In the Fusion development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-84 and Table 2-85 list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in Fusion support up to five different drive strengths.

***Table 2-84 •*** **Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications**

| I/O Standards | SLEW (output only) | OUT_DRIVE (output only) | SKEW (all macros with OE)* | RES_PULL | OUT_LOAD (output only) | COMBINE_REGISTER |
|---|---|---|---|---|---|---|
| LVTTL/LVCMOS 3.3 V | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 2.5 V | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 2.5/5.0 V | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 1.8 V | 3 | 3 | 3 | 3 | 3 | 3 |
| LVCMOS 1.5 V | 3 | 3 | 3 | 3 | 3 | 3 |
| PCI (3.3 V) | | | 3 | | 3 | 3 |
| PCI-X (3.3 V) | 3 | | 3 | | 3 | 3 |
| LVDS, BLVDS, M-LVDS | | | 3 | | | 3 |
| LVPECL | | | | | | 3 |

*Note: * This feature does not apply to the standard I/O banks, which are the north I/O banks of AFS090 and AFS250 devices*

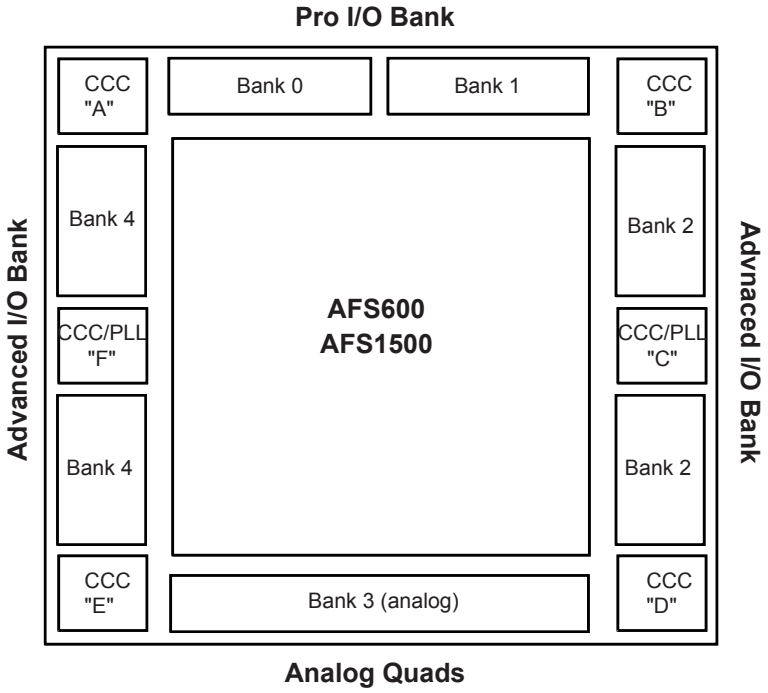


***Figure 2-114 •*** **Naming Conventions of Fusion Devices with Four I/O Banks**

**Table 2-115 • 2.5 V LVCMOS High Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Advanced I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.66 | 8.66 | 0.04 | 1.31 | 0.43 | 7.83 | 8.66 | 2.68 | 2.30 | 10.07 | 10.90 | ns |
| | –1 | 0.56 | 7.37 | 0.04 | 1.11 | 0.36 | 6.66 | 7.37 | 2.28 | 1.96 | 8.56 | 9.27 | ns |
| | –2 | 0.49 | 6.47 | 0.03 | 0.98 | 0.32 | 5.85 | 6.47 | 2.00 | 1.72 | 7.52 | 8.14 | ns |
| 8 mA | Std. | 0.66 | 5.17 | 0.04 | 1.31 | 0.43 | 5.04 | 5.17 | 3.05 | 3.00 | 7.27 | 7.40 | ns |
| | –1 | 0.56 | 4.39 | 0.04 | 1.11 | 0.36 | 4.28 | 4.39 | 2.59 | 2.55 | 6.19 | 6.30 | ns |
| | –2 | 0.49 | 3.86 | 0.03 | 0.98 | 0.32 | 3.76 | 3.86 | 2.28 | 2.24 | 5.43 | 5.53 | ns |
| 12 mA | Std. | 0.66 | 3.56 | 0.04 | 1.31 | 0.43 | 3.63 | 3.43 | 3.30 | 3.44 | 5.86 | 5.67 | ns |
| | –1 | 0.56 | 3.03 | 0.04 | 1.11 | 0.36 | 3.08 | 2.92 | 2.81 | 2.92 | 4.99 | 4.82 | ns |
| | –2 | 0.49 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |
| 16 mA | Std. | 0.66 | 3.35 | 0.04 | 1.31 | 0.43 | 3.41 | 3.06 | 3.36 | 3.55 | 5.65 | 5.30 | ns |
| | –1 | 0.56 | 2.85 | 0.04 | 1.11 | 0.36 | 2.90 | 2.60 | 2.86 | 3.02 | 4.81 | 4.51 | ns |
| | –2 | 0.49 | 2.50 | 0.03 | 0.98 | 0.32 | 2.55 | 2.29 | 2.51 | 2.65 | 4.22 | 3.96 | ns |
| 24 mA | Std. | 0.66 | 3.56 | 0.04 | 1.31 | 0.43 | 3.63 | 3.43 | 3.30 | 3.44 | 5.86 | 5.67 | ns |
| | –1 | 0.56 | 3.03 | 0.04 | 1.11 | 0.36 | 3.08 | 2.92 | 2.81 | 2.92 | 4.99 | 4.82 | ns |
| | –2 | 0.49 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**Table 2-116 • 2.5 V LVCMOS Low Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | –1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | –2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 4 mA | Std. | 0.66 | 11.00 | 0.04 | 1.29 | 0.43 | 10.37 | 11.00 | 2.03 | 1.83 | ns |
| | –1 | 0.56 | 9.35 | 0.04 | 1.10 | 0.36 | 8.83 | 9.35 | 1.73 | 1.56 | ns |
| | –2 | 0.49 | 8.21 | 0.03 | 0.96 | 0.32 | 7.75 | 8.21 | 1.52 | 1.37 | ns |
| 6 mA | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | –1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | –2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |
| 8 mA | Std. | 0.66 | 7.50 | 0.04 | 1.29 | 0.43 | 7.36 | 7.50 | 2.39 | 2.46 | ns |
| | –1 | 0.56 | 6.38 | 0.04 | 1.10 | 0.36 | 6.26 | 6.38 | 2.03 | 2.10 | ns |
| | –2 | 0.49 | 5.60 | 0.03 | 0.96 | 0.32 | 5.49 | 5.60 | 1.78 | 1.84 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**Table 2-121 • 1.8 V LVCMOS High Slew**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**
**Applicable to Pro I/Os**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 12.10 | 0.04 | 1.45 | 1.91 | 0.43 | 9.59 | 12.10 | 2.78 | 1.64 | 11.83 | 14.34 | ns |
| | –1 | 0.56 | 10.30 | 0.04 | 1.23 | 1.62 | 0.36 | 8.16 | 10.30 | 2.37 | 1.39 | 10.06 | 12.20 | ns |
| | –2 | 0.49 | 9.04 | 0.03 | 1.08 | 1.42 | 0.32 | 7.16 | 9.04 | 2.08 | 1.22 | 8.83 | 10.71 | ns |
| 4 mA | Std. | 0.66 | 7.05 | 0.04 | 1.45 | 1.91 | 0.43 | 6.20 | 7.05 | 3.25 | 2.86 | 8.44 | 9.29 | ns |
| | –1 | 0.56 | 6.00 | 0.04 | 1.23 | 1.62 | 0.36 | 5.28 | 6.00 | 2.76 | 2.44 | 7.18 | 7.90 | ns |
| | –2 | 0.49 | 5.27 | 0.03 | 1.08 | 1.42 | 0.32 | 4.63 | 5.27 | 2.43 | 2.14 | 6.30 | 6.94 | ns |
| 8 mA | Std. | 0.66 | 4.52 | 0.04 | 1.45 | 1.91 | 0.43 | 4.47 | 4.52 | 3.57 | 3.47 | 6.70 | 6.76 | ns |
| | –1 | 0.56 | 3.85 | 0.04 | 1.23 | 1.62 | 0.36 | 3.80 | 3.85 | 3.04 | 2.95 | 5.70 | 5.75 | ns |
| | –2 | 0.49 | 3.38 | 0.03 | 1.08 | 1.42 | 0.32 | 3.33 | 3.38 | 2.66 | 2.59 | 5.00 | 5.05 | ns |
| 12 mA | Std. | 0.66 | 4.12 | 0.04 | 1.45 | 1.91 | 0.43 | 4.20 | 3.99 | 3.63 | 3.62 | 6.43 | 6.23 | ns |
| | –1 | 0.56 | 3.51 | 0.04 | 1.23 | 1.62 | 0.36 | 3.57 | 3.40 | 3.09 | 3.08 | 5.47 | 5.30 | ns |
| | –2 | 0.49 | 3.08 | 0.03 | 1.08 | 1.42 | 0.32 | 3.14 | 2.98 | 2.71 | 2.71 | 4.81 | 4.65 | ns |
| 16 mA | Std. | 0.66 | 3.80 | 0.04 | 1.45 | 1.91 | 0.43 | 3.87 | 3.09 | 3.73 | 4.24 | 6.10 | 5.32 | ns |
| | –1 | 0.56 | 3.23 | 0.04 | 1.23 | 1.62 | 0.36 | 3.29 | 2.63 | 3.18 | 3.60 | 5.19 | 4.53 | ns |
| | –2 | 0.49 | 2.83 | 0.03 | 1.08 | 1.42 | 0.32 | 2.89 | 2.31 | 2.79 | 3.16 | 4.56 | 3.98 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

### Timing Characteristics

**Table 2-136 • 3.3 V PCI/PCI-X**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Pro I/Os**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.81 | 0.04 | 1.05 | 1.67 | 0.43 | 2.86 | 2.00 | 3.28 | 3.61 | 5.09 | 4.23 | ns |
| –1 | 0.56 | 2.39 | 0.04 | 0.89 | 1.42 | 0.36 | 2.43 | 1.70 | 2.79 | 3.07 | 4.33 | 3.60 | ns |
| –2 | 0.49 | 2.09 | 0.03 | 0.78 | 1.25 | 0.32 | 2.13 | 1.49 | 2.45 | 2.70 | 3.80 | 3.16 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

**Table 2-137 • 3.3 V PCI/PCI-X**
**Commercial Temperature Range Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/Os**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{PYS}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.68 | 0.04 | 0.86 | 0.43 | 2.73 | 1.95 | 3.21 | 3.58 | 4.97 | 4.19 | 0.66 | ns |
| –1 | 0.56 | 2.28 | 0.04 | 0.73 | 0.36 | 2.32 | 1.66 | 2.73 | 3.05 | 4.22 | 3.56 | 0.56 | ns |
| –2 | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | 0.49 | ns |

*Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

## Differential I/O Characteristics

Configuration of the I/O modules as a differential pair is handled by the Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with these standards.

### LVDS

Low-Voltage Differential Signal (ANSI/TIA/EIA-644) is a high-speed differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-134. The building blocks of the LVDS transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

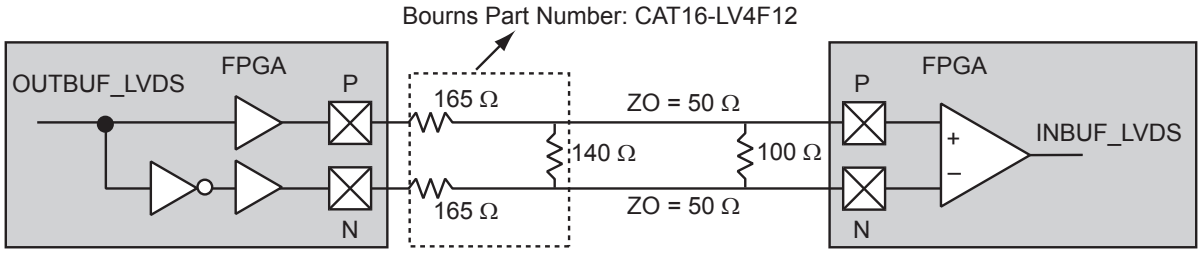


***Figure 2-134* • LVDS Circuit Diagram and Board-Level Implementation**

***Table 2-168* • Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| VCCI | Supply Voltage | 2.375 | 2.5 | 2.625 | V |
| VOL | Output Low Voltage | 0.9 | 1.075 | 1.25 | V |
| VOH | Input High Voltage | 1.25 | 1.425 | 1.6 | V |
| IOL [1] | Output Low Voltage | 0.65 | 0.91 | 1.16 | mA |
| IOH [1] | Output High Voltage | 0.65 | 0.91 | 1.16 | mA |
| VI | Input Voltage | 0 | | 2.925 | V |
| IIL [2,3] | Input Low Voltage | | | 10 | µA |
| IIH [2,4] | Input High Voltage | | | 10 | µA |
| VODIFF | Differential Output Voltage | 250 | 350 | 450 | mV |
| VOCM | Output Common Mode Voltage | 1.125 | 1.25 | 1.375 | V |
| VICM | Input Common Mode Voltage | 0.05 | 1.25 | 2.35 | V |
| VIDIFF | Input Differential Voltage | 100 | 350 | | mV |

*Notes:*

1. *IOL/IOH defined by VODIFF/(Resistor Network)*
2. *Currents are measured at 85°C junction temperature.*
3. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
4. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*

## Static Power Consumption of Various Internal Resources

***Table 3-15* • Different Components Contributing to the Static Power Consumption in Fusion Devices**

| Parameter | Definition | Power Supply | | Device-Specific Static Contributions | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | AFS1500 | AFS600 | AFS250 | AFS090 | |
| PDC1 | Core static power contribution in operating mode | VCC | 1.5 V | 18 | 7.5 | 4.50 | 3.00 | mW |
| PDC2 | Device static power contribution in standby mode | VCC33A | 3.3 V | 0.66 | | | | mW |
| PDC3 | Device static power contribution in sleep mode | VCC33A | 3.3 V | 0.03 | | | | mW |
| PDC4 | NVM static power contribution | VCC | 1.5 V | 1.19 | | | | mW |
| PDC5 | Analog Block static power contribution of ADC | VCC33A | 3.3 V | 8.25 | | | | mW |
| PDC6 | Analog Block static power contribution per Quad | VCC33A | 3.3 V | 3.3 | | | | mW |
| PDC7 | Static contribution per input pin – standard dependent contribution | VCCI | See Table 3-12 on page 3-18 | | | | | |
| PDC8 | Static contribution per input pin – standard dependent contribution | VCCI | See Table 3-13 on page 3-20 | | | | | |
| PDC9 | Static contribution for PLL | VCC | 1.5 V | 2.55 | | | | mW |

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of NVM blocks used in the design
- The number of Analog Quads used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-16 on page 3-27.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-17 on page 3-27.
- Read rate and write rate to the RAM—guidelines are provided for typical applications in Table 3-17 on page 3-27.
- Read rate to the NVM blocks

The calculation should be repeated for each clock domain defined in the design.

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| A1 | NC |
| A2 | GND |
| A3 | NC |
| A4 | NC |
| A5 | GND |
| A6 | NC |
| A7 | NC |
| A8 | GND |
| A9 | IO17NDB0V2 |
| A10 | IO17PDB0V2 |
| A11 | GND |
| A12 | IO18NDB0V2 |
| A13 | IO18PDB0V2 |
| A14 | IO20NDB0V2 |
| A15 | IO20PDB0V2 |
| A16 | GND |
| A17 | IO21PDB0V2 |
| A18 | IO21NDB0V2 |
| A19 | GND |
| A20 | IO39NDB1V2 |
| A21 | IO39PDB1V2 |
| A22 | GND |
| A23 | NC |
| A24 | NC |
| A25 | GND |
| A26 | NC |
| AA1 | NC |
| AA2 | VCCIB4 |
| AA3 | IO93PDB4V0 |
| AA4 | GND |
| AA5 | IO93NDB4V0 |
| AA6 | GEB2/IO86PDB4V0 |
| AA7 | IO86NDB4V0 |
| AA8 | AV0 |
| AA9 | GNDA |
| AA10 | AV1 |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| AA11 | AV2 |
| AA12 | GNDA |
| AA13 | AV3 |
| AA14 | AV6 |
| AA15 | GNDA |
| AA16 | AV7 |
| AA17 | AV8 |
| AA18 | GNDA |
| AA19 | AV9 |
| AA20 | VCCIB2 |
| AA21 | IO68PPB2V0 |
| AA22 | TCK |
| AA23 | GND |
| AA24 | IO76PPB2V0 |
| AA25 | VCCIB2 |
| AA26 | NC |
| AB1 | GND |
| AB2 | NC |
| AB3 | GEC2/IO87PDB4V0 |
| AB4 | IO87NDB4V0 |
| AB5 | GEA2/IO85PDB4V0 |
| AB6 | IO85NDB4V0 |
| AB7 | NCAP |
| AB8 | AC0 |
| AB9 | VCC33A |
| AB10 | AC1 |
| AB11 | AC2 |
| AB12 | VCC33A |
| AB13 | AC3 |
| AB14 | AC6 |
| AB15 | VCC33A |
| AB16 | AC7 |
| AB17 | AC8 |
| AB18 | VCC33A |
| AB19 | AC9 |
| AB20 | ADCGNDREF |

| FG676 | |
|---|---|
| Pin Number | AFS1500 Function |
| AB21 | PTBASE |
| AB22 | GNDNVM |
| AB23 | VCCNVM |
| AB24 | VPUMP |
| AB25 | NC |
| AB26 | GND |
| AC1 | NC |
| AC2 | NC |
| AC3 | NC |
| AC4 | GND |
| AC5 | VCCIB4 |
| AC6 | VCCIB4 |
| AC7 | PCAP |
| AC8 | AG0 |
| AC9 | GNDA |
| AC10 | AG1 |
| AC11 | AG2 |
| AC12 | GNDA |
| AC13 | AG3 |
| AC14 | AG6 |
| AC15 | GNDA |
| AC16 | AG7 |
| AC17 | AG8 |
| AC18 | GNDA |
| AC19 | AG9 |
| AC20 | VAREF |
| AC21 | VCCIB2 |
| AC22 | PTEM |
| AC23 | GND |
| AC24 | NC |
| AC25 | NC |
| AC26 | NC |
| AD1 | NC |
| AD2 | NC |
| AD3 | GND |
| AD4 | NC |

| Revision | Changes | Page |
|---|---|---|
| v2.0, Revision 1 (July 2009) | The MicroBlade and Fusion datasheets have been combined. Pigeon Point information is new.<br>CoreMP7 support was removed since it is no longer offered.<br>–F was removed from the datasheet since it is no longer offered.<br>The operating temperature was changed from ambient to junction to better reflect actual conditions of operations.<br>Commercial: 0°C to 85°C<br>Industrial: –40°C to 100°C<br>The version number category was changed from Preliminary to Production, which means the datasheet contains information based on final characterization. The version number changed from Preliminary v1.7 to v2.0. | N/A |
| | The "Integrated Analog Blocks and Analog I/Os" section was updated to include a reference to the "Analog System Characteristics" section in the *Device Architecture* chapter of the datasheet, which includes Table 2-46 • Analog Channel Specifications and specific voltage data. | 1-4 |
| | The phrase "Commercial-Case Conditions" in timing table titles was changed to "Commercial Temperature Range Conditions." | N/A |
| | The "Crystal Oscillator" section was updated significantly. Please review carefully. | 2-20 |
| | The "Real-Time Counter (part of AB macro)" section was updated significantly. Please review carefully. | 2-33 |
| | There was a typo in Table 2-19 • Flash Memory Block Pin Names for the ERASEPAGE description; it was the same as DISCARDPAGE. As as a result, the ERASEPAGE description was updated. | 2-40 |
| | The $t_{FMAXCLKNVM}$ parameter was updated in Table 2-25 • Flash Memory Block Timing. | 2-52 |
| | Table 2-31 • RAM4K9 and Table 2-32 • RAM512X18 were updated. | 2-66 |
| | In Table 2-36 • Analog Block Pin Description, the Function description for PWRDWN was changed from "Comparator power-down if 1"<br>to<br>"ADC comparator power-down if 1. When asserted, the ADC will stop functioning, and the digital portion of the analog block will continue operating. This may result in invalid status flags from the analog block. Therefore, Microsemi does not recommend asserting the PWRDWN pin." | 2-78 |
| | Figure 2-75 • Gate Driver Example was updated. | 2-91 |
| | The "ADC Operation" section was updated. Please review carefully. | 2-104 |
| | Figure 2-92 • Intra-Conversion Timing Diagram and Figure 2-93 • Injected Conversion Timing Diagram are new. | 2-113 |
| | The "Typical Performance Characteristics" section is new. | 2-115 |
| | Table 2-49 • Analog Channel Specifications was significantly updated. | 2-117 |
| | Table 2-50 • ADC Characteristics in Direct Input Mode was significantly updated. | 2-120 |
| | In Table 2-52 • Calibrated Analog Channel Accuracy 1,2,3, note 2 was updated. | 2-123 |
| | In Table 2-53 • Analog Channel Accuracy: Monitoring Standard Positive Voltages, note 1 was updated. | 2-124 |
| | In Table 2-54 • ACM Address Decode Table for Analog Quad, bit 89 was removed. | 2-126 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.6 (continued) | The "Analog-to-Digital Converter Block" section was updated with the following statement:<br>"All results are MSB justified in the ADC." | 2-99 |
| | The information about the ADCSTART signal was updated in the "ADC Description" section. | 2-102 |
| | Table 2-46 · Analog Channel Specifications was updated. | 2-118 |
| | Table 2-47 · ADC Characteristics in Direct Input Mode was updated. | 2-121 |
| | Table 2-51 • ACM Address Decode Table for Analog Quad was updated. | 2-127 |
| | In Table 2-53 • Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated. | 2-130 |
| | The "Introduction" section was updated to include information about digital inputs, outputs, and bibufs. | 2-133 |
| | In Table 2-69 • Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features:<br>Single-ended receiver<br>Voltage-referenced differential receiver<br>LVDS/LVPECL differential receiver features | 2-137 |
| | The "User I/O Naming Convention" section was updated to include "V" and "z" descriptions | 2-159 |
| | The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw. | 2-224 |
| | The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw. | 2-224 |
| | The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and $V_{CCI}$ pins within a given I/O bank. | 2-185 |
| | The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The "PTEM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used. | 2-228 |
| | The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090. | 3-8 |

**Microsemi Corporate Headquarters**
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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