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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Deta	ils

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	95
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/afs600-2pq208

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Temperature Grade Offerings

Fusion Devices	AFS090	AFS250	AFS600	AFS1500
ARM Cortex-M1 Devices		M1AFS250	M1AFS600	M1AFS1500
Pigeon Point Devices			P1AFS600 ³	P1AFS1500 ³
MicroBlade Devices		U1AFS250 ⁴	U1AFS600 ⁴	U1AFS1500 ⁴
QN108 ⁵	C, I	-	-	_
QN180 ⁵	C, I	C, I	-	-
PQ208	-	C, I	C, I	-
FG256	C, I	C, I	C, I	C, I
FG484	-	-	C, I	C, I
FG676	-	-	-	C, I

Notes:

1. C = Commercial Temperature Range: 0°C to 85°C Junction

2. I = Industrial Temperature Range: -40°C to 100°C Junction

3. Pigeon Point devices are only offered in FG484 and FG256.

4. MicroBlade devices are only offered in FG256.

5. Package not available.

Speed Grade and Temperature Grade Matrix

	Std. ¹	-1	-2 ²
C ³	\checkmark	\checkmark	\checkmark
l ⁴	\checkmark	\checkmark	\checkmark

Notes:

1. MicroBlade devices are only offered in standard speed grade.

2. Pigeon Point devices are only offered in –2 speed grade.

3. C = Commercial Temperature Range: 0°C to 85°C Junction

4. I = Industrial Temperature Range: -40°C to 100°C Junction

Contact your local Microsemi SoC Products Group representative for device availability:

http://www.microsemi.com/index.php?option=com_content&id=137&lang=en&view=article.

Cortex-M1, Pigeon Point, and MicroBlade Fusion Device Information

This datasheet provides information for all Fusion (AFS), Cortex-M1 (M1), Pigeon Point (P1), and MicroBlade (U1) devices. The remainder of the document will only list the Fusion (AFS) devices. Please apply relevant information to M1, P1, and U1 devices when appropriate. Please note the following:

- Cortex-M1 devices are offered in the same speed grades and packages as basic Fusion devices.
- Pigeon Point devices are only offered in –2 speed grade and FG484 and FG256 packages.
- MicroBlade devices are only offered in standard speed grade and the FG256 package.



Fusion Device Family Overview

With Fusion, Microsemi also introduces the Analog Quad I/O structure (Figure 1-1). Each quad consists of three analog inputs and one gate driver. Each quad can be configured in various built-in circuit combinations, such as three prescaler circuits, three digital input circuits, a current monitor circuit, or a temperature monitor circuit. Each prescaler has multiple scaling factors programmed by FPGA signals to support a large range of analog inputs with positive or negative polarity. When the current monitor circuit is selected, two adjacent analog inputs measure the voltage drop across a small external sense resistor. For more information, refer to the "Analog System Characteristics" section on page 2-117. Built-in operational amplifiers amplify small voltage signals for accurate current measurement. One analog input in each quad can be connected to an external temperature monitor diode. In addition to the external temperature monitor diode(s), a Fusion device can monitor an internal temperature diode using dedicated channel 31 of the ADCMUX.

Figure 1-1 on page 1-5 illustrates a typical use of the Analog Quad I/O structure. The Analog Quad shown is configured to monitor and control an external power supply. The AV pad measures the source of the power supply. The AC pad measures the voltage drop across an external sense resistor to calculate current. The AG MOSFET gate driver pad turns the external MOSFET on and off. The AT pad measures the load-side voltage level.



Figure 1-1 • Analog Quad

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Fusion technology stack, the application can be easily created in FPGA gates by importing and configuring multiple applets.

In fact, in some cases an entire FPGA system design can be created without any HDL coding.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Core Architecture

VersaTile

Based upon successful ProASIC3/E logic architecture, Fusion devices provide granularity comparable to gate arrays. The Fusion device core consists of a sea-of-VersaTiles architecture.

As illustrated in Figure 2-2, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- · D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, the SET/CLR signal is supported by a fourth input, which can only be routed to the core cell over the VersaNet (global) network.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources (Figure 2-2).



Note: *This input can only be connected to the global clock distribution network.

Figure 2-2 • Fusion Core VersaTile

Example: Calculation for Match Count

To put the Fusion device on standby for one hour using an external crystal of 32.768 KHz: The period of the crystal oscillator is $T_{crystal}$:

T_{crystal} = 1 / 32.768 KHz = 30.518 µs

The period of the counter is T_{counter}:

T_{counter} = 30.518 us X 128 = 3.90625 ms

The Match Count for 1 hour is Δ tmatch:

 Δ tmatch / T_{counter} = (1 hr X 60 min/hr X 60 sec/min) / 3.90625 ms = 921600 or 0xE1000

Using a 32.768 KHz crystal, the maximum standby time of the 40-bit counter is 4,294,967,296 seconds, which is 136 years.

Table 2-15 • Memory Map for RTC in ACM Register and Description

ACMADDR	Register Name	Description	Use	Default Value
0x40	COUNTER0	Counter bits 7:0	Used to preload the counter to a specified start point.	0x00
0x41	COUNTER1	Counter bits 15:8		0x00
0x42	COUNTER2	Counter bits 23:16		0x00
0x43	COUNTER3	Counter bits 31:24		0x00
0x44	COUNTER4	Counter bits 39:32		0x00
0x48	MATCHREG0	Match register bits 7:0	The RTC comparison bits	0x00
0x49	MATCHREG1	Match register bits 15:8		0x00
0x4A	MATCHREG2	Match register bits 23:16		0x00
0x4B	MATCHREG3	Match register bits 31:24		0x00
0x4C	MATCHREG4	Match register bits 39:32		0x00
0x50	MATCHBIT0	Individual match bits 7:0	The output of the XNOR gates 0 – Not matched 1 – Matched	0x00
0x51	MATCHBIT1	Individual match bits 15:8		0x00
0x52	MATCHBIT2	Individual match bits 23:16		0x00
0x53	MATCHBIT3	Individual match bits 31:24		0x00
0x54	MATCHBIT4	Individual match bits 29:32		0x00
0x58	CTRL_STAT	Control (write/read) / Status (read only) register bits	Refer to Table 2-16 on page 2-35 for details.	0x00



The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries and the AEVAL setting is based on the number of software and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16, instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios are specified, the FIFO will assert FULL or EMPTY as soon as at least a minimum of one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

Channel Input Offset Error

Channel Offset error is measured as the input voltage that causes the transition from zero to a count of one. An Ideal Prescaler will have offset equal to $\frac{1}{2}$ of LSB voltage. Offset error is a positive or negative when the first transition point is higher or lower than ideal. Offset error is expressed in LSB or input voltage.

Total Channel Error

Total Channel Error is defined as the total error measured compared to the ideal value. Total Channel Error is the sum of gain error and offset error combined. Figure 2-68 shows how Total Channel Error is measured.

Total Channel Error is defined as the difference between the actual ADC output and ideal ADC output. In the example shown in Figure 2-68, the Total Channel Error would be a negative number.



Figure 2-68 • Total Channel Error Example



Refer to Table 2-46 on page 2-109 and the "Acquisition Time or Sample Time Control" section on page 2-107

$$t_{sample} = (2 + STC) \times t_{ADCCLK}$$

EQ 20

STC: Sample Time Control value (0–255)

t_{SAMPLE} is the sample time

Table 2-46 • STC Bits Function

Name	Bits	Function
STC	[7:0]	Sample time control

Sample time is computed based on the period of ADCCLK.

Distribution Phase

The second phase is called the distribution phase. During distribution phase, the ADC computes the equivalent digital value from the value stored in the input capacitor. In this phase, the output signal SAMPLE goes back to '0', indicating the sample is completed; but the BUSY signal remains '1', indicating the ADC is still busy for distribution. The distribution time depends strictly on the number of bits. If the ADC is configured as a 10-bit ADC, then 10 ADCCLK cycles are needed. EQ 8 describes the distribution time.

$$t_{distrib} = N \times t_{ADCCLK}$$

EQ 21

N: Number of bits

Post-Calibration Phase

The last phase is the post-calibration phase. This is an optional phase. The post-calibration phase takes two ADCCLK cycles. The output BUSY signal will remain '1' until the post-calibration phase is completed. If the post-calibration phase is skipped, then the BUSY signal goes to '0' after distribution phase. As soon as BUSY signal goes to '0', the DATAVALID signal goes to '1', indicating the digital result is available on the RESULT output signals. DATAVAILD will remain '1' until the next ADCSTART is asserted. Microsemi recommends enabling post-calibration to compensate for drift and temperature-dependent effects. This ensures that the ADC remains consistent over time and with temperature. The post-calibration phase is enabled by bit 3 of the Mode register. EQ 9 describes the post-calibration time.

$$t_{post-cal} = MODE[3] \times (2 \times t_{ADCCLK})$$

EQ 22

EQ 23

MODE[3]: Bit 3 of the Mode register, described in Table 2-41 on page 2-106.

The calculation for the conversion time for the ADC is summarized in EQ 23.

 $t_{conv} = t_{sync_read} + t_{sample} + t_{distrib} + t_{post-cal} + t_{sync_write}$

t_{conv}: conversion time

 t_{sync_read} : maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK} .

t_{sample}: Sample time

t_{distrib}: Distribution time

tpost-cal: Post-calibration time

 t_{sync_write} : Maximum time for a signal to synchronize with SYSCLK. For calculation purposes, the worst case is a period of SYSCLK, t_{SYSCLK} .



Table 2-50 • ADC Characteristics in Direct Input Mode (continued)

Commercial Temperature Range Conditions, $T_J = 85^{\circ}C$ (unless noted otherwise), Typical: VCC33A = 3.3 V, VCC = 1.5 V

Parameter	Description	Condition	Min.	Тур.	Max.	Units
Dynamic Pe	erformance					
SNR	Signal-to-Noise Ratio	8-bit mode	48.0	49.5		dB
		10-bit mode	58.0	60.0		dB
		12-bit mode	62.9	64.5		dB
SINAD	Signal-to-Noise Distortion	8-bit mode	47.6	49.5		dB
		10-bit mode	57.4	59.8		dB
		12-bit mode	62.0	64.2		dB
THD	Total Harmonic Distortion	8-bit mode		-74.4	-63.0	dBc
		10-bit mode		-78.3	-63.0	dBc
		12-bit mode		-77.9	-64.4	dBc
ENOB	Effective Number of Bits	8-bit mode	7.6	7.9		bits
		10-bit mode	9.5	9.6		bits
		12-bit mode	10.0	10.4		bits
Conversion	Rate	ŀ				
	Conversion Time	8-bit mode	1.7			μs
		10-bit mode	1.8			μs
		12-bit mode	2			μs
	Sample Rate	8-bit mode			600	Ksps
		10-bit mode			550	Ksps
		12-bit mode			500	Ksps

Notes:

1. Accuracy of the external reference is 2.56 V \pm 4.6 mV.

2. Data is based on characterization.

3. The sample rate is time-shared among active analog inputs.



Similarly,

Min. Output Voltage = (Max. Negative input offset) + (Input Voltage x Max. Negative Channel Gain) = $(-88 \text{ mV}) + (5 \text{ V} \times 0.96) = 4.712 \text{ V}$

Calculating Accuracy for a Calibrated Analog Channel

Formula

For a given prescaler range, EQ 31 gives the output voltage.

Output Voltage = Channel Error in V + Input Voltage

EQ 31

where

Channel Error in V = Total Channel Error in LSBs x Equivalent voltage per LSB

Example

Input Voltage = 5 VChosen Prescaler range = 8 V range Refer to Table 2-52 on page 2-123.

Max. Output Voltage = Max. Positive Channel Error in V + Input Voltage Max. Positive Channel Error in V = (6 LSB) × (8 mV per LSB in 10-bit mode) = 48 mV Max. Output Voltage = 48 mV + 5 V = **5.048 V**

Similarly,

Min. Output Voltage = Max. Negative Channel Error in V + Input Voltage = (-48 mV) + 5 V = 4.952 V

Calculating LSBs from a Given Error Budget

Formula

For a given prescaler range, LSB count = ± (Input Voltage × Required % error) / (Equivalent voltage per LSB)

Example

Input Voltage = $3.3 \vee$ Required error margin= 1% Refer to Table 2-52 on page 2-123. Equivalent voltage per LSB = 16 mV for a 16V prescaler, with ADC in 10-bit mode LSB Count = $\pm (5.0 \vee \times 1\%) / (0.016)$ LSB Count = ± 3.125 Equivalent voltage per LSB = 8 mV for an $8 \vee$ prescaler, with ADC in 10-bit mode LSB Count = $\pm (5.0 \vee \times 1\%) / (0.008)$ LSB Count = $\pm (5.0 \vee \times 1\%) / (0.008)$ LSB Count = ± 6.25 The $8 \vee$ prescaler satisfies the calculated LSB count accuracy requirement (see Table 2-52 on page 2-123).



Table 2-96 • I/O Output Buffer Maximum Resistances ¹ (continued)

Standard	Drive Strength	R _{PULL-DOWN} (ohms) ²	R _{PULL-UP} (ohms) ³								
Applicable to Standard I/O Banks											
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300								
	4 mA	100	300								
	6 mA	50	150								
	8 mA	50	150								
2.5 V LVCMOS	2 mA	100	200								
	4 mA	100	200								
	6 mA	50	100								
	8 mA	50	100								
1.8 V LVCMOS	2 mA	200	225								
	4 mA	100	112								
1.5 V LVCMOS	2 mA	200	224								

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.

2. R_(PULL-DOWN-MAX) = VOLspec / I_{OLspec}

3. R_(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec

Table 2-97 • I/O Weak Pull-Up/Pull-Down Resistances Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	R _{(WEAK I} (oh	PULL-UP) ms)	R _(WEAK PULL-DOWN) ² (ohms)		
VCCI	Min.	Max.	Min.	Max.	
3.3 V	10 k	45 k	10 k	45 k	
2.5 V	11 k	55 k	12 k	74 k	
1.8 V	18 k	70 k	17 k	110 k	
1.5 V	19 k	90 k	19 k	140 k	

Notes:

R_(WEAK PULL-UP-MAX) = (VCCImax – VOHspec) / I_{WEAK PULL-UP-MIN}
R_(WEAK PULL-DOWN-MAX) = VOLspec / I_{WEAK PULL-DOWN-MIN}



Table 2-105 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/Os

Drive	Speed						^τ ΕΟU							11
Strength	Grade	TDOUT	τ _{DP}	τ _{DIN}	τ _{ΡΥ}	τ _{PYS}	Т	۲ZL	τzΗ	ιLZ	τ _{HZ}	τ _{ZLS}	τ _{zhs}	Units
4 mA	Std.	0.66	7.88	0.04	1.20	1.57	0.43	8.03	6.70	2.69	2.59	10.26	8.94	ns
	-1	0.56	6.71	0.04	1.02	1.33	0.36	6.83	5.70	2.29	2.20	8.73	7.60	ns
	-2	0.49	5.89	0.03	0.90	1.17	0.32	6.00	5.01	2.01	1.93	7.67	6.67	ns
8 mA	Std.	0.66	5.08	0.04	1.20	1.57	0.43	5.17	4.14	3.05	3.21	7.41	6.38	ns
	-1	0.56	4.32	0.04	1.02	1.33	0.36	4.40	3.52	2.59	2.73	6.30	5.43	ns
	-2	0.49	3.79	0.03	0.90	1.17	0.32	3.86	3.09	2.28	2.40	5.53	4.76	ns
12 mA	Std.	0.66	3.67	0.04	1.20	1.57	0.43	3.74	2.87	3.28	3.61	5.97	5.11	ns
	-1	0.56	3.12	0.04	1.02	1.33	0.36	3.18	2.44	2.79	3.07	5.08	4.34	ns
	-2	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
16 mA	Std.	0.66	3.46	0.04	1.20	1.57	0.43	3.53	2.61	3.33	3.72	5.76	4.84	ns
	-1	0.56	2.95	0.04	1.02	1.33	0.36	3.00	2.22	2.83	3.17	4.90	4.12	ns
	-2	0.49	2.59	0.03	0.90	1.17	0.32	2.63	1.95	2.49	2.78	4.30	3.62	ns
24 mA	Std.	0.66	3.21	0.04	1.20	1.57	0.43	3.27	2.16	3.39	4.13	5.50	4.39	ns
	-1	0.56	2.73	0.04	1.02	1.33	0.36	2.78	1.83	2.88	3.51	4.68	3.74	ns
	-2	0.49	2.39	0.03	0.90	1.17	0.32	2.44	1.61	2.53	3.08	4.11	3.28	ns



3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-144 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+	· VIL		VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
35 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	-	35	35	181	268	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-126 • AC Loading

Table	2-145	AC Wavef	orms. Meas	suring Poin	ts, and Ca	pacitive Loads
i ubic	2-140		ormo, mous	ournig i oni	its, and ou	

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-146 • 3.3 V GTL+

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
-1	0.56	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
-2	0.49	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

SSTL3 Class II

Stub-Speed Terminated Logic for 3.3 V memory bus standard (JESD8-8). Fusion devices support Class II. This provides a differential amplifier input buffer and a push-pull output buffer.

SSTL3 Class II		VIL	VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
21 mA	-0.3	VREF – 0.2	VREF + 0.2	3.6	0.5	VCCI – 0.9	21	21	109	103	10	10

Table 2-165 • Minimum and Maximum DC Input and Output Levels

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-133 • AC Loading

Table 2-166 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.5	1.5	1.485	30

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-167 • SSTL3- Class II Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.5 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.07	0.04	1.25	0.43	2.10	1.67			4.34	3.91	ns
-1	0.56	1.76	0.04	1.06	0.36	1.79	1.42			3.69	3.32	ns
-2	0.49	1.54	0.03	0.93	0.32	1.57	1.25			3.24	2.92	ns



LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-136. The building blocks of the LVPECL transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.



EINURA 2 426 . IVDECI	Circuit Disarom and Deard La	
FIGHTE Z=1.30 • 1 VPFL.1	CITCUU DIAOFAM AND BOAFO-LE	vei impiementation
1 IYUIC 2-130 ° LVFLOL	Circuit Diagram and Doard-Le	

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3	3.3		3.6	
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-171 • Minimum and Maximum DC Input and Output Levels

Table 2-172 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	
1.64	1.94	Cross point	_	

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-173 • LVPECL

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/Os

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	Units
Std.	0.66	2.14	0.04	1.63	ns
-1	0.56	1.82	0.04	1.39	ns
-2	0.49	1.60	0.03	1.22	ns

ATRTNx Temperature Monitor Return

AT returns are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is one analog return pin for every two Analog Quads. The x in the ATRTNx designator indicates the quad pairing (x = 0 for AQ1 and AQ2, x = 1 for AQ2 and AQ3, ..., x = 4 for AQ8 and AQ9). The signals that drive these pins are called out as ATRETURNxy in the software (where x and y refer to the quads that share the return signal). ATRTN is internally connected to ground. It can be left floating when it is unused. The maximum capacitance allowed across the AT pins is 500 pF.

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-22.

Refer to the "User I/O Naming Convention" section on page 2-158 for a description of naming of global pins.

JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device.

Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pullup/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to Table 2-183 for more information.

VJTAG	Tie-Off Resistance ^{2, 3}
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Table 2-183 • Recommended Tie-Off Values for the TCK and TRST Pins

Notes:

- 1. Equivalent parallel resistance if more than one device is on JTAG chain.
- 2. The TCK pin can be pulled up/down.
- 3. The TRST pin can only be pulled down.

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.



Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{\mathsf{J}\mathsf{A}} = \frac{\mathsf{T}_{\mathsf{J}} - \theta_{\mathsf{A}}}{\mathsf{P}}$$

EQ 1

$$\theta_{\mathsf{JB}} = \frac{\mathsf{T}_{\mathsf{J}} - \mathsf{T}_{\mathsf{B}}}{\mathsf{P}}$$

EQ 2

EQ 3

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

where

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JB} = Junction-to-board thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 3-6 • Package Thermal Resistance

		Θ_{JA}				
Product	Still Air	1.0 m/s	2.5 m/s	θ JC	θ_{JB}	Units
AFS090-QN108	34.5	30.0	27.7	8.1	16.7	°C/W
AFS090-QN180	33.3	27.6	25.7	9.2	21.2	°C/W
AFS250-QN180	32.2	26.5	24.7	5.7	15.0	°C/W
AFS250-PQ208	42.1	38.4	37	20.5	36.3	°C/W
AFS600-PQ208	23.9	21.3	20.48	6.1	16.5	°C/W
AFS090-FG256	37.7	33.9	32.2	11.5	29.7	°C/W
AFS250-FG256	33.7	30.0	28.3	9.3	24.8	°C/W
AFS600-FG256	28.9	25.2	23.5	6.8	19.9	°C/W
AFS1500-FG256	23.3	19.6	18.0	4.3	14.2	°C/W
AFS600-FG484	21.8	18.2	16.7	7.7	16.8	°C/W
AFS1500-FG484	21.6	16.8	15.2	5.6	14.9	°C/W
AFS1500-FG676	TBD	TBD	TBD	TBD	TBD	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the AFS600-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

Maximum Power Allowed =
$$\frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

 θ_{JA} = 19.00°C/W (taken from Table 3-6 on page 3-7).

 $T_A = 75.00^{\circ}C$

Maximum Power Allowed =
$$\frac{100.00^{\circ}C - 75.00^{\circ}C}{19.00^{\circ}C/W} = 1.3 W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an AFS600-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

 $T_{J} = 100.00^{\circ}C$

 $T_A = 70.00^{\circ}C$

From the datasheet:

 $\theta_{JA} = 17.00^{\circ}C/W$ $\theta_{JC} = 8.28^{\circ}C/W$

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100^{\circ}C - 70^{\circ}C}{17.00 \text{ W}} = 1.76 \text{ W}$$

EQ 6

PLL/CCC Contribution—P_{PLL}

PLL is not used in this application.

 $P_{PLL} = 0 W$

Nonvolatile Memory—P_{NVM}

Nonvolatile memory is not used in this application.

 $P_{NVM} = 0 W$

Crystal Oscillator—P_{XTL-OSC}

The application utilizes standby mode. The crystal oscillator is assumed to be active.

Operating Mode

P_{XTL-OSC} = PAC18

 $P_{XTL-OSC} = 0.63 \text{ mW}$

Standby Mode

P_{XTL-OSC} = PAC18

P_{XTL-OSC} = 0.63 mW

Sleep Mode

 $P_{XTL-OSC} = 0 W$

RC Oscillator—P_{RC-OSC}

Operating Mode

P_{RC-OSC} = PAC19

 $P_{RC-OSC} = 3.30 \text{ mW}$

Standby Mode and Sleep Mode

 $P_{RC-OSC} = 0 W$

Analog System—P_{AB}

Number of Quads used: N_{QUADS} = 4

Operating Mode

P_{AB} = PAC20

 P_{AB} = 3.00 mW

Standby Mode and Sleep Mode

 $P_{AB} = 0 W$

Total Dynamic Power Consumption—P_{DYN}

Operating Mode

P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{NVM}+ P_{XTL-OSC} + P_{RC-OSC} + P_{AB} P_{DYN} = 41.28 mW + 21.1 mW + 4.35 mW + 19.25 mW + 1.30 mW + 47.47 mW + 1.38 mW + 0 + 0 + 0 + 0.63 mW + 3.30 mW + 3.00 mW

P_{DYN} = 143.06 mW

Standby Mode

 $P_{DYN} = P_{XTL-OSC}$ $P_{DYN} = 0.63 \text{ mW}$

Sleep Mode

 $P_{DYN} = 0 W$



FG676



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.

Microsemi -Fusion Family of Mixed Signal FPGAs

	FG676		FG676
Pin Number	AFS1500 Function	Pin Number	AFS1500 Function
AD5	IO94NPB4V0	AE15	GNDA
AD6	GND	AE16	NC
AD7	VCC33N	AE17	NC
AD8	AT0	AE18	GNDA
AD9	ATRTN0	AE19	NC
AD10	AT1	AE20	NC
AD11	AT2	AE21	NC
AD12	ATRTN1	AE22	NC
AD13	AT3	AE23	NC
AD14	AT6	AE24	NC
AD15	ATRTN3	AE25	GND
AD16	AT7	AE26	GND
AD17	AT8	AF1	NC
AD18	ATRTN4	AF2	GND
AD19	AT9	AF3	NC
AD20	VCC33A	AF4	NC
AD21	GND	AF5	NC
AD22	IO76NPB2V0	AF6	NC
AD23	NC	AF7	NC
AD24	GND	AF8	NC
AD25	NC	AF9	VCC33A
AD26	NC	AF10	NC
AE1	GND	AF11	NC
AE2	GND	AF12	VCC33A
AE3	NC	AF13	NC
AE4	NC	AF14	NC
AE5	NC	AF15	VCC33A
AE6	NC	AF16	NC
AE7	NC	AF17	NC
AE8	NC	AF18	VCC33A
AE9	GNDA	AF19	NC
AE10	NC	AF20	NC
AE11	NC	AF21	NC
AE12	GNDA	AF22	NC
AE13	NC	AF23	NC
AE14	NC	AF24	NC

FG676	
Pin Number	AFS1500 Function
AF25	GND
AF26	NC
B1	GND
B2	GND
B3	NC
B4	NC
B5	NC
B6	VCCIB0
B7	NC
B8	NC
B9	VCCIB0
B10	IO15NDB0V2
B11	IO15PDB0V2
B12	VCCIB0
B13	IO19NDB0V2
B14	IO19PDB0V2
B15	VCCIB1
B16	IO25NDB1V0
B17	IO25PDB1V0
B18	VCCIB1
B19	IO33NDB1V1
B20	IO33PDB1V1
B21	VCCIB1
B22	NC
B23	NC
B24	NC
B25	GND
B26	GND
C1	NC
C2	NC
C3	GND
C4	NC
C5	GAA1/IO01PDB0V0
C6	GAB0/IO02NDB0V0
C7	GAB1/IO02PDB0V0
C8	IO07NDB0V1