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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	95
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/afs600-2pq208i

The on-chip crystal and RC oscillators work in conjunction with the integrated phase-locked loops (PLLs) to provide clocking support to the FPGA array and on-chip resources. In addition to supporting typical RTC uses such as watchdog timer, the Fusion RTC can control the on-chip voltage regulator to power down the device (FPGA fabric, flash memory block, and ADC), enabling a low power standby mode.

The Fusion family offers revolutionary features, never before available in an FPGA. The nonvolatile flash technology gives the Fusion solution the advantage of being a highly secure, low power, single-chip solution that is Instant On. Fusion is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based Fusion devices are Instant On and do not need to be loaded from an external boot PROM.
On-board security mechanisms prevent access to the programming information and enable remote updates of the FPGA logic that are protected with high level security. Designers can perform remote in-system reprogramming to support future design iterations and field upgrades, with confidence that valuable IP is highly unlikely to be compromised or copied. ISP can be performed using the
industry-standard AES algorithm with MAC data authentication on the device. The Fusion family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the Fusion family a cost-effective ASIC replacement solution for applications in the consumer, networking and communications, computing, and avionics markets.

Security

As the nonvolatile, flash-based Fusion family requires no boot PROM, there is no vulnerable external bitstream. Fusion devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Fusion devices utilize a 128-bit flash-based key lock and a separate AES key to provide the highest level of protection in the FPGA industry for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the industry-leading AES-128 block cipher encryption standard (FIPS Publication 192). The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the DES standard, which was adopted in 1977. Fusion devices have a
built-in AES decryption engine and a flash-based AES key that make Fusion devices the most comprehensive programmable logic device security solution available today. Fusion devices with
AES-based security provide a high level of protection for remote field updates over public networks, such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the Fusion family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. Fusion with FlashLock and AES security is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with
industry-standard security, making remote ISP possible. A Fusion device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Fusion FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Advanced Architecture

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 1-1 on page 1-5):

- Embedded memories
  - Flash memory blocks
  - FlashROM
  - SRAM and FIFO
- Clocking resources
  - PLL and CCC
  - RC oscillator
  - Crystal oscillator
  - No-Glitch MUX (NGMUX)
- Digital I/Os with advanced I/O standards
- FPGA VersaTiles
- Analog components
  - ADC
  - Analog I/Os supporting voltage, current, and temperature monitoring
  - 1.5 V on-board voltage regulator
  - Real-time counter

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic lookup table (LUT) equivalent or a D-flip-flop or latch (with or without enable) by programming the appropriate flash switch interconnections. This versatility allows efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi families of flash-based FPGAs. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid (3.3 V) single-voltage programming of Fusion devices via an IEEE 1532 JTAG interface.

Unprecedented Integration

Integrated Analog Blocks and Analog I/Os

Fusion devices offer robust and flexible analog mixed signal capability in addition to the high-performance flash FPGA fabric and flash memory block. The many built-in analog peripherals include a configurable 32:1 input analog MUX, up to 10 independent MOSFET gate driver outputs, and a configurable ADC. The ADC supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (Ksps), differential nonlinearity (DNL) < 1.0 LSB, and Total Unadjusted Error (TUE) of 0.72 LSB in 10-bit mode. The TUE is used for characterization of the conversion error and includes errors from all sources, such as offset and linearity. Internal bandgap circuitry offers 1% voltage reference accuracy with the flexibility of utilizing an external reference voltage. The ADC channel sampling sequence and sampling rate are programmable and implemented in the FPGA logic using Designer and Libero SoC software tool support.

Two channels of the 32-channel ADCMUX are dedicated. Channel 0 is connected internally to VCC and can be used to monitor core power supply. Channel 31 is connected to an internal temperature diode which can be used to monitor device temperature. The 30 remaining channels can be connected to external analog signals. The exact number of I/Os available for external connection signals is device-dependent (refer to the "Fusion Family" table on page I for details).

VersaNet Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are dependent upon I/O standard, and the clock may be driven and conditioned internally by the CCC module. Table 2-5, Table 2-6, Table 2-7, and Table 2-8 on page 2-17 present minimum and maximum global clock delays within the device Minimum and maximum delays are measured with minimum and maximum loading, respectively.

Timing Characteristics

Table 2-5 • AFS1500 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.53	1.75	1.74	1.99	2.05	2.34	ns
t_{RCKH}	Input High Delay for Global Clock	1.53	1.79	1.75	2.04	2.05	2.40	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

Table 2-6 • AFS600 Global Resource Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.27	1.49	1.44	1.70	1.69	2.00	ns
t_{RCKH}	Input High Delay for Global Clock	1.26	1.54	1.44	1.75	1.69	2.06	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock							ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock							ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27		0.31		0.36	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.*

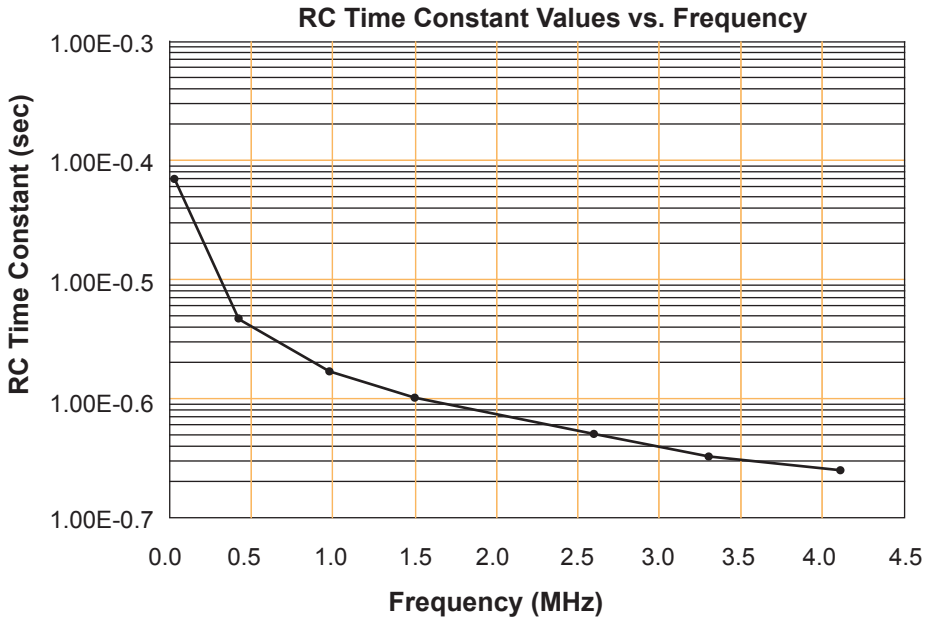

Figure 2-18 • **Crystal Oscillator: RC Time Constant Values vs. Frequency (typical)**

Table 2-10 • **XTLOSC Signals Descriptions**

Signal Name	Width	Direction	Function		
XTL_EN*	1		Enables the crystal. Active high.		
XTL_MODE*	2		Settings for the crystal clock for different frequency.		
			Value	**Modes**	**Frequency Range**
			b'00	RC network	32 KHz to 4 MHz
			b'01	Low gain	32 to 200 KHz
			b'10	Medium gain	0.20 to 2.0 MHz
			b'11	High gain	2.0 to 20.0 MHz
SELMODE	1	IN	Selects the source of XTL_MODE and also enables the XTL_EN. Connect from RTCXTLSEL from AB.		
			0	For normal operation or sleep mode, XTL_EN depends on FPGA_EN, XTL_MODE depends on MODE	
			1	For Standby mode, XTL_EN is enabled, XTL_MODE depends on RTC_MODE	
RTC_MODE[1:0]	2	IN	Settings for the crystal clock for different frequency ranges. XTL_MODE uses RTC_MODE when SELMODE is '1'.		
MODE[1:0]	2	IN	Settings for the crystal clock for different frequency ranges. XTL_MODE uses MODE when SELMODE is '0'. In Standby, MODE inputs will be 0's.		
FPGA_EN*	1	IN	0 when 1.5 V is not present for VCC 1 when 1.5 V is present for VCC		
XTL	1	IN	Crystal Clock source		
CLKOUT	1	OUT	Crystal Clock output		

*Note: *Internal signal—does not exist in macro.*

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS macros are composite macros that include an I/O macro driving a global buffer, hardwired together (Figure 2-20).

The CLKINT macro provides a global buffer function driven by the FPGA core.

The CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by Fusion devices. The available CLKBUF macros are described in the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide*.

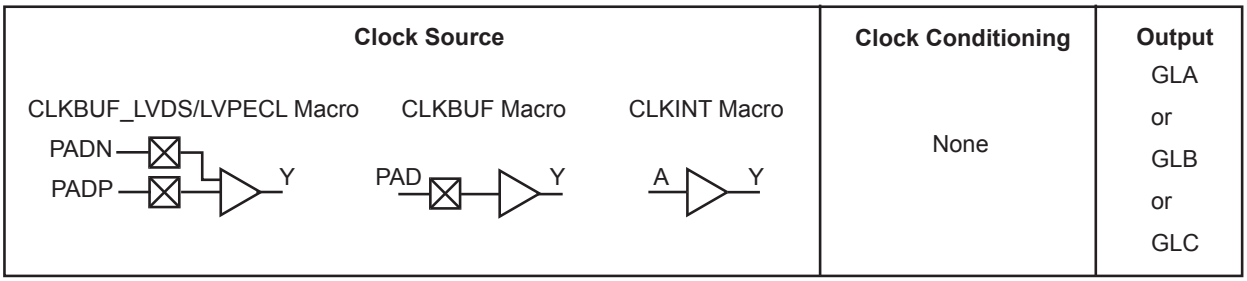

Figure 2-20 • **Global Buffers with No Programmable Delay**

Global Buffers with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay (Figure 2-21 on page 2-25). The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the Fusion family. The available INBUF macros are described in the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide.*

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero SoC and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

Erase Page Operation

The Erase Page operation is initiated when the ERASEPAGE pin is asserted. The Erase Page operation allows the user to erase (set user data to zero) any page within the FB.

The use of the OVERWRITEPAGE and PAGELOSSPROTECT pins is the same for erase as for a Program Page operation.

As with the Program Page operation, a STATUS of '01' indicates that the addressed page is not erased.

A waveform for an Erase Page operation is shown in Figure 2-37.

Erase errors include the following:

1. Attempting to erase a page that is Overwrite Protected (STATUS = '01')
2. Attempting to erase a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection mode (STATUS = '01')
3. The Write Count of the erased page exceeding the Write Threshold defined in the part specification (STATUS = '11')
4. The ECC Logic determining that there is an uncorrectable error within the erased page (STATUS = '10')

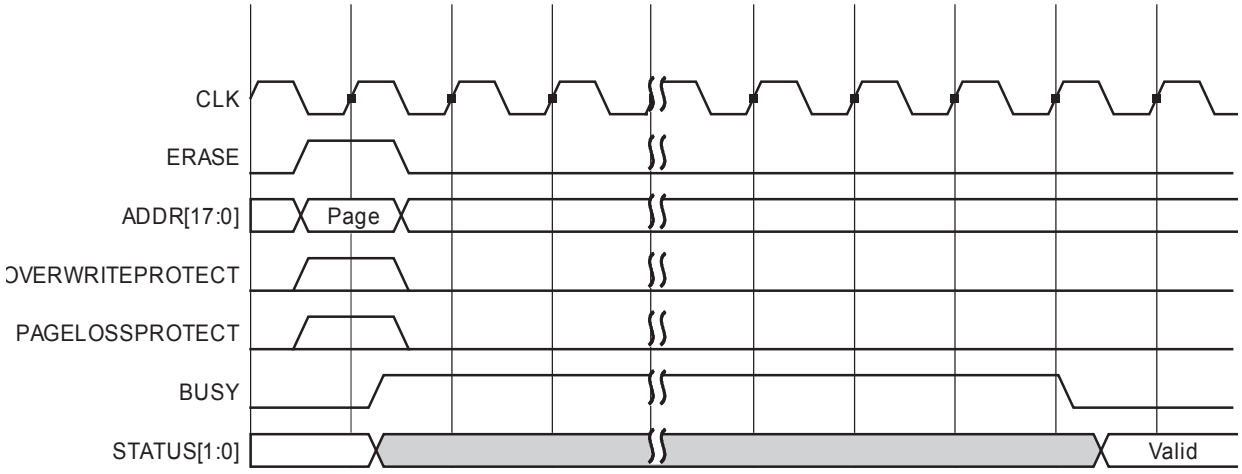

Figure 2-37 • **FB Erase Page Waveform**

Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in Figure 2-40 and Figure 2-41.

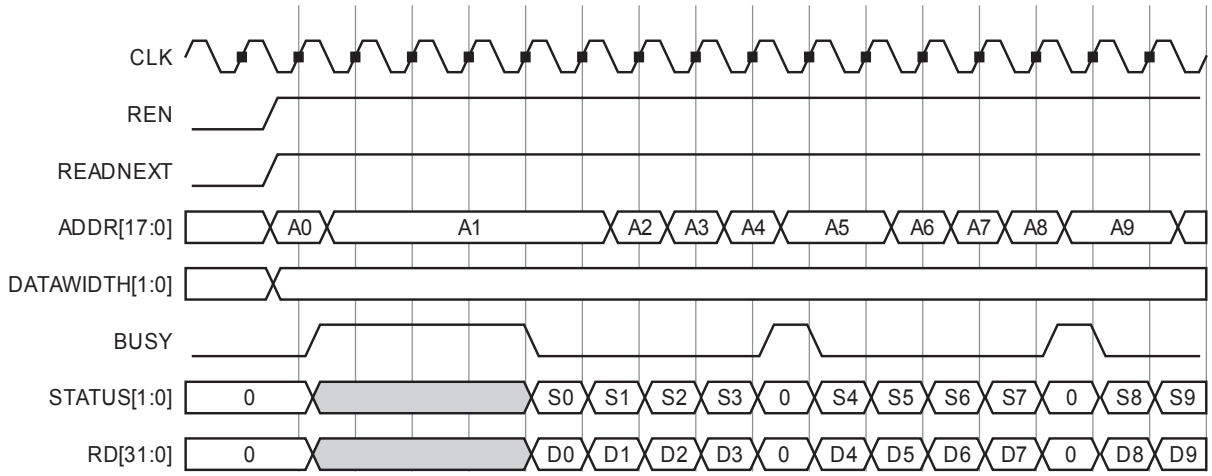

***Figure 2-40* • Read Next Waveform (Non-Pipe Mode, 32-bit access)**

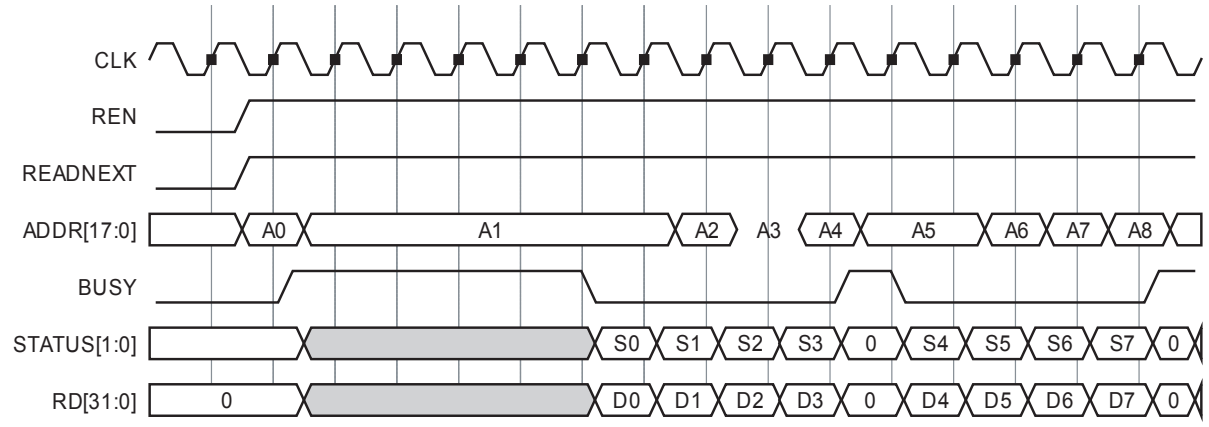

***Figure 2-41* • Read Next WaveForm (Pipe Mode, 32-bit access)**

Table 2-36 • **Analog Block Pin Description (continued)**

Signal Name	Number of Bits	Direction	Function	Location of Details
AG6	1	Output		Analog Quad
AT6	1	Input		Analog Quad
ATRETURN67	1	Input	Temperature monitor return shared by Analog Quads 6 and 7	Analog Quad
AV7	1	Input	Analog Quad 7	Analog Quad
AC7	1	Input		Analog Quad
AG7	1	Output		Analog Quad
AT7	1	Input		Analog Quad
AV8	1	Input	Analog Quad 8	Analog Quad
AC8	1	Input		Analog Quad
AG8	1	Output		Analog Quad
AT8	1	Input		Analog Quad
ATRETURN89	1	Input	Temperature monitor return shared by Analog Quads 8 and 9	Analog Quad
AV9	1	Input	Analog Quad 9	Analog Quad
AC9	1	Input		Analog Quad
AG9	1	Output		Analog Quad
AT9	1	Input		Analog Quad
RTCMATCH	1	Output	MATCH	RTC
RTCPSMMATCH	1	Output	MATCH connected to VRPSM	RTC
RTCXTLMODE[1:0]	2	Output	Drives XTLOSC RTCMODE[1:0] pins	RTC
RTCXTLSEL	1	Output	Drives XTLOSC MODESEL pin	RTC
RTCCLK	1	Input	RTC clock input	RTC

Analog Quad

With the Fusion family, Microsemi introduces the Analog Quad, shown in Figure 2-65 on page 2-81, as the basic analog I/O structure. The Analog Quad is a four-channel system used to precondition a set of analog signals before sending it to the ADC for conversion into a digital signal. To maximize the usefulness of the Analog Quad, the analog input signals can also be configured as LVTTL digital input signals. The Analog Quad is divided into four sections.

The first section is called the Voltage Monitor Block, and its input pin is named AV. It contains a two-channel analog multiplexer that allows an incoming analog signal to be routed directly to the ADC or allows the signal to be routed to a prescaler circuit before being sent to the ADC. The prescaler can be configured to accept analog signals between –12 V and 0 or between 0 and +12 V. The prescaler circuit scales the voltage applied to the ADC input pad such that it is compatible with the ADC input voltage range. The AV pin can also be used as a digital input pin.

The second section of the Analog Quad is called the Current Monitor Block. Its input pin is named AC. The Current Monitor Block contains all the same functions as the Voltage Monitor Block with one addition, which is a current monitoring function. A small external current sensing resistor (typically less than 1 Ω) is connected between the AV and AC pins and is in series with a power source. The Current Monitor Block contains a current monitor circuit that converts the current through the external resistor to a voltage that can then be read using the ADC.

Table 2-51 • Uncalibrated Analog Channel Accuracy*
Worst-Case Industrial Conditions, T_J = 85°C

		Total Channel Error (LSB)			Channel Input Offset Error (LSB)			Channel Input Offset Error (mV)			Channel Gain Error (%FSR)		
Analog Pad	**Prescaler Range (V)**	**Neg. Max.**	**Med.**	**Pos. Max.**	**Neg Max**	**Med.**	**Pos. Max.**	**Neg. Max.**	**Med.**	**Pos. Max.**	**Min.**	**Typ.**	**Max.**
Positive Range		**ADC in 10-Bit Mode**											
AV, AC	16	–22	–2	12	–11	–2	14	–169	–32	224	3	0	–3
	8	–40	–5	17	–11	–5	21	–87	–40	166	2	0	–4
	4	–45	–9	24	–16	–11	36	–63	–43	144	2	0	–4
	2	–70	–19	33	–33	–20	66	–66	–39	131	2	0	–4
	1	–25	–7	5	–11	–3	26	–11	–3	26	3	–1	–3
	0.5	–41	–12	8	–12	–7	38	–6	–4	19	3	–1	–3
	0.25	–53	–14	19	–20	–14	40	–5	–3	10	5	0	–4
	0.125	–89	–29	24	–40	–28	88	–5	–4	11	7	0	–5
AT	16	–3	9	15	–4	0	4	–64	5	64	1	0	–1
	4	–10	2	15	–11	–2	11	–44	–8	44	1	0	–1
Negative Range		**ADC in 10-Bit Mode**											
AV, AC	16	–35	–10	9	–24	–6	9	–383	–96	148	5	–1	–6
	8	–65	–19	12	–34	–12	9	–268	–99	75	5	–1	–5
	4	–86	–28	21	–64	–24	19	–254	–96	76	5	–1	–6
	2	–136	–53	37	–115	–42	39	–230	–83	78	6	–2	–7
	1	–98	–35	8	–39	–8	15	–39	–8	15	10	–3	–10
	0.5	–121	–46	7	–54	–14	18	–27	–7	9	10	–4	–11
	0.25	–149	–49	19	–72	–16	40	–18	–4	10	14	–4	–12
	0.125	–188	–67	38	–112	–27	56	–14	–3	7	16	–5	–14

*Note: *Channel Accuracy includes prescaler and ADC accuracies. For 12-bit mode, multiply the LSB count by 4. For 8-bit mode, divide the LSB count by 4. Gain remains the same.*

For Fusion devices requiring Level 3 and/or Level 4 compliance, the board drivers connected to Fusion I/Os need to have 10 kΩ (or lower) output drive resistance at hot insertion, and 1 kΩ (or lower) output drive resistance at hot removal. This is the resistance of the transmitter sending a signal to the Fusion I/O, and no additional resistance is needed on the board. If that cannot be assured, three levels of staging can be used to meet Level 3 and/or Level 4 compliance. Cards with two levels of staging should have the following sequence:

1. Grounds
2. Powers, I/Os, other pins

Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

Pro I/O banks and standard I/O banks fully support cold-sparing.

For Pro I/O banks, standards such as PCI that require I/O clamp diodes, can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

For Advanced I/O banks, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each advanced I/O pin to 0 V.

If Standard I/O banks are used in applications requiring cold-sparing, a discharge path from the power supply to ground should be provided. This can be done with a discharge resistor or a switched resistor. This is necessary because the standard I/O buffers do not have built-in I/O clamp diodes.

If a resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitor is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if the pin is configured with either a pull-up or pull down resistor and driven in the opposite direction. A small static current is induced on each IO pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Please refer to Table 2-95 on page 2-169, Table 2-96 on page 2-169, and Table 2-97 on page 2-171 for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTL 3.3 V input pin is configured with a weak Pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven low. For an LVTTL 3.3 V, pull-up resistor is ~45 kΩ and the resulting current is equal to 3.3 V / 45 kΩ = 73 µA for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven high. Avoiding this current can be done by driving the input low when a weak pull-down resistor is used, and driving it high when a weak pull-up resistor is used.

In Active and Static modes, this current draw can occur in the following cases:

- Input buffers with pull-up, driven low
- Input buffers with pull-down, driven high
- Bidirectional buffers with pull-up, driven low
- Bidirectional buffers with pull-down, driven high
- Output buffers with pull-up, driven low
- Output buffers with pull-down, driven high
- Tristate buffers with pull-up, driven low
- Tristate buffers with pull-down, driven high

***Table 2-77* • Comparison Table for 5 V–Compliant Receiver Scheme**

Scheme	Board Components	Speed	Current Limitations
1	Two resistors	Low to high[1]	Limited by transmitter's drive strength
2	Resistor and Zener 3.3 V	Medium	Limited by transmitter's drive strength
3	Bus switch	High	N/A
4	Minimum resistor value[2] R = 47 Ω at T_J = 70°C R = 150 Ω at T_J = 85°C R = 420 Ω at T_J = 100°C	Medium	Maximum diode current at 100% duty cycle, signal constantly at '1' 52.7 mA at T_J =70°C / 10-year lifetime 16.5 mA at T_J = 85°C / 10-year lifetime 5.9 mA at T_J = 100°C / 10-year lifetime For duty cycles other than 100%, the currents can be increased by a factor = 1 / (duty cycle). Example: 20% duty cycle at 70°C Maximum current = (1 / 0.2) * 52.7 mA = 5 * 52.7 mA = 263.5 mA

Notes:

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long-term reliability.*

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss or transmitter overstress due to transmitter-to-transmitter current shorts. Figure 2-110 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-111 shows how bus contention is created, and Figure 2-112 on page 2-151 shows how it can be avoided with the skew circuit.

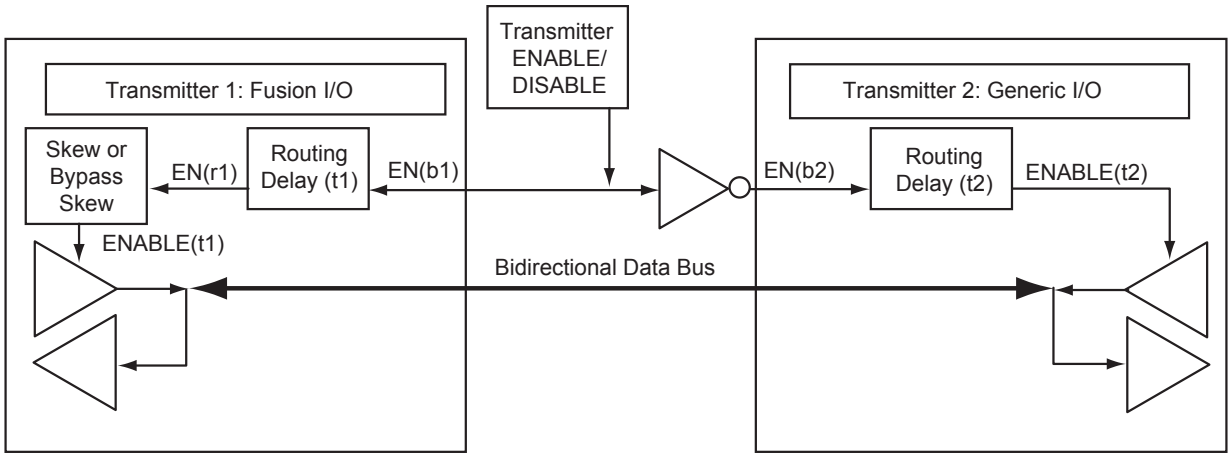

Figure 2-110 • **Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using Fusion Devices**

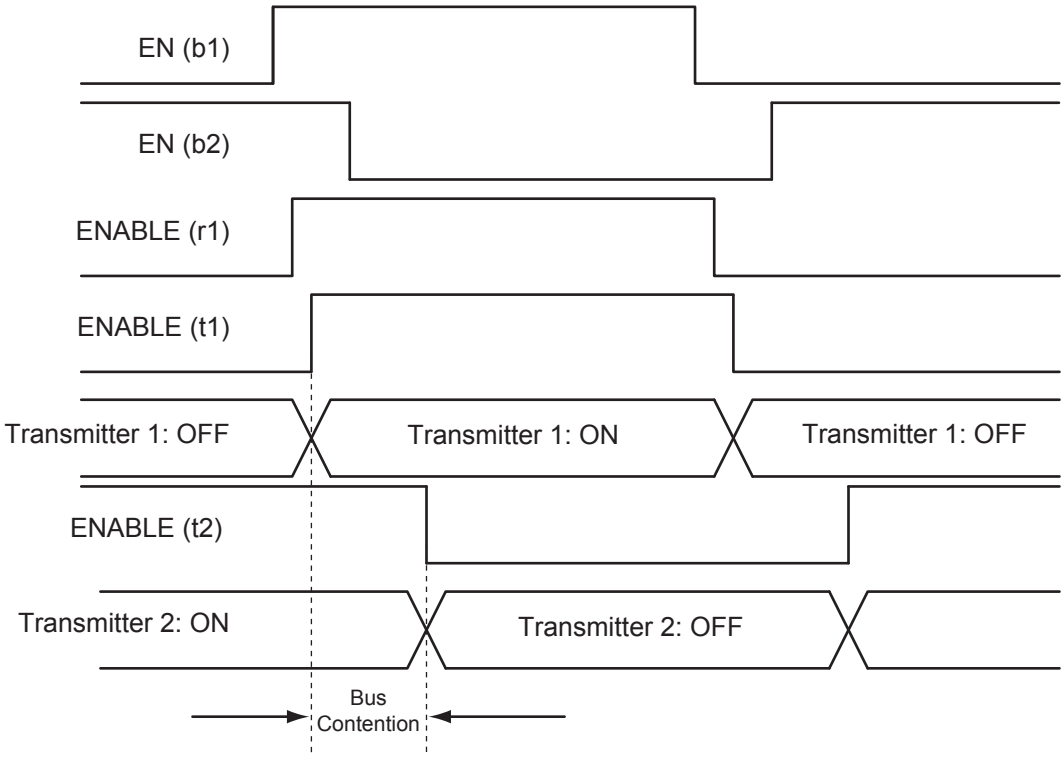

Figure 2-111 • **Timing Diagram (bypasses skew circuit)**

***Table 2-78* • Fusion Standard I/O Standards—OUT_DRIVE Settings**

I/O Standards	OUT_DRIVE (mA)					
	2	4	6	8	Slew	
LVTTL/LVCMOS 3.3 V	3	3	3	3	High	Low
LVCMOS 2.5 V	3	3	3	3	High	Low
LVCMOS 1.8 V	3	3	–	–	High	Low
LVCMOS 1.5 V	3	–	–	–	High	Low

***Table 2-79* • Fusion Advanced I/O Standards—SLEW and OUT_DRIVE Settings**

I/O Standards	OUT_DRIVE (mA)							
	2	4	6	8	12	16	Slew	
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3	High	Low
LVCMOS 2.5 V	3	3	3	3	3	–	High	Low
LVCMOS 1.8 V	3	3	3	3	–	–	High	Low
LVCMOS 1.5 V	3	3	–	–	–	–	High	Low

***Table 2-80* • Fusion Pro I/O Standards—SLEW and OUT_DRIVE Settings**

I/O Standards	OUT_DRIVE (mA)							Slew	
	2	4	6	8	12	16	24		
LVTTL/LVCMOS 3.3 V	3	3	3	3	3	3	3	High	Low
LVCMOS 2.5 V	3	3	3	3	3	3	3	High	Low
LVCMOS 2.5 V/5.0 V	3	3	3	3	3	3	3	High	Low
LVCMOS 1.8 V	3	3	3	3	3	3	–	High	Low
LVCMOS 1.5 V	3	3	3	3	3	–	–	High	Low

Table 2-92 • Summary of I/O Timing Characteristics – Software Default Settings
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCI = I/O Standard Dependent
Applicable to Pro I/Os

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ohm)	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTL/ 3.3 V LVCMOS	12 mA	High	35	–	0.49	2.74	0.03	0.90	1.17	0.32	2.79	2.14	2.45	2.70	4.46	3.81	ns
2.5 V LVCMOS	12 mA	High	35	–	0.49	2.80	0.03	1.13	1.24	0.32	2.85	2.61	2.51	2.61	4.52	4.28	ns
1.8 V LVCMOS	12 mA	High	35	–	0.49	2.83	0.03	1.08	1.42	0.32	2.89	2.31	2.79	3.16	4.56	3.98	ns
1.5 V LVCMOS	12 mA	High	35	–	0.49	3.30	0.03	1.27	1.60	0.32	3.36	2.70	2.96	3.27	5.03	4.37	ns
3.3 V PCI	Per PCI spec	High	10	25 [2]	0.49	2.09	0.03	0.78	1.25	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25 [2]	0.49	2.09	0.03	0.77	1.17	0.32	2.13	1.49	2.45	2.70	3.80	3.16	ns
3.3 V GTL	20 mA	High	10	25	0.49	1.55	0.03	2.19	–	0.32	1.52	1.55	0.00	0.00	3.19	3.22	ns
2.5 V GTL	20 mA	High	10	25	0.49	1.59	0.03	1.83	–	0.32	1.61	1.59	0.00	0.00	3.28	3.26	ns
3.3 V GTL+	35 mA	High	10	25	0.49	1.53	0.03	1.19	–	0.32	1.56	1.53	0.00	0.00	3.23	3.20	ns
2.5 V GTL+	33 mA	High	10	25	0.49	1.65	0.03	1.13	–	0.32	1.68	1.57	0.00	0.00	3.35	3.24	ns
HSTL (I)	8 mA	High	20	50	0.49	2.37	0.03	1.59	–	0.32	2.42	2.35	0.00	0.00	4.09	4.02	ns
HSTL (II)	15 mA	High	20	25	0.49	2.26	0.03	1.59	–	0.32	2.30	2.03	0.00	0.00	3.97	3.70	ns
SSTL2 (I)	17 mA	High	30	50	0.49	1.59	0.03	1.00	–	0.32	1.62	1.38	0.00	0.00	3.29	3.05	ns
SSTL2 (II)	21 mA	High	30	25	0.49	1.62	0.03	1.00	–	0.32	1.65	1.32	0.00	0.00	3.32	2.99	ns
SSTL3 (I)	16 mA	High	30	50	0.49	1.72	0.03	0.93	–	0.32	1.75	1.37	0.00	0.00	3.42	3.04	ns
SSTL3 (II)	24 mA	High	30	25	0.49	1.54	0.03	0.93	–	0.32	1.57	1.25	0.00	0.00	3.24	2.92	ns
LVDS	24 mA	High	–	–	0.49	1.57	0.03	1.36	–	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.49	1.60	0.03	1.22	–	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage-supply levels, refer to Table 3-6 on page 3-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-123 on page 2-197 for connectivity. This resistor is not required during normal operation.*

Table 2-123 • 1.8 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	–1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	–2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	–1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	–2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
8 mA	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	–1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	–2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
12 mA	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	–1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	–2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
16 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	–1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	–2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-124 • 1.8 V LVCMOS Low Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	15.01	0.04	1.20	0.43	13.15	15.01	1.99	1.99	ns
	–1	0.56	12.77	0.04	1.02	0.36	11.19	12.77	1.70	1.70	ns
	–2	0.49	11.21	0.03	0.90	0.32	9.82	11.21	1.49	1.49	ns
4 mA	Std.	0.66	10.10	0.04	1.20	0.43	9.55	10.10	2.41	2.37	ns
	–1	0.56	8.59	0.04	1.02	0.36	8.13	8.59	2.05	2.02	ns
	–2	0.49	7.54	0.03	0.90	0.32	7.13	7.54	1.80	1.77	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-125 • 1.8 V LVCMOS High Slew
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard I/Os

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	11.21	0.04	1.20	0.43	8.53	11.21	1.99	1.21	ns
	–1	0.56	9.54	0.04	1.02	0.36	7.26	9.54	1.69	1.03	ns
	–2	0.49	8.37	0.03	0.90	0.32	6.37	8.37	1.49	0.90	ns
4 mA	Std.	0.66	6.34	0.04	1.20	0.43	5.38	6.34	2.41	2.48	ns
	–1	0.56	5.40	0.04	1.02	0.36	4.58	5.40	2.05	2.11	ns
	–2	0.49	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

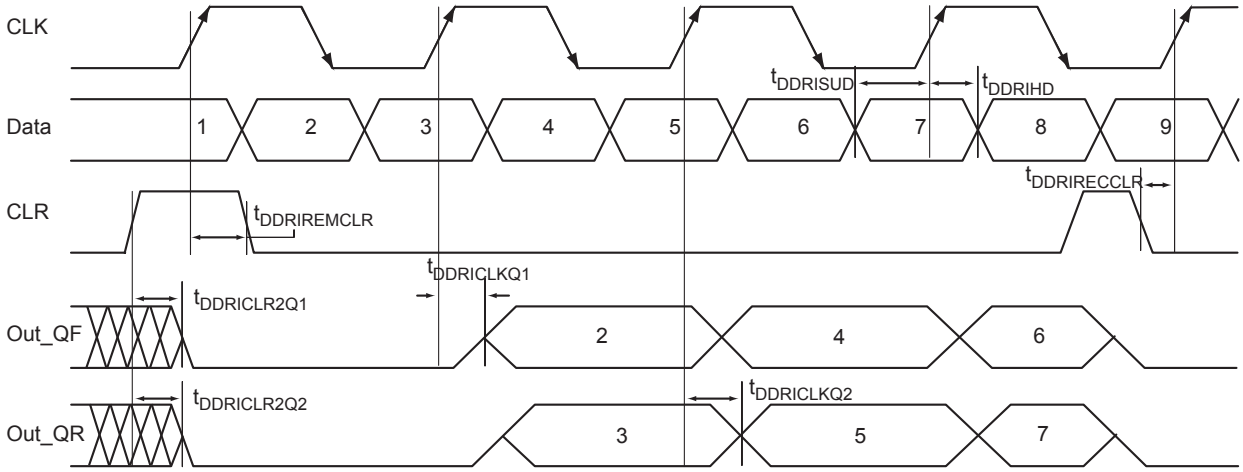

Figure 2-143 • **Input DDR Timing Diagram**

Timing Characteristics

Table 2-180 • **Input DDR Propagation Delays**
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.39	0.44	0.52	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.27	0.31	0.37	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.28	0.32	0.38	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.57	0.65	0.76	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.46	0.53	0.62	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.22	0.25	0.30	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.37	0.43	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	1404	1232	1048	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

XTAL2 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates highly secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a security-protected programming environment (such as the Microsemi in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and with high level security by simply sending a STAPL file with AES-encrypted data. Highly secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the *Fusion Security* application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (protected with security) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain as secure as possible.

AES decryption can also be used on the 1,024-bit FlashROM to allow for remote updates of the FlashROM contents. This allows for easy support of subscription model products and protects them with measures designed to provide the highest level of security available. See the application note *Fusion Security* for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This provides the best available security during update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.

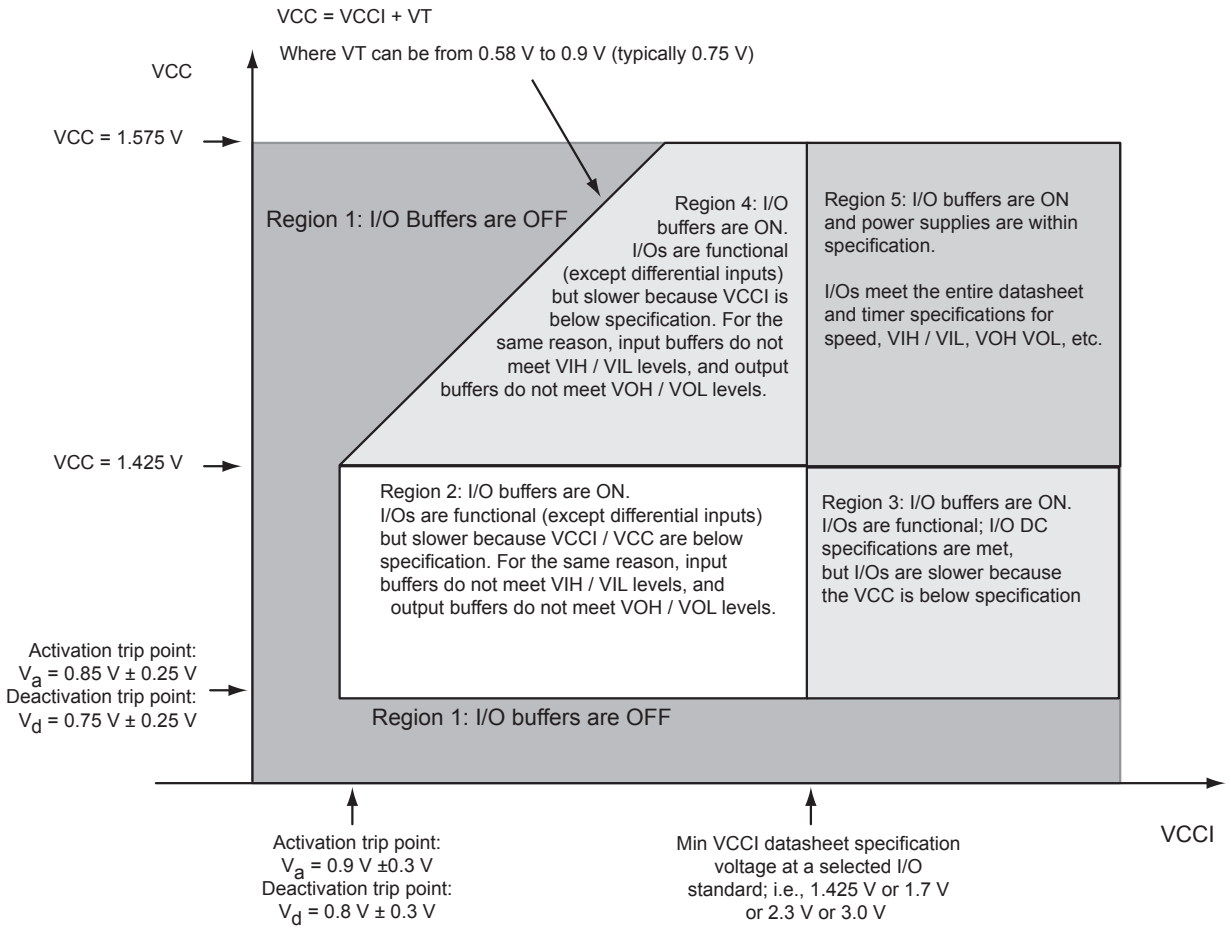

Figure 3-1 • **I/O State as a Function of VCCI and VCC Voltage Levels**

FG256				
Pin Number	**AFS090 Function**	**AFS250 Function**	**AFS600 Function**	**AFS1500 Function**
M15	TRST	TRST	TRST	TRST
M16	GND	GND	GND	GND
N1	GEB2/IO42PDB3V0	GEB2/IO59PDB3V0	GEB2/IO59PDB4V0	GEB2/IO86PDB4V0
N2	GEA2/IO42NDB3V0	IO59NDB3V0	IO59NDB4V0	IO86NDB4V0
N3	NC	GEA2/IO58PPB3V0	GEA2/IO58PPB4V0	GEA2/IO85PPB4V0
N4	VCC33PMP	VCC33PMP	VCC33PMP	VCC33PMP
N5	VCC15A	VCC15A	VCC15A	VCC15A
N6	NC	NC	AG0	AG0
N7	AC1	AC1	AC3	AC3
N8	AG3	AG3	AG5	AG5
N9	AV3	AV3	AV5	AV5
N10	AG4	AG4	AG6	AG6
N11	NC	NC	AC8	AC8
N12	GNDA	GNDA	GNDA	GNDA
N13	VCC33A	VCC33A	VCC33A	VCC33A
N14	VCCNVM	VCCNVM	VCCNVM	VCCNVM
N15	TCK	TCK	TCK	TCK
N16	TDI	TDI	TDI	TDI
P1	VCCNVM	VCCNVM	VCCNVM	VCCNVM
P2	GNDNVM	GNDNVM	GNDNVM	GNDNVM
P3	GNDA	GNDA	GNDA	GNDA
P4	NC	NC	AC0	AC0
P5	NC	NC	AG1	AG1
P6	NC	NC	AV1	AV1
P7	AG0	AG0	AG2	AG2
P8	AG2	AG2	AG4	AG4
P9	GNDA	GNDA	GNDA	GNDA
P10	NC	AC5	AC7	AC7
P11	NC	NC	AV8	AV8
P12	NC	NC	AG8	AG8
P13	NC	NC	AV9	AV9
P14	ADCGNDREF	ADCGNDREF	ADCGNDREF	ADCGNDREF
P15	PTBASE	PTBASE	PTBASE	PTBASE
P16	GNDNVM	GNDNVM	GNDNVM	GNDNVM
R1	VCCIB3	VCCIB3	VCCIB4	VCCIB4
R2	PCAP	PCAP	PCAP	PCAP
R3	NC	NC	AT1	AT1
R4	NC	NC	AT0	AT0