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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	93
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m1afs250-1pqg208

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Advanced Architecture

The proprietary Fusion architecture provides granularity comparable to standard-cell ASICs. The Fusion device consists of several distinct and programmable architectural features, including the following (Figure 1-1 on page 1-5):

- Embedded memories
 - Flash memory blocks
 - FlashROM
 - SRAM and FIFO
- Clocking resources
 - PLL and CCC
 - RC oscillator
 - Crystal oscillator
 - No-Glitch MUX (NGMUX)
- Digital I/Os with advanced I/O standards
- FPGA VersaTiles
- Analog components
 - ADC
 - Analog I/Os supporting voltage, current, and temperature monitoring
 - 1.5 V on-board voltage regulator
 - Real-time counter

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic lookup table (LUT) equivalent or a D-flip-flop or latch (with or without enable) by programming the appropriate flash switch interconnections. This versatility allows efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi families of flash-based FPGAs. VersaTiles and larger functions are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid (3.3 V) single-voltage programming of Fusion devices via an IEEE 1532 JTAG interface.

Unprecedented Integration

Integrated Analog Blocks and Analog I/Os

Fusion devices offer robust and flexible analog mixed signal capability in addition to the highperformance flash FPGA fabric and flash memory block. The many built-in analog peripherals include a configurable 32:1 input analog MUX, up to 10 independent MOSFET gate driver outputs, and a configurable ADC. The ADC supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 k samples per second (Ksps), differential nonlinearity (DNL) < 1.0 LSB, and Total Unadjusted Error (TUE) of 0.72 LSB in 10-bit mode. The TUE is used for characterization of the conversion error and includes errors from all sources, such as offset and linearity. Internal bandgap circuitry offers 1% voltage reference accuracy with the flexibility of utilizing an external reference voltage. The ADC channel sampling sequence and sampling rate are programmable and implemented in the FPGA logic using Designer and Libero SoC software tool support.

Two channels of the 32-channel ADCMUX are dedicated. Channel 0 is connected internally to VCC and can be used to monitor core power supply. Channel 31 is connected to an internal temperature diode which can be used to monitor device temperature. The 30 remaining channels can be connected to external analog signals. The exact number of I/Os available for external connection signals is device-dependent (refer to the "Fusion Family" table on page I for details).



2 – Device Architecture

Fusion Stack Architecture

To manage the unprecedented level of integration in Fusion devices, Microsemi developed the Fusion technology stack (Figure 2-1). This layered model offers a flexible design environment, enabling design at very high and very low levels of abstraction. Fusion peripherals include hard analog IP and hard and soft digital IP. Peripherals communicate across the FPGA fabric via a layer of soft gates—the Fusion backbone. Much more than a common bus interface, this Fusion backbone integrates a micro-sequencer within the FPGA fabric and configures the individual peripherals and supports low-level processing of peripheral data. Fusion applets are application building blocks that can control and respond to peripherals and other system signals. Applets can be rapidly combined to create large applications. The technology is scalable across devices, families, design types, and user expertise, and supports a well-defined interface for external IP and tool integration.

At the lowest level, Level 0, are Fusion peripherals. These are configurable functional blocks that can be hardwired structures such as a PLL or analog input channel, or soft (FPGA gate) blocks such as a UART or two-wire serial interface. The Fusion peripherals are configurable and support a standard interface to facilitate communication and implementation.

Connecting and controlling access to the peripherals is the Fusion backbone, Level 1. The backbone is a soft-gate structure, scalable to any number of peripherals. The backbone is a bus and much more; it manages peripheral configuration to ensure proper operation. Leveraging the common peripheral interface and a low-level state machine, the backbone efficiently offloads peripheral management from the system design. The backbone can set and clear flags based upon peripheral behavior and can define performance criteria. The flexibility of the stack enables a designer to configure the silicon, directly bypassing the backbone if that level of control is desired.

One step up from the backbone is the Fusion applet, Level 2. The applet is an application building block that implements a specific function in FPGA gates. It can react to stimuli and board-level events coming through the backbone or from other sources, and responds to these stimuli by accessing and manipulating peripherals via the backbone or initiating some other action. An applet controls or responds to the peripheral(s). Applets can be easily imported or exported from the design environment. The applet structure is open and well-defined, enabling users to import applets from Microsemi, system developers, third parties, and user groups.



Note: Levels 1, 2, and 3 are implemented in FPGA logic gates.

Figure 2-1 • Fusion Architecture Stack

Program Operation

A Program operation is initiated by asserting the PROGRAM signal on the interface. Program operations save the contents of the Page Buffer to the FB Array. Due to the technologies inherent in the FB, the total programming (including erase) time per page of the eNVM is 6.8 ms. While the FB is writing the data to the array, the BUSY signal will be asserted.

During a Program operation, the sector and page addresses on ADDR are compared with the stored address for the page (and sector) in the Page Buffer. If there is a mismatch between the two addresses, the Program operation will be aborted and an error will be reported on the STATUS output.

It is possible to write the Page Buffer to a different page in memory. When asserting the PROGRAM pin, if OVERWRITEPAGE is asserted as well, the FB will write the contents of the Page Buffer to the sector and page designated on the ADDR inputs if the destination page is not Overwrite Protected.

A Program operation can be utilized to either modify the contents of the page in the flash memory block or change the protections for the page. Setting the OVERWRITEPROTECT bit on the interface while asserting the PROGRAM pin will put the page addressed into Overwrite Protect Mode. Overwrite Protect Mode safeguards a page from being inadvertently overwritten during subsequent Program or Erase operations.

Program operations that result in a STATUS value of '01' do not modify the addressed page. For all other values of STATUS, the addressed page is modified. Program errors include the following:

- 1. Attempting to program a page that is Overwrite Protected (STATUS = '01')
- 2. Attempting to program a page that is not in the Page Buffer when the Page Buffer has entered Page Loss Protection Mode (STATUS = '01')
- Attempting to perform a program with OVERWRITEPAGE set when the page addressed has been Overwrite Protected (STATUS = '01')
- 4. The Write Count of the page programmed exceeding the Write Threshold defined in the part specification (STATUS = '11')
- 5. The ECC Logic determining that there is an uncorrectable error within the programmed page (STATUS = '10')
- 6. Attempting to program a page that is **not** in the Page Buffer when OVERWRITEPAGE is not set and the page in the Page Buffer is modified (STATUS = '01')
- 7. Attempting to program the page in the Page Buffer when the Page Buffer is **not** modified

The waveform for a Program operation is shown in Figure 2-36.



Figure 2-36 • FB Program Waveform

Note: OVERWRITEPAGE is only sampled when the PROGRAM or ERASEPAGE pins are asserted. OVERWRITEPAGE is ignored in all other operations.





Figure 2-54 • One Port Write / Other Port Read Same



Figure 2-55 • RAM Reset. Applicable to both RAM4K9 and RAM512x18.



The third part of the Analog Quad is called the Gate Driver Block, and its output pin is named AG. This section is used to drive an external FET. There are two modes available: a High Current Drive mode and a Current Source Control mode. Both negative and positive voltage polarities are available, and in the current source control mode, four different current levels are available.

The fourth section of the Analog Quad is called the Temperature Monitor Block, and its input pin name is AT. This block is similar to the Voltage Monitor Block, except that it has an additional function: it can be used to monitor the temperature of an external diode-connected transistor. It has a modified prescaler and is limited to positive voltages only.

The Analog Quad can be configured during design time by Libero SoC; however, the ACM can be used to change the parameters of any of these I/Os during runtime. This type of change is referred to as a context switch. The Analog Quad is a modular structure that is replicated to generate the analog I/O resources. Each Fusion device supports between 5 and 10 Analog Quads.

The analog pads are numbered to clearly identify both the type of pad (voltage, current, gate driver, or temperature pad) and its corresponding Analog Quad (AV0, AC0, AG0, AT0, AV1, ..., AC9, AG9, and AT9). There are three types of input pads (AVx, ACx, and ATx) and one type of analog output pad (AGx). Since there can be up to 10 Analog Quads on a device, there can be a maximum of 30 analog input pads and 10 analog output pads.



Figure 2-65 • Analog Quad

ADC Terminology

Conversion Time

Conversion time is the interval between the release of the hold state (imposed by the input circuitry of a track-and-hold) and the instant at which the voltage on the sampling capacitor settles to within one LSB of a new input value.

DNL – Differential Non-Linearity

For an ideal ADC, the analog-input levels that trigger any two successive output codes should differ by one LSB (DNL = 0). Any deviation from one LSB in defined as DNL (Figure 2-83).



Figure 2-83 • Differential Non-Linearity (DNL)

ENOB – Effective Number of Bits

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization of noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD (also see "Signal-to-Noise and Distortion Ratio (SINAD)".) ENOB for a full-scale, sinusoidal input waveform is computed using EQ 12.

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

EQ 12

FS Error – Full-Scale Error

Full-scale error is the difference between the actual value that triggers that transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error.



Device Architecture

Integrated Voltage Reference

The Fusion device has an integrated on-chip 2.56 V reference voltage for the ADC. The value of this reference voltage was chosen to make the prescaling and postscaling factors for the prescaler blocks change in a binary fashion. However, if desired, an external reference voltage of up to 3.3 V can be connected between the VAREF and ADCGNDREF pins. The VAREFSEL control pin is used to select the reference voltage.

Table 2-42 • VAREF Bit Function

Name	Bit	Function
VAREF	0	Reference voltage selection
		0 – Internal voltage reference selected. VAREF pin outputs 2.56 V.
		1 – Input external voltage reference from VAREF and ADCGNDREF

ADC Clock

The speed of the ADC depends on its internal clock, ADCCLK, which is not accessible to users. The ADCCLK is derived from SYSCLK. Input signal TVC[7:0], Time Divider Control, determines the speed of the ADCCLK in relationship to SYSCLK, based on EQ 15.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK}$$

EQ 15

TVC: Time Divider Control (0-255)

 t_{ADCCLK} is the period of ADCCLK, and must be between 0.5 MHz and 10 MHz t_{SYSCLK} is the period of SYSCLK

Table 2-43 • TVC Bits Function

Name	Bits	Function		
TVC	[7:0]	SYSCLK divider control		

The frequency of ADCCLK, f_{ADCCLK}, must be within 0.5 Hz to 10 MHz.

The inputs to the ADC are synchronized to SYSCLK. A conversion is initiated by asserting the ADCSTART signal on a rising edge of SYSCLK. Figure 2-90 on page 2-112 and Figure 2-91 on page 2-112 show the timing diagram for the ADC.

Acquisition Time or Sample Time Control

Acquisition time (t_{SAMPLE}) specifies how long an analog input signal has to charge the internal capacitor array. Figure 2-88 shows a simplified internal input sampling mechanism of a SAR ADC.



Figure 2-88 • Simplified Sample and Hold Circuitry

The internal impedance (Z_{INAD}), external source resistance (R_{SOURCE}), and sample capacitor (C_{INAD}) form a simple RC network. As a result, the accuracy of the ADC can be affected if the ADC is given insufficient time to charge the capacitor. To resolve this problem, you can either reduce the source resistance or increase the sampling time by changing the acquisition time using the STC signal.



Figure 2-90 • Input Setup Time

Standard Conversion



Notes:

1. Refer to EQ 20 on page 2-109 for the calculation on the sample time, t_{SAMPLE} .

2. See EQ 23 on page 2-109 for calculation of the conversion time, t_{CONV} .

3. Minimum time to issue an ADCSTART after DATAVALID is 1 SYSCLK period

Figure 2-91 • Standard Conversion Status Signal Timing Diagram

Analog Configuration MUX

The ACM is the interface between the FPGA, the Analog Block configurations, and the real-time counter. Microsemi Libero SoC will generate IP that will load and configure the Analog Block via the ACM. However, users are not limited to using the Libero SoC IP. This section provides a detailed description of the ACM's register map, truth tables for proper configuration of the Analog Block and RTC, as well as timing waveforms so users can access and control the ACM directly from their designs.

The Analog Block contains four 8-bit latches per Analog Quad that are initialized through the ACM. These latches act as configuration bits for Analog Quads. The ACM block runs from the core voltage supply (1.5 V).

Access to the ACM is achieved via 8-bit address and data busses with enables. The pin list is provided in Table 2-36 on page 2-78. The ACM clock speed is limited to a maximum of 10 MHz, more than sufficient to handle the low-bandwidth requirements of configuring the Analog Block and the RTC (sub-block of the Analog Block).

Table 2-54 decodes the ACM address space and maps it to the corresponding Analog Quad and configuration byte for that quad.

ACMADDR [7:0] in Decimal	Name	Description	Associated Peripheral		
0	-	_	Analog Quad		
1	AQ0	Byte 0	Analog Quad		
2	AQ0	Byte 1	Analog Quad		
3	AQ0	Byte 2	Analog Quad		
4	AQ0	Byte 3	Analog Quad		
5	AQ1	Byte 0	Analog Quad		
			Analog Quad		
	· .	· · ·			
36	AQ8	Byte 3	Analog Quad		
37	AQ9	Byte 0	Analog Quad		
38	AQ9	Byte 1	Analog Quad		
39	AQ9	Byte 2	Analog Quad		
40	AQ9	Byte 3	Analog Quad		
41		Undefined	Analog Quad		
		Undefined	Analog Quad		
	· · ·				
63		Undefined	RTC		
64	COUNTER0	Counter bits 7:0	RTC		
65	COUNTER1	Counter bits 15:8	RTC		
66	COUNTER2	Counter bits 23:16	RTC		
67	COUNTER3	Counter bits 31:24	RTC		
68	COUNTER4	Counter bits 39:32	RTC		
72	MATCHREG0	Match register bits 7:0 RTC			

Table 2-54 • ACM Address Decode Table for Analog Quad

Table 2-82 • Advanced I/O Default Attributes

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	Refer to the following	Refer to the following tables	Off	None	35 pF	-
LVCMOS 2.5 V	information:	Table 2-78 on page 2-152	Off	None	35 pF	-
LVCMOS 2.5/5.0 V	Table 2-78 on page 2-152	Table 2-79 on page 2-152	Off	None	35 pF	-
LVCMOS 1.8 V	Table 2-79 on page 2-152	Table 2-80 on page 2-152	Off	None	35 pF	-
LVCMOS 1.5 V	Table 2-80 on page 2-152		Off	None	35 pF	-
PCI (3.3 V)			Off	None	10 pF	-
PCI-X (3.3 V)			Off	None	10 pF	-
LVDS, BLVDS, M-LVDS			Off	None	_	_
LVPECL			Off	None	-	-

Microsemi

Device Architecture

Table 2-123 • 1.8 V LVCMOS High Slew

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Advanced I/Os

Drive	Speed		4	4	4	4	4	4		4	4		11
Strength	Grade	^t DOUT	τ _{DP}	τ _{DIN}	τργ	^τ EOUT	τ _{ZL}	τ _{ZH}	τ _{LZ}	^τ ΗΖ	^t ZLS	τzhs	Units
2 mA	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	-1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	-2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	-1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	-2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
8 mA	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	-1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	-2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
12 mA	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	-1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	-2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
16 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	-1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	-2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Table 2-124 • 1.8 V LVCMOS Low Slew

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V Applicable to Standard I/Os

Drive	Speed										
Strength	Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{eout}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	15.01	0.04	1.20	0.43	13.15	15.01	1.99	1.99	ns
	–1	0.56	12.77	0.04	1.02	0.36	11.19	12.77	1.70	1.70	ns
	-2	0.49	11.21	0.03	0.90	0.32	9.82	11.21	1.49	1.49	ns
4 mA	Std.	0.66	10.10	0.04	1.20	0.43	9.55	10.10	2.41	2.37	ns
	–1	0.56	8.59	0.04	1.02	0.36	8.13	8.59	2.05	2.02	ns
	-2	0.49	7.54	0.03	0.90	0.32	7.13	7.54	1.80	1.77	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



Pin Descriptions

Supply Pins

GND Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND. Note: In FG256, FG484, and FG676 packages, GNDQ and GND pins are connected within the package and are labeled as GND pins in the respective package pin assignment tables.

ADCGNDREF Analog Reference Ground

Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.

GNDA Ground (analog)

Quiet ground supply voltage to the Analog Block of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation.

GNDAQ Ground (analog quiet)

Quiet ground supply voltage to the analog I/O of Fusion devices. The use of a separate analog ground helps isolate the analog functionality of the Fusion device from any digital switching noise. A 0.2 V maximum differential voltage between GND and GNDA/GNDQ should apply to system implementation. Note: In FG256, FG484, and FG676 packages, GNDAQ and GNDA pins are connected within the package and are labeled as GNDA pins in the respective package pin assignment tables.

GNDNVM Flash Memory Ground

Ground supply used by the Fusion device's flash memory block module(s).

GNDOSC Oscillator Ground

Ground supply for both integrated RC oscillator and crystal oscillator circuit.

VCC15A Analog Power Supply (1.5 V)

1.5 V clean analog power supply input for use by the 1.5 V portion of the analog circuitry.

VCC33A Analog Power Supply (3.3 V)

3.3 V clean analog power supply input for use by the 3.3 V portion of the analog circuitry.

VCC33N Negative 3.3 V Output

This is the -3.3 V output from the voltage converter. A 2.2 μ F capacitor must be connected from this pin to ground.

VCC33PMP Analog Power Supply (3.3 V)

3.3 V clean analog power supply input for use by the analog charge pump. To avoid high current draw, VCC33PMP should be powered up simultaneously with or after VCC33A.

VCCNVM Flash Memory Block Power Supply (1.5 V)

1.5 V power supply input used by the Fusion device's flash memory block module(s). To avoid high current draw, VCC should be powered up before or simultaneously with VCCNVM.

VCCOSC Oscillator Power Supply (3.3 V)

Power supply for both integrated RC oscillator and crystal oscillator circuit. The internal 100 MHz oscillator, powered by the VCCOSC pin, is needed for device programming, operation of the VDDN33 pump, and eNVM operation. VCCOSC is off only when VCCA is off. VCCOSC must be powered whenever the Fusion device needs to function.

ATRTNx Temperature Monitor Return

AT returns are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is one analog return pin for every two Analog Quads. The x in the ATRTNx designator indicates the quad pairing (x = 0 for AQ1 and AQ2, x = 1 for AQ2 and AQ3, ..., x = 4 for AQ8 and AQ9). The signals that drive these pins are called out as ATRETURNxy in the software (where x and y refer to the quads that share the return signal). ATRTN is internally connected to ground. It can be left floating when it is unused. The maximum capacitance allowed across the AT pins is 500 pF.

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-22.

Refer to the "User I/O Naming Convention" section on page 2-158 for a description of naming of global pins.

JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device.

Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pullup/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements. Refer to Table 2-183 for more information.

VJTAG	Tie-Off Resistance ^{2, 3}
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Table 2-183 • Recommended Tie-Off Values for the TCK and TRST Pins

Notes:

- 1. Equivalent parallel resistance if more than one device is on JTAG chain.
- 2. The TCK pin can be pulled up/down.
- 3. The TRST pin can only be pulled down.

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

XTAL2 Crystal Oscillator Circuit Input

Input to crystal oscillator circuit. Pin for connecting external crystal, ceramic resonator, RC network, or external clock input. When using an external crystal or ceramic oscillator, external capacitors are also recommended (Please refer to the crystal oscillator manufacturer for proper capacitor value).

If using external RC network or clock input, XTAL1 should be used and XTAL2 left unconnected. In the case where the Crystal Oscillator block is not used, the XTAL1 pin should be connected to GND and the XTAL2 pin should be left floating.

Security

Fusion devices have a built-in 128-bit AES decryption core. The decryption core facilitates highly secure, in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently from each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a security-protected programming environment (such as the Microsemi in-house programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late stage product changes or personalization can be implemented easily and with high level security by simply sending a STAPL file with AES-encrypted data. Highly secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data. For more information, refer to the *Fusion Security* application note.

128-Bit AES Decryption

The 128-bit AES standard (FIPS-197) block cipher is the National Institute of Standards and Technology (NIST) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4 × 10³⁸ possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (protected with security) in Fusion devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of Fusion devices remain as secure as possible.

AES decryption can also be used on the 1,024-bit FlashROM to allow for remote updates of the FlashROM contents. This allows for easy support of subscription model products and protects them with measures designed to provide the highest level of security available. See the application note *Fusion Security* for more details.

AES for Flash Memory

AES decryption can also be used on the flash memory blocks. This provides the best available security during update of the flash memory blocks. During runtime, the encrypted data can be clocked in via the JTAG interface. The data can be passed through the internal AES decryption engine, and the decrypted data can then be stored in the flash memory block.

Programming

Programming can be performed using various programming tools, such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Microsemi).

The user can generate STP programming files from the Designer software and can use these files to program a device.

Fusion devices can be programmed in-system. During programming, VCCOSC is needed in order to power the internal 100 MHz oscillator. This oscillator is used as a source for the 20 MHz oscillator that is used to drive the charge pump for programming.



The 1.76 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{ja(total)} = \frac{T_J - T_A}{P} = \frac{100^{\circ}C - 70^{\circ}C}{3.00 W} = 10.00^{\circ}C/W$$

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{\text{JA(TOTAL)}} = \theta_{\text{JC}} + \theta_{\text{CS}} + \theta_{\text{SA}}$$

EQ 8

EQ 7

where

- $\theta_{JA} = 0.37^{\circ}C/W$
 - Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer

 θ_{SA} = Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 13.33^{\circ}C/W - 8.28^{\circ}C/W - 0.37^{\circ}C/W = 5.01^{\circ}C/W$$

A heat sink with a thermal resistance of 5.01°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an Microsemi FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 3-7 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V)

Array Voltage	Junction Temperature (°C)								
VCC (V)	–40°C	0°C	25°C	70°C	85°C	100°C			
1.425	0.88	0.93	0.95	1.00	1.02	1.05			
1.500	0.83	0.88	0.90	0.95	0.96	0.99			
1.575	0.80	0.85	0.87	0.91	0.93	0.96			

Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC8 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³
Applicable to Pro I/O Banks				
Single-Ended				
3.3 V LVTTL/LVCMOS	35	3.3	-	474.70
2.5 V LVCMOS	35	2.5	-	270.73
1.8 V LVCMOS	35	1.8	-	151.78
1.5 V LVCMOS (JESD8-11)	35	1.5	-	104.55
3.3 V PCI	10	3.3	-	204.61
3.3 V PCI-X	10	3.3	-	204.61
Voltage-Referenced	•	•		
3.3 V GTL	10	3.3	-	24.08
2.5 V GTL	10	2.5	-	13.52
3.3 V GTL+	10	3.3	-	24.10
2.5 V GTL+	10	2.5	-	13.54
HSTL (I)	20	1.5	7.08	26.22
HSTL (II)	20	1.5	13.88	27.22
SSTL2 (I)	30	2.5	16.69	105.56
SSTL2 (II)	30	2.5	25.91	116.60
SSTL3 (I)	30	3.3	26.02	114.87
SSTL3 (II)	30	3.3	42.21	131.76
Differential	•	•		
LVDS	-	2.5	7.70	89.62
LVPECL	-	3.3	19.42	168.02
Applicable to Advanced I/O Ban	ks	•		
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	-	468.67
2.5 V LVCMOS	35	2.5	-	267.48
1.8 V LVCMOS	35	1.8	-	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	-	103.12
3.3 V PCI	10	3.3	-	201.02
3.3 V PCI-X	10	3.3	-	201.02

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.

2. PDC8 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.



RC Oscillator Dynamic Contribution—**P**_{RC-OSC}

Operating Mode

P_{RC-OSC} = PAC19

Standby Mode and Sleep Mode

 $P_{RC-OSC} = 0 W$

Analog System Dynamic Contribution—P_{AB}

Operating Mode

P_{AB} = PAC20

Standby Mode and Sleep Mode

 $P_{AB} = 0 W$

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 3-16 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α ₂	I/O buffer toggle rate	10%

Table 3-17 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β ₁	I/O output buffer enable rate	100%
β ₂	RAM enable rate for read operations	12.5%
β ₃	RAM enable rate for write operations	12.5%
β ₄	NVM enable rate for read operations	0%

FG484		FG484			
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
B5	IO05NDB0V0	IO04NDB0V0	C18	VCCIB1	VCCIB1
B6	IO05PDB0V0	IO04PDB0V0	C19	VCOMPLB	VCOMPLB
B7	GND	GND	C20	GBA2/IO30PDB2V0	GBA2/IO44PDB2V0
B8	IO10NDB0V1	IO09NDB0V1	C21	NC	IO48PSB2V0
B9	IO13PDB0V1	IO11PDB0V1	C22	GBB2/IO31PDB2V0	GBB2/IO45PDB2V0
B10	GND	GND	D1	IO82NDB4V0	IO121NDB4V0
B11	IO17NDB1V0	IO24NDB1V0	D2	GND	GND
B12	IO18NDB1V0	IO26NDB1V0	D3	IO83NDB4V0	IO123NDB4V0
B13	GND	GND	D4	GAC2/IO83PDB4V0	GAC2/IO123PDB4V0
B14	IO21NDB1V0	IO31NDB1V1	D5	GAA2/IO85PDB4V0	GAA2/IO125PDB4V0
B15	IO21PDB1V0	IO31PDB1V1	D6	GAC0/IO03NDB0V0	GAC0/IO03NDB0V0
B16	GND	GND	D7	GAC1/IO03PDB0V0	GAC1/IO03PDB0V0
B17	GBC1/IO26PDB1V1	GBC1/IO40PDB1V2	D8	IO09NDB0V1	IO10NDB0V1
B18	GBA1/IO28PDB1V1	GBA1/IO42PDB1V2	D9	IO09PDB0V1	IO10PDB0V1
B19	GND	GND	D10	IO11NDB0V1	IO14NDB0V2
B20	VCCPLB	VCCPLB	D11	IO16NDB1V0	IO23NDB1V0
B21	GND	GND	D12	IO16PDB1V0	IO23PDB1V0
B22	VCC	NC	D13	NC	IO32NPB1V1
C1	IO82PDB4V0	IO121PDB4V0	D14	IO23NDB1V1	IO34NDB1V1
C2	NC	IO122PSB4V0	D15	IO23PDB1V1	IO34PDB1V1
C3	IO00NDB0V0	IO00NDB0V0	D16	IO25PDB1V1	IO37PDB1V2
C4	IO00PDB0V0	IO00PDB0V0	D17	GBB1/IO27PDB1V1	GBB1/IO41PDB1V2
C5	VCCIB0	VCCIB0	D18	VCCIB2	VCCIB2
C6	IO06NDB0V0	IO05NDB0V1	D19	NC	IO47PPB2V0
C7	IO06PDB0V0	IO05PDB0V1	D20	IO30NDB2V0	IO44NDB2V0
C8	VCCIB0	VCCIB0	D21	GND	GND
C9	IO13NDB0V1	IO11NDB0V1	D22	IO31NDB2V0	IO45NDB2V0
C10	IO11PDB0V1	IO14PDB0V2	E1	IO81NDB4V0	IO120NDB4V0
C11	VCCIB0	VCCIB0	E2	IO81PDB4V0	IO120PDB4V0
C12	VCCIB1	VCCIB1	E3	VCCIB4	VCCIB4
C13	IO20NDB1V0	IO29NDB1V1	E4	GAB2/IO84PDB4V0	GAB2/IO124PDB4V0
C14	IO20PDB1V0	IO29PDB1V1	E5	IO85NDB4V0	IO125NDB4V0
C15	VCCIB1	VCCIB1	E6	GND	GND
C16	IO25NDB1V1	IO37NDB1V2	E7	VCCIB0	VCCIB0
C17	GBB0/IO27NDB1V1	GBB0/IO41NDB1V2	E8	NC	IO08NDB0V1

Fusion Family of Mixed Signal FPGAs

Revision	Changes	Page
Advance 1.0 (continued)	In Table 2-47 • ADC Characteristics in Direct Input Mode, the commercial conditions were updated and note 2 is new.	2-121
	The V_{CC33ACAP} signal name was changed to "XTAL1 Crystal Oscillator Circuit Input".	2-228
	Table 2-48 • Uncalibrated Analog Channel Accuracy* is new.	2-123
	Table 2-49 • Calibrated Analog Channel Accuracy ^{1,2,3} is new.	2-124
	Table 2-50 • Analog Channel Accuracy: Monitoring Standard Positive Voltages is new.	2-125
	In Table 2-57 • Voltage Polarity Control Truth Table—AV ($x = 0$), AC ($x = 1$), and AT ($x = 3$)*, the following I/O Bank names were changed:	2-131
	Hot-Swap changed to Standard	
	LVDS changed to Advanced	
	In Table 2-58 • Prescaler Op Amp Power-Down Truth Table—AV ($x = 0$), AC ($x = 1$), and AT ($x = 3$), the following I/O Bank names were changed:	2-132
	Hot-Swap changed to Standard	
	In the title of Table 2.64 - 1/O Standards Supported by Dark Tures, IV/DS 1/O uses	0.404
	changed to Advanced I/O.	2-134
	The title was changed from "Fusion Standard, LVDS, and Standard plus Hot-Swap I/O" to Table 2-68 • Fusion Standard and Advanced I/O Features. In addition, the table headings were all updated. The heading used to be Standard and LVDS I/O and was changed to Advanced I/O. Standard Hot-Swap was changed to just Standard.	2-136
	 This sentence was deleted from the "Slew Rate Control and Drive Strength" section: The Standard hot-swap I/Os do not support slew rate control. In addition, these references were changed: From: Fusion hot-swap I/O (Table 2-69 on page 2-122) To: Fusion Standard I/O From: Fusion LVDS I/O (Table 2-70 on page 2-122) To: Fusion Advanced I/O 	2-152
	The "Cold-Sparing Support" section was significantly updated.	2-143
	In the title of Table 2-75 • Fusion Standard I/O Standards—OUT_DRIVE Settings, Hot-Swap was changed to Standard.	2-153
	In the title of Table 2-76 • Fusion Advanced I/O Standards—SLEW and OUT_DRIVE Settings, LVDS was changed to Advanced.	2-153
	In the title of Table 2-81 • Fusion Standard and Advanced I/O Attributes vs. I/O Standard Applications, LVDS was changed to Advanced.	2-157
	In Figure 2-111 • Naming Conventions of Fusion Devices with Three Digital I/O Banks and Figure 2-112 • Naming Conventions of Fusion Devices with Four I/O Banks the following names were changed: Hot-Swap changed to Standard	2-160
	LVDS changed to Advanced	
	The Figure 2-113 • Timing Model was updated.	2-161
	In the notes for Table 2-86 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions, T_J was changed to T_A .	2-166



Datasheet Information

Revision	Changes	Page
Advance v0.5	The low power modes of operation were updated and clarified.	N/A
(June 2006)	The AFS1500 digital I/O count was updated in Table 1 • Fusion Family.	i
	The AFS1500 digital I/O count was updated in the "Package I/Os: Single-/Double- Ended (Analog)" table.	
	The "Voltage Regulator Power Supply Monitor (VRPSM)" was updated.	2-36
	Figure 2-45 • FlashROM Timing Diagram was updated.	2-53
	The "256-Pin FBGA" table for the AFS1500 is new.	
Advance v0.4 (April 2006)	The G was moved in the "Product Ordering Codes" section.	III
Advance v0.3	The "Features and Benefits" section was updated.	I
(April 2006)	The "Fusion Family" table was updated.	
	The "Package I/Os: Single-/Double-Ended (Analog)" table was updated.	
	The "Product Ordering Codes" table was updated.	Ш
	The "Temperature Grade Offerings" table was updated.	IV
	The "General Description" section was updated to include ARM information.	1-1
	Figure 2-46 • FlashROM Timing Diagram was updated.	2-58
	The "FlashROM" section was updated.	2-57
	The "RESET" section was updated.	2-61
	The "RESET" section was updated.	2-64
	Figure 2-27 · Real-Time Counter System was updated.	2-35
	Table 2-19 • Flash Memory Block Pin Names was updated.	2-43
	Figure 2-33 • Flash Memory Block Diagram was updated to include AUX block information.	2-45
	Figure 2-34 • Flash Memory Block Organization was updated to include AUX block information.	2-46
	The note in the "Program Operation" section was updated.	2-48
	Figure 2-76 • Gate Driver Example was updated.	2-95
	The "Analog Quad ACM Description" section was updated.	2-130
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94
	Figure 2-65 • Analog Block Macro was updated.	2-81
	Figure 2-65 • Analog Block Macro was updated.	2-81
	The "Analog Quad" section was updated.	2-84
	The "Voltage Monitor" section was updated.	2-86
	The "Direct Digital Input" section was updated.	2-89
	The "Current Monitor" section was updated.	2-90
	Information about the maximum pad input frequency was added to the "Gate Driver" section.	2-94