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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	93
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m1afs250-pqg208i

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PLL Macro

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[2:0] package pins. Refer to Figure 2-22 on page 2-25 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL feedback loop can be driven either internally or externally. The PLL macro also provides power-down input and lock output signals. During power-up, POWERDOWN should be asserted Low until VCC is up. See Figure 2-19 on page 2-23 for more information.

Inputs:

- · CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is power-down on (active low).

Outputs:

- LOCK (active high): indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-23 on page 2-26 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global networks, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate it from the hardwired I/O connection described earlier.

The visual PLL configuration in SmartGen, available with the Libero SoC and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select where the input clock is coming from. SmartGen automatically instantiates the special macro, PLLINT, when needed.







Figure 2-31 • State Diagram for All Different Power Modes

When TRST is 1 or PUB is 0, the 1.5 V voltage regulator is always ON, putting the Fusion device in normal operation at all times. Therefore, when the JTAG port is not in reset, the Fusion device cannot enter sleep mode or standby mode.

To enter standby mode, the Fusion device must first power-up into normal operation. The RTC is enabled through the RTC Control/Status Register described in the "Real-Time Counter (part of AB macro)" section on page 2-33. A match value corresponding to the wake-up time is loaded into the Match Register. The 1.5 V voltage regulator is disabled by setting VRPU to 0 to allow the Fusion device to enter standby mode, when the 1.5 V supply is off but the RTC remains on.

Read Next Operation

The Read Next operation is a feature by which the next block relative to the block in the Block Buffer is read from the FB Array while performing reads from the Block Buffer. The goal is to minimize wait states during consecutive sequential Read operations.

The Read Next operation is performed in a predetermined manner because it does look-ahead reads. The general look-ahead function is as follows:

- Within a page, the next block fetched will be the next in linear address.
- When reading the last data block of a page, it will fetch the first block of the next page.
- When reading spare pages, it will read the first block of the next sector's spare page.
- Reads of the last sector will wrap around to sector 0.
- · Reads of Auxiliary blocks will read the next linear page's Auxiliary block.

When an address on the ADDR input does not agree with the predetermined look-ahead address, there is a time penalty for this access. The FB will be busy finishing the current look-ahead read before it can start the next read. The worst case is a total of nine BUSY cycles before data is delivered.

The Non-Pipe Mode and Pipe Mode waveforms for Read Next operations are illustrated in Figure 2-40 and Figure 2-41.



Figure 2-40 • Read Next Waveform (Non-Pipe Mode, 32-bit access)



Figure 2-41 • Read Next WaveForm (Pipe Mode, 32-bit access)



Unprotect Page Operation

An Unprotect Page operation will clear the protection for a page addressed on the ADDR input. It is initiated by setting the UNPROTECTPAGE signal on the interface along with the page address on ADDR.

If the page is not in the Page Buffer, the Unprotect Page operation will copy the page into the Page Buffer. The Copy Page operation occurs only if the current page in the Page Buffer is not Page Loss Protected.

The waveform for an Unprotect Page operation is shown in Figure 2-42.



Figure 2-42 • FB Unprotected Page Waveform

The Unprotect Page operation can incur the following error conditions:

- 1. If the copy of the page to the Page Buffer determines that the page has a single-bit correctable error in the data, it will report a STATUS = '01'.
- 2. If the address on ADDR does not match the address of the Page Buffer, PAGELOSSPROTECT is asserted, and the Page Buffer has been modified, then STATUS = '11' and the addressed page is not loaded into the Page Buffer.
- 3. If the copy of the page to the Page Buffer determines that at least one block in the page has a double-bit uncorrectable error, STATUS = '10' and the Page Buffer will contain the corrupted data.

Discard Page Operation

If the contents of the modified Page Buffer have to be discarded, the DISCARDPAGE signal should be asserted. This command results in the Page Buffer being marked as unmodified.

The timing for the operation is shown in Figure 2-43. The BUSY signal will remain asserted until the operation has completed.



Figure 2-43 • FB Discard Page Waveform



Figure 2-72 • Positive Current Monitor

Care must be taken when choosing the right resistor for current measurement application. Note that because of the 10× amplification, the maximum measurable difference between the AV and AC pads is V_{AREF} / 10. A larger AV-to-AC voltage drop will result in ADC saturation; that is, the digital code put out by the ADC will stay fixed at the full scale value. Therefore, the user must select the external sense resistor appropriately. Table 2-38 shows recommended resistor values for different current measurement ranges. When choosing resistor values for a system, there is a trade-off between measurement accuracy and power consumption. Choosing a large resistor will increase the voltage drop and hence increase accuracy of the measurement; however the larger voltage drop dissipates more power (P = I² × R).

The Current Monitor is a unipolar system, meaning that the differential voltage swing must be from 0 V to $V_{AREF}/10$. Therefore, the Current Monitor only supports differential voltage where $|V_{AV}-V_{AC}|$ is greater than 0 V. This results in the requirement that the potential of the AV pad must be larger than the potential of the AC pad. This is straightforward for positive voltage systems. For a negative voltage system, it means that the AV pad must be "more negative" than the AC pad. This is shown in Figure 2-73.

In this case, both the AV pad and the AC pad are configured for negative operations and the output of the differential amplifier still falls between 0 V and V_{AREF} as required.

Current Range	Recommended Minimum Resistor Value (Ohms)
> 5 mA – 10 mA	10 – 20
> 10 mA – 20 mA	5 – 10
> 20 mA – 50 mA	2.5 – 5
> 50 mA – 100 mA	1 – 2
> 100 mA – 200 mA	0.5 – 1
> 200 mA – 500 mA	0.3 – 0.5
> 500 mA – 1 A	0.1 – 0.2
> 1 A – 2 A	0.05 – 0.1
> 2 A – 4 A	0.025 – 0.05
> 4 A – 8 A	0.0125 – 0.025
> 8 A – 12 A	0.00625 – 0.02

Table 2-37 • Recommended Resistor for Different Current Range Measurement



Analog Quad ACM Description

Table 2-56 maps out the ACM space associated with configuration of the Analog Quads within the Analog Block. Table 2-56 shows the byte assignment within each quad and the function of each bit within each byte. Subsequent tables will explain each bit setting and how it corresponds to a particular configuration. After 3.3 V and 1.5 V are applied to Fusion, Analog Quad configuration registers are loaded with default settings until the initialization and configuration state machine changes them to user-defined settings.

Table	2-56 •	Analog	Quad	Bvte /	Assianme	nt
1 4010	200	Analog	auuu .		Rooiginno	

Byte	Bit	Signal (Bx)	Function	Default Setting	
Byte 0	0	B0[0]	Scaling factor control – prescaler	Highest voltage range	
(AV)	1	B0[1]			
	2	B0[2]	-		
	3	B0[3]	Analog MUX select	Prescaler	
	4	B0[4]	Current monitor switch	Off	
	5	B0[5]	Direct analog input switch	Off	
	6	B0[6]	Selects V-pad polarity	Positive	
	7	B0[7]	Prescaler op amp mode	Power-down	
Byte 1	0	B1[0]	Scaling factor control – prescaler	Highest voltage range	
(AC)	1	B1[1]			
	2	B1[2]			
	3	B1[3]	Analog MUX select	Prescaler	
	4	B1[4]			
	5	B1[5]	Direct analog input switch	Off	
	6	B1[6]	Selects C-pad polarity	Positive	
	7	B1[7]	Prescaler op amp mode	Power-down	
Byte 2	0	B2[0]	Internal chip temperature monitor *	Off	
(AG)	1	B2[1]	Spare	-	
	2	B2[2]	Current drive control	Lowest current	
	3	B2[3]			
	4	B2[4]	Spare	-	
	5	B2[5]	Spare	-	
	6	B2[6]	Selects G-pad polarity	Positive	
	7	B2[7]	Selects low/high drive	Low drive	
Byte 3	0	B3[0]	Scaling factor control – prescaler	Highest voltage range	
(AT)	1	B3[1]	-		
	2	B3[2]	-		
	3	B3[3]	Analog MUX select	Prescaler	
	4	B3[4]			
	5	B3[5]	Direct analog input switch	Off	
	6	B3[6]	_	-	
	7	B3[7]	Prescaler op amp mode	Power-down	

Note: *For the internal temperature monitor to function, Bit 0 of Byte 2 for all 10 Quads must be set.

Table 2-68 • I/O Bank Support by Device

I/O Bank	AFS090	AFS250	AFS600	AFS1500
Standard I/O	Ν	Ν	_	-
Advanced I/O	E, W	E, W	E, W	E, W
Pro I/O	-	_	Ν	Ν
Analog Quad	S	S	S	S

Note: E = *East side of the device*

W = West side of the device

N = North side of the device

S = South side of the device

Table 2-69 • Fusion VCCI Voltages and Compatible Standards

VCCI (typical)	Compatible Standards
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, SSTL3 (Class I and II),* GTL+ 3.3, GTL 3.3,* LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, SSTL2 (Class I and II),* GTL+ 2.5,* GTL 2.5,* LVDS, BLVDS, M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I),* HSTL (Class II)*

Note: *I/O standard supported by Pro I/O banks.

Table 2-70 • Fusion VREF Voltages and Compatible Standards*

VREF (typical)	Compatible Standards
1.5 V	SSTL3 (Class I and II)
1.25 V	SSTL2 (Class I and II)
1.0 V	GTL+ 2.5, GTL+ 3.3
0.8 V	GTL 2.5, GTL 3.3
0.75 V	HSTL (Class I), HSTL (Class II)

Note: *I/O standards supported by Pro I/O banks.





Result: No Bus Contention

Figure 2-112 • Timing Diagram (with skew circuit selected)

Weak Pull-Up and Weak Pull-Down Resistors

Fusion devices support optional weak pull-up and pull-down resistors for each I/O pin. When the I/O is pulled up, it is connected to the VCCI of its corresponding I/O bank. When it is pulled down, it is connected to GND. Refer to Table 2-97 on page 2-171 for more information.

Slew Rate Control and Drive Strength

Fusion devices support output slew rate control: high and low. The high slew rate option is recommended to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V, 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

For Fusion slew rate and drive strength specifications, refer to the appropriate I/O bank table:

- Fusion Standard I/O (Table 2-78 on page 2-152)
- Fusion Advanced I/O (Table 2-79 on page 2-152)
- Fusion Pro I/O (Table 2-80 on page 2-152)

Table 2-83 on page 2-155 lists the default values for the above selectable I/O attributes as well as those that are preset for each I/O standard.

Refer to Table 2-78, Table 2-79, and Table 2-80 on page 2-152 for SLEW and OUT_DRIVE settings. Table 2-81 on page 2-153 and Table 2-82 on page 2-154 list the I/O default attributes. Table 2-83 on page 2-155 lists the voltages for the supported I/O standards.



I/O Standard	Input/Output Supply Voltage (VCCI_TYP)	Input Reference Voltage (VREF_TYP)	Board Termination Voltage (VTT_TYP)
LVTTL/LVCMOS 3.3 V	3.30 V	-	-
LVCMOS 2.5 V	2.50 V	-	-
LVCMOS 2.5 V / 5.0 V Input	2.50 V	-	-
LVCMOS 1.8 V	1.80 V	-	-
LVCMOS 1.5 V	1.50 V	-	-
PCI 3.3 V	3.30 V	-	-
PCI-X 3.3 V	3.30 V	-	-
GTL+ 3.3 V	3.30 V	1.00 V	1.50 V
GTL+ 2.5 V	2.50 V	1.00 V	1.50 V
GTL 3.3 V	3.30 V	0.80 V	1.20 V
GTL 2.5 V	2.50 V	0.80 V	1.20 V
HSTL Class I	1.50 V	0.75 V	0.75 V
HSTL Class II	1.50 V	0.75 V	0.75 V
SSTL3 Class I	3.30 V	1.50 V	1.50 V
SSTL3 Class II	3.30 V	1.50 V	1.50 V
SSTL2 Class I	2.50 V	1.25 V	1.25 V
SSTL2 Class II	2.50 V	1.25 V	1.25 V
LVDS, BLVDS, M-LVDS	2.50 V	-	-
LVPECL	3.30 V	_	-

Table 2-83 • Fusion Pro I/O Supported Standards and Corresponding VREF and VTT Voltages





Figure 2-116 • Input Buffer Timing Model and Delays (example)



Detailed I/O DC Characteristics

Table 2-95 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C _{IN}	Input capacitance	VIN = 0, f = 1.0 MHz		8	pF
C _{INCLK}	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz		8	pF

Table 2-96 • I/O Output Buffer Maximum Resistances ¹

Drive Strength	R _{PULL-DOWN} (ohms) ²	R _{PULL-UP} (ohms) ³
4 mA	100	300
8 mA	50	150
12 mA	25	75
16 mA	17	50
24 mA	11	33
4 mA	100	200
8 mA	50	100
12 mA	25	50
16 mA	20	40
24 mA	11	22
2 mA	200	225
4 mA	100	112
6 mA	50	56
8 mA	50	56
12 mA	20	22
16 mA	20	22
2 mA	200	224
4 mA	100	112
6 mA	67	75
8 mA	33	37
12 mA	33	37
Per PCI/PCI-X specification	25	75
20 mA	11	-
20 mA	14	-
35 mA	12	-
33 mA	15	_
	Drive Strength 4 mA 8 mA 12 mA 16 mA 24 mA 4 mA 8 mA 12 mA 16 mA 24 mA 4 mA 8 mA 12 mA 16 mA 24 mA 6 mA 8 mA 112 mA 16 mA 2 mA 4 mA 6 mA 8 mA 12 mA 16 mA 8 mA 12 mA 12 mA 13 mA Per PCI/PCI-X specification 20 mA 35 mA 33 mA	Drive Strength "PULL-DOWN (ohms) 2" 4 mA 100 8 mA 50 12 mA 25 16 mA 17 24 mA 11 4 mA 100 8 mA 50 12 mA 25 16 mA 11 4 mA 100 8 mA 50 12 mA 25 16 mA 20 24 mA 11 2 mA 200 4 mA 100 6 mA 50 12 mA 20 16 mA 20 2 mA 200 4 mA 100 6 mA 50 12 mA 20 2 mA 200 4 mA 100 6 mA 67 8 mA 33 12 mA 33 Per PCI/PCI-X specification 25 20 mA 11 20 mA 14 <

Notes:

 These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.

2. R_(PULL-DOWN-MAX) = VOLspec / I_{OLspec}

3. R_(PULL-UP-MAX) = (VCCImax – VOHspec) / IOHspec



3.3 V GTL+

Gunning Transceiver Logic Plus is a high-speed bus standard (JESD8-3). It provides a differential amplifier input buffer and an open-drain output buffer. The VCCI pin should be connected to 3.3 V.

Table 2-144 • Minimum and Maximum DC Input and Output Levels

3.3 V GTL+		VIL	VIH		VOL	VOH	IOL	ЮН	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
35 mA	-0.3	VREF – 0.1	VREF + 0.1	3.6	0.6	-	35	35	181	268	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.



Figure 2-126 • AC Loading

Table	2-145	AC Wavef	orms. Meas	suring Poin	ts, and Ca	pacitive Loads
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Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C _{LOAD} (pF)	
VREF – 0.1	VREF + 0.1	1.0	1.0	1.5	10	

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-146 • 3.3 V GTL+

Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V, VREF = 1.0 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	2.06	0.04	1.59	0.43	2.09	2.06			4.33	4.29	ns
-1	0.56	1.75	0.04	1.35	0.36	1.78	1.75			3.68	3.65	ns
-2	0.49	1.53	0.03	1.19	0.32	1.56	1.53			3.23	3.20	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.



LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-136. The building blocks of the LVPECL transmitter–receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.



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FIGHTE Z=1.30 • 1 VPFL.1	CITCUU DIAOFAM AND BOAFO-LE	vei impiementation
1 IYUIC 2-130 ° LVFLOL	Circuit Diagram and Doard-Le	

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3	.0	3	.3	3.	6	V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-171 • Minimum and Maximum DC Input and Output Levels

Table 2-172 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	
1.64	1.94	Cross point	_	

Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.

Timing Characteristics

Table 2-173 • LVPECL

Commercial Temperature Range Conditions: $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Pro I/Os

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	Units
Std.	0.66	2.14	0.04	1.63	ns
-1	0.56	1.82	0.04	1.39	ns
-2	0.49	1.60	0.03	1.22	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.





Figure	2-145 •	Output DDR	Timing	Diagram

Timing Characteristics

Table 2-182 • Output DDR Propagation Delays	
Commercial Temperature Range Conditions: T ₁ = 70°C, Worst-Case VCC = 1.425 V	

Parameter	Description	-2	-1	Std.	Units
t _{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.70	0.80	0.94	ns
t _{DDROSUD1}	Data_F Data Setup for Output DDR	0.38	0.43	0.51	ns
t _{DDROSUD2}	Data_R Data Setup for Output DDR	0.38	0.43	0.51	ns
t _{DDROHD1}	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
t _{DDROHD2}	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
t _{DDROCLR2Q}	Asynchronous Clear-to-Out for Output DDR	0.80	0.91	1.07	ns
t _{DDROREMCLR}	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
t _{DDRORECCLR}	Asynchronous Clear Recovery Time for Output DDR	0.22	0.25	0.30	ns
t _{DDROWCLR1}	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
t _{DDROCKMPWH}	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
t _{DDROCKMPWL}	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
F _{DDOMAX}	Maximum Frequency for the Output DDR	1404	1232	1048	MHz

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Parameter	Description	Conditions	Temp.	Min	Тур	Мах	Unit
ICC ¹	1.5 V quiescent current	Operational standby ⁴ ,	T _J = 25°C		13	25	mA
		VCC = 1.575 V	T _J = 85°C		20	45	mA
			T _J =100°C		25	75	mA
		Standby mode ⁵ or Sleep mode ⁶ , VCC = 0 V			0	0	μA
ICC33 ²	3.3 V analog supplies	Operational standby ⁴ ,	T _J = 25°C		9.8	13	mA
	current	VCC33 = 3.63 V	T _J = 85°C		10.7	14	mA
			T _J = 100°C		10.8	15	mA
		Operational standby,	T _J = 25°C		0.31	2	mA
		only Analog Quad and -3.3 V output ON. VCC33 = 3.63 V	T _J = 85°C		0.35	2	mA
			T _J = 100°C		0.45	2	mA
		Standby mode ⁵ , VCC33 = 3.63 V	T _J = 25°C		2.8	3.6	mA
			T _J = 85°C		2.9	4	mA
			T _J = 100°C		3.5	6	mA
		Sleep mode ⁶ , V _{CC33} = 3.63 V	T _J = 25°C		17	19	μA
			T _J = 85°C		18	20	μA
			T _J = 100°C		24	25	μA
ICCI ³	I/O quiescent current	Operational standby ⁴ ,	T _J = 25°C		417	648	μA
		VCCIX = 3.63 V	T _J = 85°C		417	648	μA
			T _J = 100°C		417	649	μA
IJTAG	JTAG I/O quiescent current	Operational standby ⁴ ,	T _J = 25°C		80	100	μA
		VJ1AG = 3.63 V	T _J = 85°C		80	100	μA
			T _J = 100°C		80	100	μA
		Standby mode ⁵ or Sleep mode ⁶ , VJTAG = 0 V			0	0	μA

Table 3-9 •	AFS600 Quiescent Supply Current Characteristics
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Notes:

1. ICC is the 1.5 V power supplies, ICC and ICC15A.

2. ICC33A includes ICC33A, ICC33PMP, and ICCOSC.

3. ICCI includes all ICCI0, ICCI1, ICCI2, and ICCI4.

4. Operational standby is when the Fusion device is powered up, all blocks are used, no I/O is toggling, Voltage Regulator is loaded with 200 mA, VCC33PMP is ON, XTAL is ON, and ADC is ON.

5. XTAL is configured as high gain, VCC = VJTAG = VPUMP = 0 V.

6. Sleep Mode, VCC = VJTAG = VPUMP = 0 V.



Table 3-13 • Summary of I/O Output Buffer Power (per pin)—Default I/O Software Settings¹ (continued)

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC8 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³
Differential				
LVDS	-	2.5	7.74	88.92
LVPECL	_	3.3	19.54	166.52
Applicable to Standard I/O Bank	s			
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	-	431.08
2.5 V LVCMOS	35	2.5	-	247.36
1.8 V LVCMOS	35	1.8	-	128.46
1.5 V LVCMOS (JESD8-11)	35	1.5	-	89.46

Notes:

1. Dynamic power consumption is given for standard load and software-default drive strength and output slew.

2. PDC8 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.



QN180



Note: The die attach paddle center of the package is tied to ground (GND).

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/default.aspx.



Package Pin Assignments

PQ208			PQ208		
Pin Number	AFS250 Function	AFS600 Function	Pin Number	AFS250 Function	AFS600 Function
147	GCC1/IO47PDB1V0	IO39NDB2V0	184	IO18RSB0V0	IO10PPB0V1
148	IO42NDB1V0	GCA2/IO39PDB2V0	185	IO17RSB0V0	IO09PPB0V1
149	GBC2/IO42PDB1V0	IO31NDB2V0	186	IO16RSB0V0	IO10NPB0V1
150	VCCIB1	GBB2/IO31PDB2V0	187	IO15RSB0V0	IO09NPB0V1
151	GND	IO30NDB2V0	188	VCCIB0	IO08PPB0V1
152	VCC	GBA2/IO30PDB2V0	189	GND	IO07PPB0V1
153	IO41NDB1V0	VCCIB2	190	VCC	IO08NPB0V1
154	GBB2/IO41PDB1V0	GNDQ	191	IO14RSB0V0	IO07NPB0V1
155	IO40NDB1V0	VCOMPLB	192	IO13RSB0V0	IO06PPB0V0
156	GBA2/IO40PDB1V0	VCCPLB	193	IO12RSB0V0	IO05PPB0V0
157	GBA1/IO39RSB0V0	VCCIB1	194	IO11RSB0V0	IO06NPB0V0
158	GBA0/IO38RSB0V0	GNDQ	195	IO10RSB0V0	IO04PPB0V0
159	GBB1/IO37RSB0V0	GBB1/IO27PPB1V1	196	IO09RSB0V0	IO05NPB0V0
160	GBB0/IO36RSB0V0	GBA1/IO28PPB1V1	197	IO08RSB0V0	IO04NPB0V0
161	GBC1/IO35RSB0V0	GBB0/IO27NPB1V1	198	IO07RSB0V0	GAC1/IO03PDB0V0
162	VCCIB0	GBA0/IO28NPB1V1	199	IO06RSB0V0	GAC0/IO03NDB0V0
163	GND	VCCIB1	200	GAC1/IO05RSB0V0	VCCIB0
164	VCC	GND	201	VCCIB0	GND
165	GBC0/IO34RSB0V0	VCC	202	GND	VCC
166	IO33RSB0V0	GBC1/IO26PDB1V1	203	VCC	GAB1/IO02PDB0V0
167	IO32RSB0V0	GBC0/IO26NDB1V1	204	GAC0/IO04RSB0V0	GAB0/IO02NDB0V0
168	IO31RSB0V0	IO24PPB1V1	205	GAB1/IO03RSB0V0	GAA1/IO01PDB0V0
169	IO30RSB0V0	IO23PPB1V1	206	GAB0/IO02RSB0V0	GAA0/IO01NDB0V0
170	IO29RSB0V0	IO24NPB1V1	207	GAA1/IO01RSB0V0	GNDQ
171	IO28RSB0V0	IO23NPB1V1	208	GAA0/IO00RSB0V0	VCCIB0
172	IO27RSB0V0	IO22PPB1V0			
173	IO26RSB0V0	IO21PPB1V0			
174	IO25RSB0V0	IO22NPB1V0			
175	VCCIB0	IO21NPB1V0			
176	GND	IO20PSB1V0			
177	VCC	IO19PSB1V0			
178	IO24RSB0V0	IO14NSB0V1			
179	IO23RSB0V0	IO12PDB0V1			
180	IO22RSB0V0	IO12NDB0V1			
181	IO21RSB0V0	VCCIB0			
182	IO20RSB0V0	GND			
183	IO19RSB0V0	VCC			



Package Pin Assignments

FG484			FG484		
Pin Number	AFS600 Function	AFS1500 Function	Pin Number	AFS600 Function	AFS1500 Function
A1	GND	GND	AA14	AG7	AG7
A2	VCC	NC	AA15	AG8	AG8
A3	GAA1/IO01PDB0V0	GAA1/IO01PDB0V0	AA16	GNDA	GNDA
A4	GAB0/IO02NDB0V0	GAB0/IO02NDB0V0	AA17	AG9	AG9
A5	GAB1/IO02PDB0V0	GAB1/IO02PDB0V0	AA18	VAREF	VAREF
A6	IO07NDB0V1	IO07NDB0V1	AA19	VCCIB2	VCCIB2
A7	IO07PDB0V1	IO07PDB0V1	AA20	PTEM	PTEM
A8	IO10PDB0V1	IO09PDB0V1	AA21	GND	GND
A9	IO14NDB0V1	IO13NDB0V2	AA22	VCC	NC
A10	IO14PDB0V1	IO13PDB0V2	AB1	GND	GND
A11	IO17PDB1V0	IO24PDB1V0	AB2	VCC	NC
A12	IO18PDB1V0	IO26PDB1V0	AB3	NC	IO94NSB4V0
A13	IO19NDB1V0	IO27NDB1V1	AB4	GND	GND
A14	IO19PDB1V0	IO27PDB1V1	AB5	VCC33N	VCC33N
A15	IO24NDB1V1	IO35NDB1V2	AB6	AT0	AT0
A16	IO24PDB1V1	IO35PDB1V2	AB7	ATRTN0	ATRTN0
A17	GBC0/IO26NDB1V1	GBC0/IO40NDB1V2	AB8	AT1	AT1
A18	GBA0/IO28NDB1V1	GBA0/IO42NDB1V2	AB9	AT2	AT2
A19	IO29NDB1V1	IO43NDB1V2	AB10	ATRTN1	ATRTN1
A20	IO29PDB1V1	IO43PDB1V2	AB11	AT3	AT3
A21	VCC	NC	AB12	AT6	AT6
A22	GND	GND	AB13	ATRTN3	ATRTN3
AA1	VCC	NC	AB14	AT7	AT7
AA2	GND	GND	AB15	AT8	AT8
AA3	VCCIB4	VCCIB4	AB16	ATRTN4	ATRTN4
AA4	VCCIB4	VCCIB4	AB17	AT9	AT9
AA5	PCAP	PCAP	AB18	VCC33A	VCC33A
AA6	AG0	AG0	AB19	GND	GND
AA7	GNDA	GNDA	AB20	NC	IO76NPB2V0
AA8	AG1	AG1	AB21	VCC	NC
AA9	AG2	AG2	AB22	GND	GND
AA10	GNDA	GNDA	B1	VCC	NC
AA11	AG3	AG3	B2	GND	GND
AA12	AG6	AG6	B3	GAA0/IO01NDB0V0	GAA0/IO01NDB0V0
AA13	GNDA	GNDA	B4	GND	GND