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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	65
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	180-WFQFN Dual Rows, Exposed Pad
Supplier Device Package	180-QFN (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/m1afs250-qng180

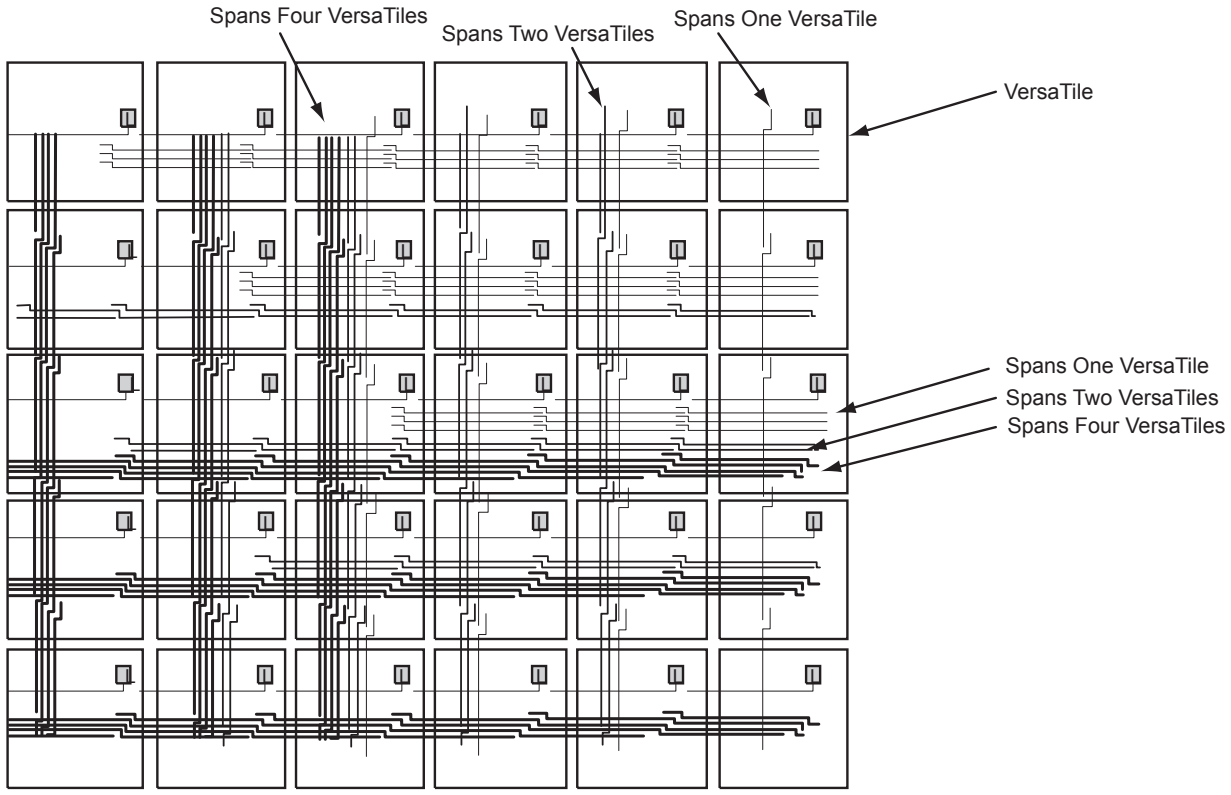

Figure 2-9 • **Efficient Long-Line Resources**

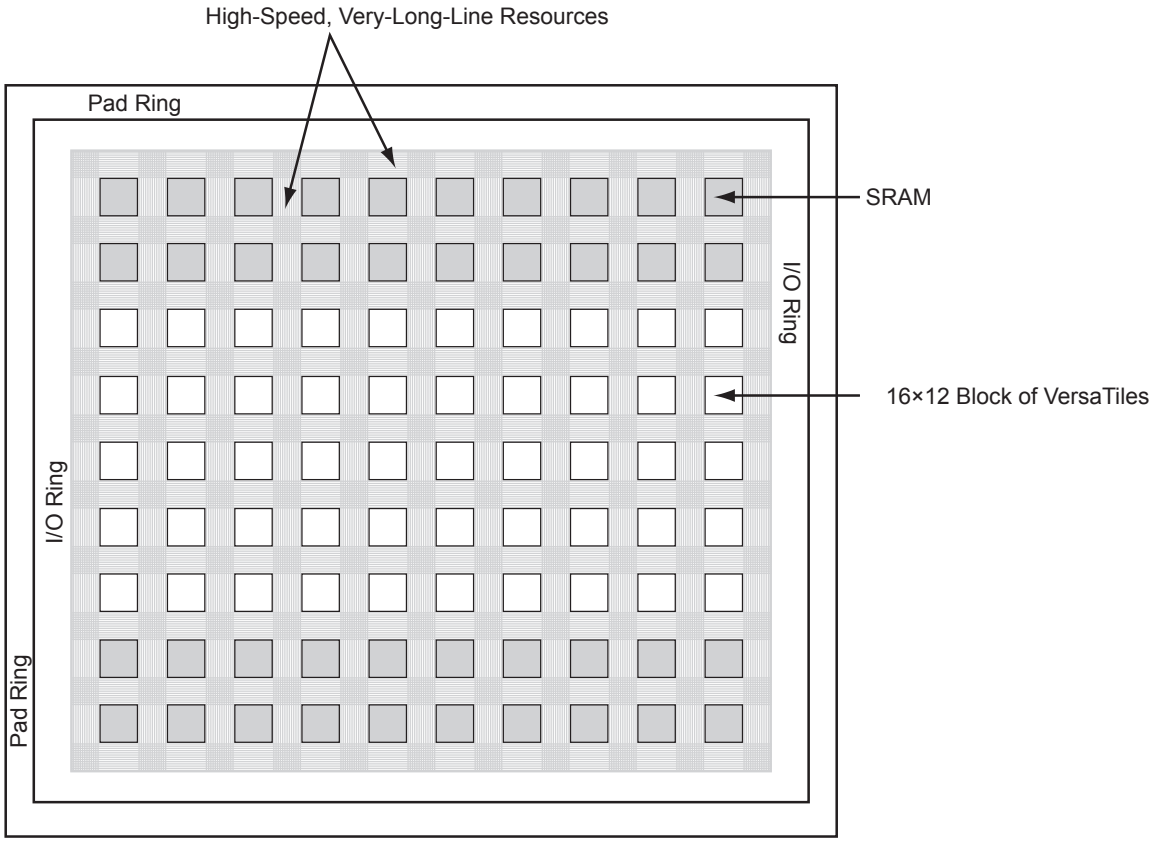

Figure 2-10 • **Very-Long-Line Resources**

Clock Conditioning Circuits

In Fusion devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations—each of the four chip corners and the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay), or a PLL function (programmable frequency division/multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, and CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and, optionally, the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used (Figure 2-19). Refer to the "PLL Macro" section on page 2-27 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the Fusion device to permit changes of parameters (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the "UJTAG Applications in Microsemi's Low-Power Flash Devices" chapter of the *Fusion FPGA Fabric User Guide* and the "CCC and PLL Characteristics" section on page 2-28 for more information.

Timing Characteristics

Table 2-35 • FIFO
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup time	1.34	1.52	1.79	ns
t_{ENH}	REN, WEN Hold time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold time	0.00	0.00	0.00	ns
t_{DS}	Input data (WD) Setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) Hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost-Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

This process results in a binary approximation of VIN. Generally, there is a fixed interval T, the sampling period, between the samples. The inverse of the sampling period is often referred to as the sampling frequency f_S = 1 / T. The combined effect is illustrated in Figure 2-82.

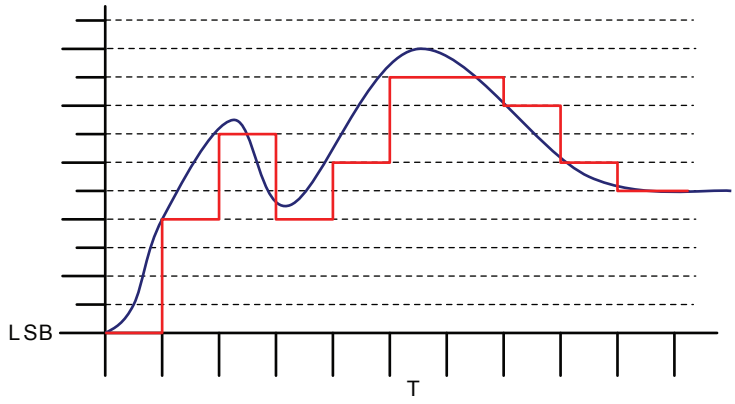

***Figure 2-82* • Conversion Example**

Figure 2-82 demonstrates that if the signal changes faster than the sampling rate can accommodate, or if the actual value of VIN falls between counts in the result, this information is lost during the conversion. There are several techniques that can be used to address these issues.

First, the sampling rate must be chosen to provide enough samples to adequately represent the input signal. Based on the Nyquist-Shannon Sampling Theorem, the minimum sampling rate must be at least twice the frequency of the highest frequency component in the target signal (Nyquist Frequency). For example, to recreate the frequency content of an audio signal with up to 22 KHz bandwidth, the user must sample it at a minimum of 44 ksps. However, as shown in Figure 2-82, significant post-processing of the data is required to interpolate the value of the waveform during the time between each sample.

Similarly, to re-create the amplitude variation of a signal, the signal must be sampled with adequate resolution. Continuing with the audio example, the dynamic range of the human ear (the ratio of the amplitude of the threshold of hearing to the threshold of pain) is generally accepted to be 135 dB, and the dynamic range of a typical symphony orchestra performance is around 85 dB. Most commercial recording media provide about 96 dB of dynamic range using 16-bit sample resolution. But 16-bit fidelity does not necessarily mean that you need a 16-bit ADC. As long as the input is sampled at or above the Nyquist Frequency, post-processing techniques can be used to interpolate intermediate values and reconstruct the original input signal to within desired tolerances.

If sophisticated digital signal processing (DSP) capabilities are available, the best results are obtained by implementing a reconstruction filter, which is used to interpolate many intermediate values with higher resolution than the original data. Interpolating many intermediate values increases the effective number of samples, and higher resolution increases the effective number of bits in the sample. In many cases, however, it is not cost-effective or necessary to implement such a sophisticated reconstruction algorithm. For applications that do not require extremely fine reproduction of the input signal, alternative methods can enhance digital sampling results with relatively simple post-processing. The details of such techniques are out of the scope of this chapter; refer to the *Improving ADC Results through Oversampling and Post-Processing of Data* white paper for more information.

Intra-Conversion

Performing a conversion during power-up calibration is possible but should be avoided, since the performance is not guaranteed, as shown in Table 2-49 on page 2-117. This is described as intra-conversion. Figure 2-92 on page 2-113 shows intra-conversion, (conversion that starts during power-up calibration).

Injected Conversion

A conversion can be interrupted by another conversion. Before the current conversion is finished, a second conversion can be started by issuing a pulse on signal ADCSTART. When a second conversion is issued before the current conversion is completed, the current conversion would be dropped and the ADC would start the second conversion on the rising edge of the SYSCLK. This is known as injected conversion. Since the ADC is synchronous, the minimum time to issue a second conversion is two clock cycles of SYSCLK after the previous one. Figure 2-93 on page 2-113 shows injected conversion, (conversion that starts before a previously started conversion is finished). The total time for calibration still remains 3,840 ADCCLK cycles.

ADC Example

This example shows how to choose the correct settings to achieve the fastest sample time in 10-bit mode for a system that runs at 66 MHz. Assume the acquisition times defined in Table 2-44 on page 2-108 for 10-bit mode, which gives 0.549 µs as a minimum hold time.

The period of SYSCLK: t_{SYSCLK} = 1/66 MHz = 0.015 µs

Choosing TVC between 1 and 33 will meet the maximum and minimum period for the ADCCLK requirement. A higher TVC leads to a higher ADCCLK period.

The minimum TVC is chosen so that $t_{distrib}$ and $t_{post\text{-}cal}$ can be run faster. The period of ADCCLK with a TVC of 1 can be computed by EQ 24.

$$t_{ADCCLK} = 4 \times (1 + TVC) \times t_{SYSCLK} = 4 \times (1 + 1) \times 0.015\ \mu s = 0.12\ \mu s$$

EQ 24

The STC value can now be computed by using the minimum sample/hold time from Table 2-44 on page 2-108, as shown in EQ 25.

$$STC = \frac{t_{sample}}{t_{ADCCLK}} - 2 = \frac{0.549\ \mu s}{0.12\ \mu s} - 2 = 4.575 - 2 = 2.575$$

EQ 25

You must round up to 3 to accommodate the minimum sample time requirement. The actual sample time, t_{sample}, with an STC of 3, is now equal to 0.6 µs, as shown in EQ 26

$$t_{sample} = (2 + STC) \times t_{ADCCLK} = (2 + 3) \times t_{ADCCLK} = 5 \times 0.12\ \mu s = 0.6\ \mu s$$

EQ 26

Microsemi recommends post-calibration for temperature drift over time, so post-calibration is enabled.

The post-calibration time, $t_{post\text{-}cal}$, can be computed by EQ 27. The post-calibration time is 0.24 µs.

$$t_{post\text{-}cal} = 2 \times t_{ADCCLK} = 0.24\ \mu s$$

EQ 27

The distribution time, $t_{distrib}$, is equal to 1.2 µs and can be computed as shown in EQ 28 (N is number of bits, referring back to EQ 8 on page 2-94).

$$t_{distrib} = N \times t_{ADCCLK} = 10 \times 0.12 = 1.2\ \mu s$$

EQ 28

The total conversion time can now be summated, as shown in EQ 29 (referring to EQ 23 on page 2-109).

$$t_{sync\_read} + t_{sample} + t_{distrib} + t_{post\text{-}cal} + t_{sync\_write} = (0.015 + 0.60 + 1.2 + 0.24 + 0.015)\ \mu s = 2.07\ \mu s$$

EQ 29

ADC Interface Timing

Table 2-48 • ADC Interface Timing
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{SUMODE}	Mode Pin Setup Time	0.56	0.64	0.75	ns
t_{HDMODE}	Mode Pin Hold Time	0.26	0.29	0.34	ns
t_{SUTVC}	Clock Divide Control (TVC) Setup Time	0.68	0.77	0.90	ns
t_{HDTVC}	Clock Divide Control (TVC) Hold Time	0.32	0.36	0.43	ns
t_{SUSTC}	Sample Time Control (STC) Setup Time	1.58	1.79	2.11	ns
t_{HDSTC}	Sample Time Control (STC) Hold Time	1.27	1.45	1.71	ns
$t_{SUVAREFSEL}$	Voltage Reference Select (VAREFSEL) Setup Time	0.00	0.00	0.00	ns
$t_{HDVAREFSEL}$	Voltage Reference Select (VAREFSEL) Hold Time	0.67	0.76	0.89	ns
$t_{SUCHNUM}$	Channel Select (CHNUMBER) Setup Time	0.90	1.03	1.21	ns
$t_{HDCHNUM}$	Channel Select (CHNUMBER) Hold Time	0.00	0.00	0.00	ns
$t_{SUADCSTART}$	Start of Conversion (ADCSTART) Setup Time	0.75	0.85	1.00	ns
$t_{HDADCSTART}$	Start of Conversion (ADCSTART) Hold Time	0.43	0.49	0.57	ns
$t_{CK2QBUSY}$	Busy Clock-to-Q	1.33	1.51	1.78	ns
$t_{CK2QCAL}$	Power-Up Calibration Clock-to-Q	0.63	0.71	0.84	ns
$t_{CK2QVAL}$	Valid Conversion Result Clock-to-Q	3.12	3.55	4.17	ns
$t_{CK2QSAMPLE}$	Sample Clock-to-Q	0.22	0.25	0.30	ns
$t_{CK2QRESULT}$	Conversion Result Clock-to-Q	2.53	2.89	3.39	ns
$t_{CLR2QBUSY}$	Busy Clear-to-Q	2.06	2.35	2.76	ns
$t_{CLR2QCAL}$	Power-Up Calibration Clear-to-Q	2.15	2.45	2.88	ns
$t_{CLR2QVAL}$	Valid Conversion Result Clear-to-Q	2.41	2.74	3.22	ns
$t_{CLR2QSAMPLE}$	Sample Clear-to-Q	2.17	2.48	2.91	ns
$t_{CLR2QRESULT}$	Conversion result Clear-to-Q	2.25	2.56	3.01	ns
t_{RECCLR}	Recovery Time of Clear	0.00	0.00	0.00	ns
t_{REMCLR}	Removal Time of Clear	0.63	0.72	0.84	ns
$t_{MPWSYSCLK}$	Clock Minimum Pulse Width for the ADC	4.00	4.00	4.00	ns
$t_{FMAXSYSCLK}$	Clock Maximum Frequency for the ADC	100.00	100.00	100.00	MHz

Table 2-54 • **ACM Address Decode Table for Analog Quad (continued)**

ACMADDR [7:0] in Decimal	Name	Description	Associated Peripheral
73	MATCHREG1	Match register bits 15:8	RTC
74	MATCHREG2	Match register bits 23:16	RTC
75	MATCHREG3	Match register bits 31:24	RTC
76	MATCHREG4	Match register bits 39:32	RTC
80	MATCHBITS0	Individual match bits 7:0	RTC
81	MATCHBITS1	Individual match bits 15:8	RTC
82	MATCHBITS2	Individual match bits 23:16	RTC
83	MATCHBITS3	Individual match bits 31:24	RTC
84	MATCHBITS4	Individual match bits 39:32	RTC
88	CTRL_STAT	Control (write) / Status (read) register bits 7:0	RTC
Note: ACMADDR bytes 1 to 40 pertain to the Analog Quads; bytes 64 to 89 pertain to the RTC.			

ACM Characteristics[1]

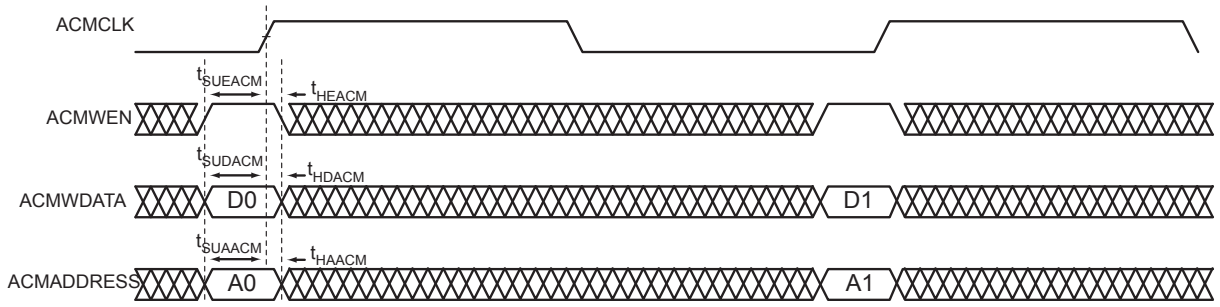

Figure 2-97 • **ACM Write Waveform**

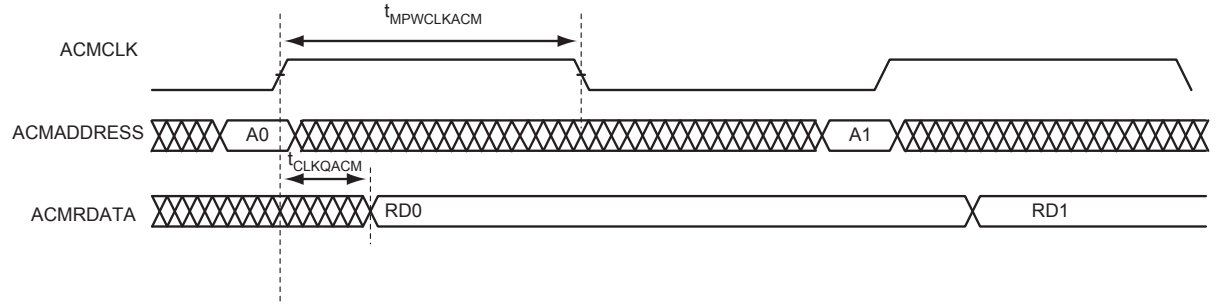

Figure 2-98 • **ACM Read Waveform**

1. *When addressing the RTC addresses (i.e., ACMADDR 64 to 89), there is no timing generator, and the rc_osc, byte_en, and aq_wen signals have no impact.*

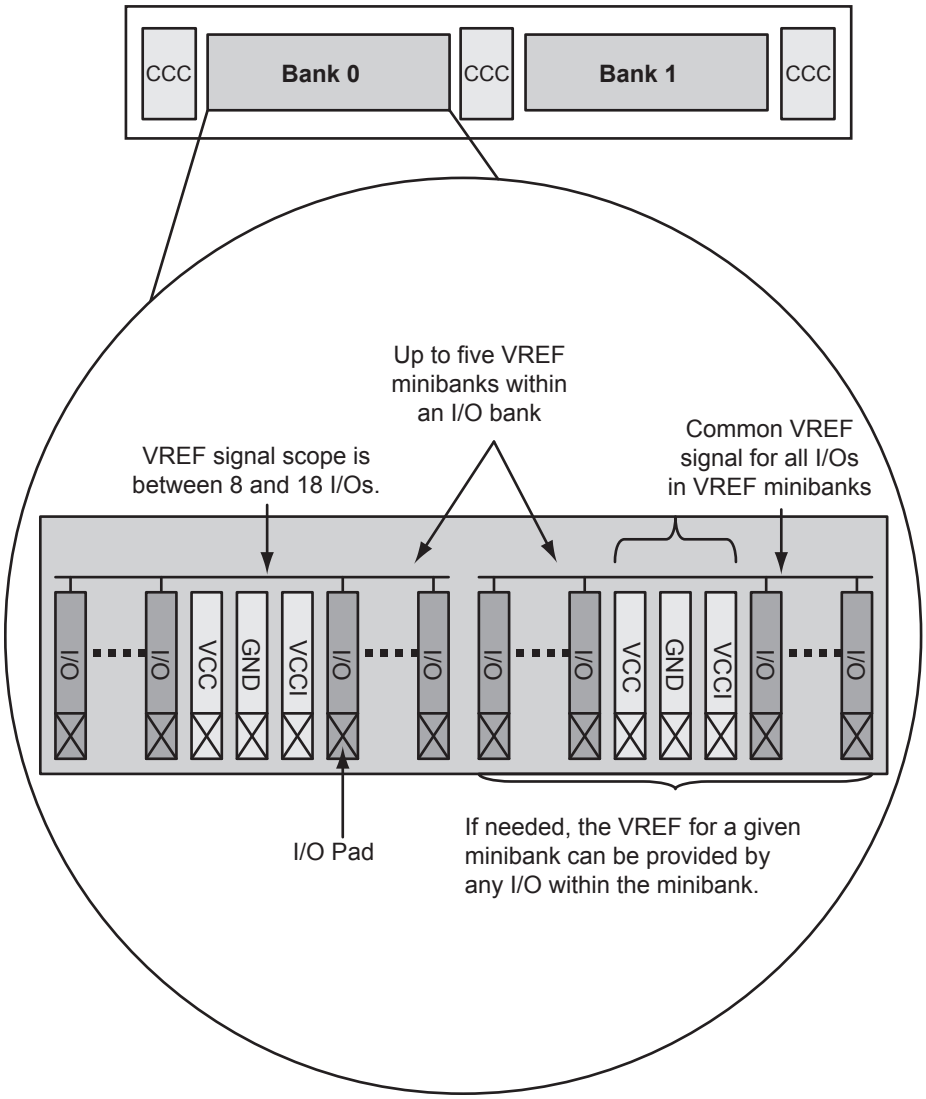

Figure 2-99 • **Fusion Pro I/O Bank Detail Showing VREF Minibanks (north side ofAFS600 and AFS1500)**

Table 2-67 • **I/O Standards Supported by Bank Type**

I/O Bank	Single-Ended I/O Standards	Differential I/O Standards	Voltage-Referenced	Hot-Swap
Standard I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V	–	–	Yes
Advanced I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X	LVPECL and LVDS	–	–
Pro I/O	LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V, 3.3 V PCI / 3.3 V PCI-X	LVPECL and LVDS	GTL+ 2.5 V / 3.3 V, GTL 2.5 V / 3.3 V, HSTL Class I and II, SSTL2 Class I and II, SSTL3 Class I and II	Yes

Features Supported on Pro I/Os

Table 2-72 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

***Table 2-72* • Fusion Pro I/O Features**

Feature	Description
Single-ended and voltage-referenced transmitter features	• Hot insertion in every mode except PCI or 5 V input tolerant (these modes use clamp diodes and do not allow hot insertion)
	• Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.
	• Weak pull-up and pull-down
	• Two slew rates
	• Skew between output buffer enable/disable time: 2 ns delay (rising edge) and 0 ns delay (falling edge); see "Selectable Skew between Output Buffer Enable/Disable Time" on page 2-149 for more information
	• Five drive strengths
	• 5 V–tolerant receiver ("5 V Input Tolerance" section on page 2-144)
	• LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-148)
	• High performance (Table 2-76 on page 2-143)
Single-ended receiver features	• Schmitt trigger option
	• ESD protection
	• Programmable delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)
	• High performance (Table 2-76 on page 2-143)
	• Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry
Voltage-referenced differential receiver features	• Programmable Delay: 0 ns if bypassed, 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)
	• High performance (Table 2-76 on page 2-143)
	• Separate ground planes, GND/GNDQ, for input buffers only to avoid output-induced noise in the input circuitry
CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL transmitter	• Two I/Os and external resistors are used to provide a CMOS-style LVDS, BLVDS, M-LVDS, or LVPECL transmitter solution.
	• Activation of hot insertion (disabling the clamp diode) is selectable by I/Os.
	• Weak pull-up and pull-down
	• Fast slew rate
LVDS/LVPECL differential receiver features	• ESD protection
	• High performance (Table 2-76 on page 2-143)
	• Programmable delay: 0.625 ns with '000' setting, 6.575 ns with '111' setting, 0.85-ns intermediate delay increments (at 25°C, 1.5 V)
	• Separate input buffer ground and power planes to avoid output-induced noise in the input circuitry

Table 2-96 • I/O Output Buffer Maximum Resistances [1] (continued)

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (ohms) [2]	$R_{PULL\text{-}UP}$ (ohms) [3]
HSTL (I)	8 mA	50	50
HSTL (II)	15 mA	25	25
SSTL2 (I)	17 mA	27	31
SSTL2 (II)	21 mA	13	15
SSTL3 (I)	16 mA	44	69
SSTL3 (II)	24 mA	18	32
Applicable to Advanced I/O Banks			
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCC, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/techdocs/models/ibis.html.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = VOLspec / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-110 • Minimum and Maximum DC Input and Output Levels

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Applicable to Pro I/O Banks												
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	10	10
Applicable to Standard I/O Banks												
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

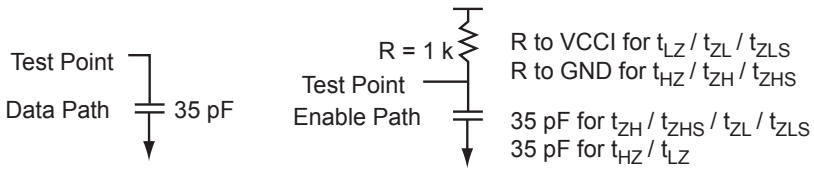

Figure 2-120 • AC Loading

Table 2-111 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

1.8 V LVCMOS

Low-Voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and push-pull output buffer.

Table 2-118 • Minimum and Maximum DC Input and Output Levels

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
Applicable to Pro I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	16	16	74	91	10	10
Applicable to Advanced I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	74	91	10	10
Applicable to Standard I/O Banks												
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

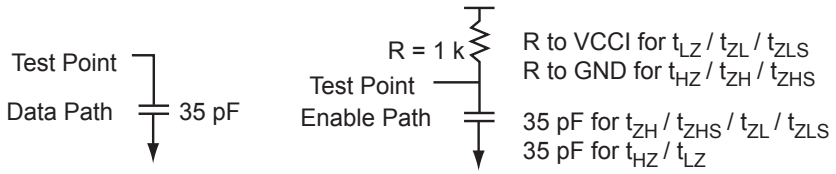

Figure 2-121 • AC Loading

Table 2-119 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input Low (V)	Measuring Point* (V)	VREF (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

SSTL2 Class I

Stub-Speed Terminated Logic for 2.5 V memory bus standard (JESD8-9). Fusion devices support Class I. This provides a differential amplifier input buffer and a push-pull output buffer.

Table 2-156 • Minimum and Maximum DC Input and Output Levels

SSTL2 Class I	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
15 mA	–0.3	VREF – 0.2	VREF + 0.2	3.6	0.54	VCCI – 0.62	15	15	87	83	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*

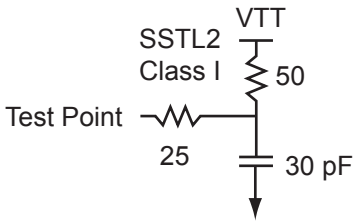

Figure 2-130 • AC Loading

Table 2-157 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	VREF (typ.) (V)	VTT (typ.) (V)	C_{LOAD} (pF)
VREF – 0.2	VREF + 0.2	1.25	1.25	1.25	30

*Note: *Measuring point = Vtrip. See Table 2-90 on page 2-166 for a complete table of trip points.*

Timing Characteristics

Table 2-158 • SSTL 2 Class I
Commercial Temperature Range Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V, VREF = 1.25 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.13	0.04	1.33	0.43	2.17	1.85			4.40	4.08	ns
–1	0.56	1.81	0.04	1.14	0.36	1.84	1.57			3.74	3.47	ns
–2	0.49	1.59	0.03	1.00	0.32	1.62	1.38			3.29	3.05	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-9.

Output DDR

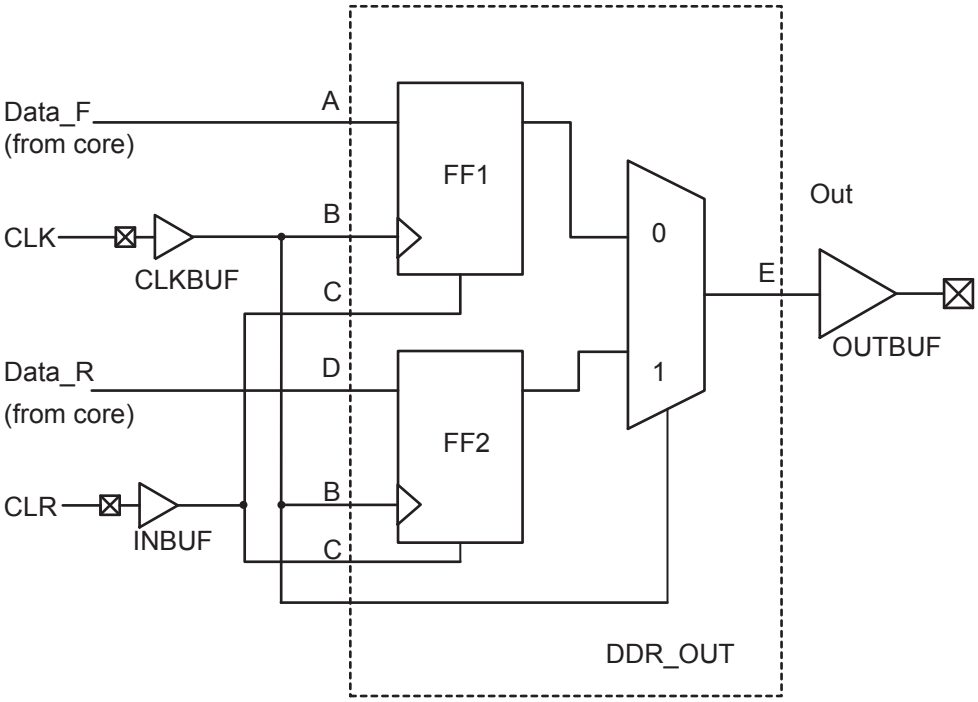

Figure 2-144 • **Output DDR Timing Model**

Table 2-181 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (From, To)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

ATRTN*x* **Temperature Monitor Return**

AT returns are the returns for the temperature sensors. The cathode terminal of the external diodes should be connected to these pins. There is one analog return pin for every two Analog Quads. The *x* in the ATRTN*x* designator indicates the quad pairing (*x* = 0 for AQ1 and AQ2, *x* = 1 for AQ2 and AQ3, ..., *x* = 4 for AQ8 and AQ9). The signals that drive these pins are called out as ATRETURN*xy* in the software (where *x* and *y* refer to the quads that share the return signal). ATRTN is internally connected to ground. It can be left floating when it is unused. The maximum capacitance allowed across the AT pins is 500 pF.

GL **Globals**

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as Pro I/Os since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-22.

Refer to the "User I/O Naming Convention" section on page 2-158 for a description of naming of global pins.

JTAG Pins

Fusion devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the Fusion part must be supplied to allow JTAG signals to transition the Fusion device.

Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRST pin could be tied to GND.

TCK **Test Clock**

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND or VJTAG through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 2-183 for more information.

***Table 2-183* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance[2, 3]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on JTAG chain.*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin can only be pulled down.*

TDI **Test Data Input**

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO **Test Data Output**

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

RC Oscillator Dynamic Contribution—$P_{RC\text{-}OSC}$

Operating Mode

$P_{RC\text{-}OSC}$ = PAC19

Standby Mode and Sleep Mode

$P_{RC\text{-}OSC}$ = 0 W

Analog System Dynamic Contribution—P_{AB}

Operating Mode

P_{AB} = PAC20

Standby Mode and Sleep Mode

P_{AB} = 0 W

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

***Table 3-16* • Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

***Table 3-17* • Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%
β_4	NVM enable rate for read operations	0%

PQ208		
Pin Number	AFS250 Function	AFS600 Function
74	AV2	AV4
75	AC2	AC4
76	AG2	AG4
77	AT2	AT4
78	ATRTN1	ATRTN2
79	AT3	AT5
80	AG3	AG5
81	AC3	AC5
82	AV3	AV5
83	AV4	AV6
84	AC4	AC6
85	AG4	AG6
86	AT4	AT6
87	ATRTN2	ATRTN3
88	AT5	AT7
89	AG5	AG7
90	AC5	AC7
91	AV5	AV7
92	NC	AV8
93	NC	AC8
94	NC	AG8
95	NC	AT8
96	NC	ATRTN4
97	NC	AT9
98	NC	AG9
99	NC	AC9
100	NC	AV9
101	GNDAQ	GNDAQ
102	VCC33A	VCC33A
103	ADCGNDREF	ADCGNDREF
104	VAREF	VAREF
105	PUB	PUB
106	VCC33A	VCC33A
107	GNDA	GNDA
108	PTEM	PTEM
109	PTBASE	PTBASE
110	GNDNVM	GNDNVM

PQ208		
Pin Number	AFS250 Function	AFS600 Function
111	VCCNVM	VCCNVM
112	VCC	VCC
112	VCC	VCC
113	VPUMP	VPUMP
114	GNDQ	NC
115	VCCIB1	TCK
116	TCK	TDI
117	TDI	TMS
118	TMS	TDO
119	TDO	TRST
120	TRST	VJTAG
121	VJTAG	IO57NDB2V0
122	IO57NDB1V0	GDC2/IO57PDB2V0
123	GDC2/IO57PDB1V0	IO56NDB2V0
124	IO56NDB1V0	GDB2/IO56PDB2V0
125	GDB2/IO56PDB1V0	IO55NDB2V0
126	VCCIB1	GDA2/IO55PDB2V0
127	GND	GDA0/IO54NDB2V0
128	IO55NDB1V0	GDA1/IO54PDB2V0
129	GDA2/IO55PDB1V0	VCCIB2
130	GDA0/IO54NDB1V0	GND
131	GDA1/IO54PDB1V0	VCC
132	GDB0/IO53NDB1V0	GCA0/IO45NDB2V0
133	GDB1/IO53PDB1V0	GCA1/IO45PDB2V0
134	GDC0/IO52NDB1V0	GCB0/IO44NDB2V0
135	GDC1/IO52PDB1V0	GCB1/IO44PDB2V0
136	IO51NSB1V0	GCC0/IO43NDB2V0
137	VCCIB1	GCC1/IO43PDB2V0
138	GND	IO42NDB2V0
139	VCC	IO42PDB2V0
140	IO50NDB1V0	IO41NDB2V0
141	IO50PDB1V0	GCC2/IO41PDB2V0
142	GCA0/IO49NDB1V0	VCCIB2
143	GCA1/IO49PDB1V0	GND
144	GCB0/IO48NDB1V0	VCC
145	GCB1/IO48PDB1V0	IO40NDB2V0
146	GCC0/IO47NDB1V0	GCB2/IO40PDB2V0

FG484		
Pin Number	AFS600 Function	AFS1500 Function
P21	IO51PDB2V0	IO73PDB2V0
P22	IO49NDB2V0	IO71NDB2V0
R1	IO69PDB4V0	IO102PDB4V0
R2	IO69NDB4V0	IO102NDB4V0
R3	VCCIB4	VCCIB4
R4	IO64PDB4V0	IO91PDB4V0
R5	IO64NDB4V0	IO91NDB4V0
R6	NC	IO92PDB4V0
R7	GND	GND
R8	GND	GND
R9	VCC33A	VCC33A
R10	GNDA	GNDA
R11	VCC33A	VCC33A
R12	GNDA	GNDA
R13	VCC33A	VCC33A
R14	GNDA	GNDA
R15	VCC	VCC
R16	GND	GND
R17	NC	IO74NDB2V0
R18	GDA0/IO54NDB2V0	GDA0/IO81NDB2V0
R19	GDB0/IO53NDB2V0	GDB0/IO80NDB2V0
R20	VCCIB2	VCCIB2
R21	IO50NDB2V0	IO75NDB2V0
R22	IO50PDB2V0	IO75PDB2V0
T1	NC	IO100PPB4V0
T2	GND	GND
T3	IO66PDB4V0	IO95PDB4V0
T4	IO66NDB4V0	IO95NDB4V0
T5	VCCIB4	VCCIB4
T6	NC	IO92NDB4V0
T7	GNDNVM	GNDNVM
T8	GNDA	GNDA
T9	NC	NC
T10	AV4	AV4
T11	NC	NC

FG484		
Pin Number	AFS600 Function	AFS1500 Function
T12	AV5	AV5
T13	AC5	AC5
T14	NC	NC
T15	GNDA	GNDA
T16	NC	IO77PPB2V0
T17	NC	IO74PDB2V0
T18	VCCIB2	VCCIB2
T19	IO55NDB2V0	IO82NDB2V0
T20	GDA2/IO55PDB2V0	GDA2/IO82PDB2V0
T21	GND	GND
T22	GDC1/IO52PDB2V0	GDC1/IO79PDB2V0
U1	IO67PDB4V0	IO98PDB4V0
U2	IO67NDB4V0	IO98NDB4V0
U3	GEC1/IO63PDB4V0	GEC1/IO90PDB4V0
U4	GEC0/IO63NDB4V0	GEC0/IO90NDB4V0
U5	GND	GND
U6	VCCNVM	VCCNVM
U7	VCCIB4	VCCIB4
U8	VCC15A	VCC15A
U9	GNDA	GNDA
U10	AC4	AC4
U11	VCC33A	VCC33A
U12	GNDA	GNDA
U13	AG5	AG5
U14	GNDA	GNDA
U15	PUB	PUB
U16	VCCIB2	VCCIB2
U17	TDI	TDI
U18	GND	GND
U19	IO57NDB2V0	IO84NDB2V0
U20	GDC2/IO57PDB2V0	GDC2/IO84PDB2V0
U21	NC	IO77NPB2V0
U22	GDC0/IO52NDB2V0	GDC0/IO79NDB2V0
V1	GEB1/IO62PDB4V0	GEB1/IO89PDB4V0
V2	GEB0/IO62NDB4V0	GEB0/IO89NDB4V0

Revision	Changes	Page
Advance v0.6 (continued)	The "Analog-to-Digital Converter Block" section was updated with the following statement: "All results are MSB justified in the ADC."	2-99
	The information about the ADCSTART signal was updated in the "ADC Description" section.	2-102
	Table 2-46 · Analog Channel Specifications was updated.	2-118
	Table 2-47 · ADC Characteristics in Direct Input Mode was updated.	2-121
	Table 2-51 • ACM Address Decode Table for Analog Quad was updated.	2-127
	In Table 2-53 • Analog Quad ACM Byte Assignment, the Function and Default Setting for Bit 6 in Byte 3 was updated.	2-130
	The "Introduction" section was updated to include information about digital inputs, outputs, and bibufs.	2-133
	In Table 2-69 • Fusion Pro I/O Features, the programmable delay descriptions were updated for the following features: Single-ended receiver Voltage-referenced differential receiver LVDS/LVPECL differential receiver features	2-137
	The "User I/O Naming Convention" section was updated to include "V" and "z" descriptions	2-159
	The "VCC33PMP Analog Power Supply (3.3 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VCCNVM Flash Memory Block Power Supply (1.5 V)" section was updated to include information about avoiding high current draw.	2-224
	The "VMVx I/O Supply Voltage (quiet)" section was updated to include this statement: VMV and VCCI must be connected to the same power supply and V_{CCI} pins within a given I/O bank.	2-185
	The "PUB Push Button" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTBASE Pass Transistor Base" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The "PTEM Pass Transistor Emitter" section was updated to include information about leaving the pin floating if it is not used.	2-228
	The heading was incorrect in the "208-Pin PQFP" table. It should be AFS250 and not AFS090.	3-8