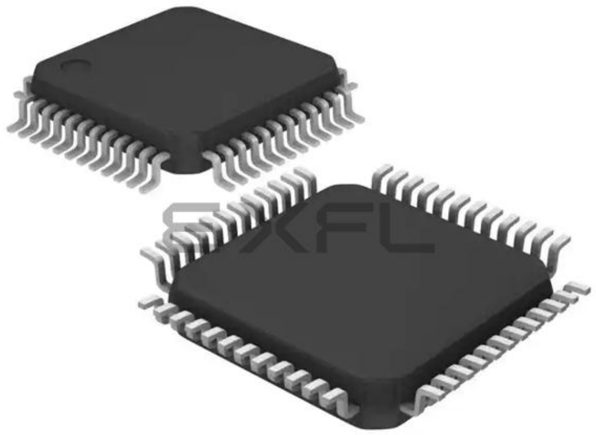
NXP USA Inc. - MKL04Z16VLF4 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 14x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl04z16vlf4

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Table 6. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVW1H}	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	—
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	—

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad (except $\overline{\text{RESET}}$)				1, 2
	• $2.7\ V \leq V_{DD} \leq 3.6\ V$, $I_{OH} = -5$ mA	$V_{DD} - 0.5$	—	V	
	• $1.71\ V \leq V_{DD} \leq 2.7\ V$, $I_{OH} = -1.5$ mA	$V_{DD} - 0.5$	—	V	
V_{OH}	Output high voltage — High drive pad (except RESET_b)				1, 2
	• $2.7\ V \leq V_{DD} \leq 3.6\ V$, $I_{OH} = -18$ mA	$V_{DD} - 0.5$	—	V	
	• $1.71\ V \leq V_{DD} \leq 2.7\ V$, $I_{OH} = -6$ mA	$V_{DD} - 0.5$	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — Normal drive pad				1
	• $2.7\ V \leq V_{DD} \leq 3.6\ V$, $I_{OL} = 5$ mA	—	0.5	V	
	• $1.71\ V \leq V_{DD} \leq 2.7\ V$, $I_{OL} = 1.5$ mA	—	0.5	V	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
I_{DD_WAIT}	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	—	2.2	2.3	mA	3
I_{DD_PSTOP2}	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus / flash disabled (flash doze enabled) • at 3.0 V	—	1.5	1.7	mA	3
I_{DD_VLPRCO}	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code executing from flash • at 3.0 V	—	182	253	µA	5
I_{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code executing from flash • at 3.0 V	—	213	284	µA	5
I_{DD_VLPR}	Very low power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code executing from flash • at 3.0 V	—	243	313	µA	4, 5
I_{DD_VLPW}	Very low power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled • at 3.0 V	—	111	170	µA	5
I_{DD_STOP}	Stop mode current • at 3.0 V				µA	
	• at 25 °C	—	257	277		
	• at 50 °C	—	265	285		
	• at 70 °C	—	278	303		
	• at 85 °C	—	295	326		
	• at 105 °C	—	353	412		
I_{DD_VLPS}	Very-low-power stop mode current • at 3.0 V				µA	
	• at 25 °C	—	2.25	5.76		
	• at 50 °C	—	4.08	8.27		
	• at 70 °C	—	8.10	14.52		
	• at 85 °C	—	14.18	23.78		
	• at 105 °C	—	37.07	58.58		
I_{DD_LLS}	Low-leakage stop mode current • at 3.0 V					

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.[1]	Unit	Notes
	• at 25 °C	—	1.72	2.01	μA	
	• at 50 °C	—	2.52	3.18		
	• at 70 °C	—	4.32	5.94		
	• at 85 °C	—	7.18	10.00		
	• at 105 °C	—	18.67	25.65		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current • at 3.0 V				μA	
	• at 25 °C	—	1.16	1.36		
	• at 50 °C	—	1.78	2.27		
	• at 70 °C	—	3.23	4.38		
	• at 85 °C	—	5.57	7.53		
	• at 105 °C	—	14.80	19.74		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current • at 3.0 V					
	• at 25°C	—	0.64	0.81	μA	
	• at 50°C	—	1.14	1.50		
	• at 70°C	—	2.35	3.20		
	• at 85°C	—	4.37	5.80		
	• at 105°C	—	12.40	16.13		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) • at 3.0 V					
	• at 25 °C	—	0.38	0.54	μA	
	• at 50 °C	—	0.88	1.23		
	• at 70 °C	—	2.10	2.95		
	• at 85 °C	—	4.14	5.59		
	• at 105 °C	—	12.00	15.73		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) • at 3.0 V					6
	• at 25 °C	—	0.30	0.45	μA	
	• at 50 °C	—	0.79	1.12		
	• at 70 °C	—	2.01	2.82		
	• at 85 °C	—	4.05	5.45		
	• at 105 °C	—	11.96	15.63		

1. Data based on characterization results.

2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode.
6. No brownout

Table 10. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. • VLLS1 • VLLS3 • LLS • VLPS • STOP	440 440 490 510 510	490 490 490 560 560	540 540 540 560 560	560 560 560 560 560	570 570 570 610 610	580 580 680 680 680	nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. • MCGIRCLK (4 MHz internal reference clock) • OSCERCLK (4 MHz external crystal)	66 214	66 237	66 246	66 254	66 260	66 268	µA

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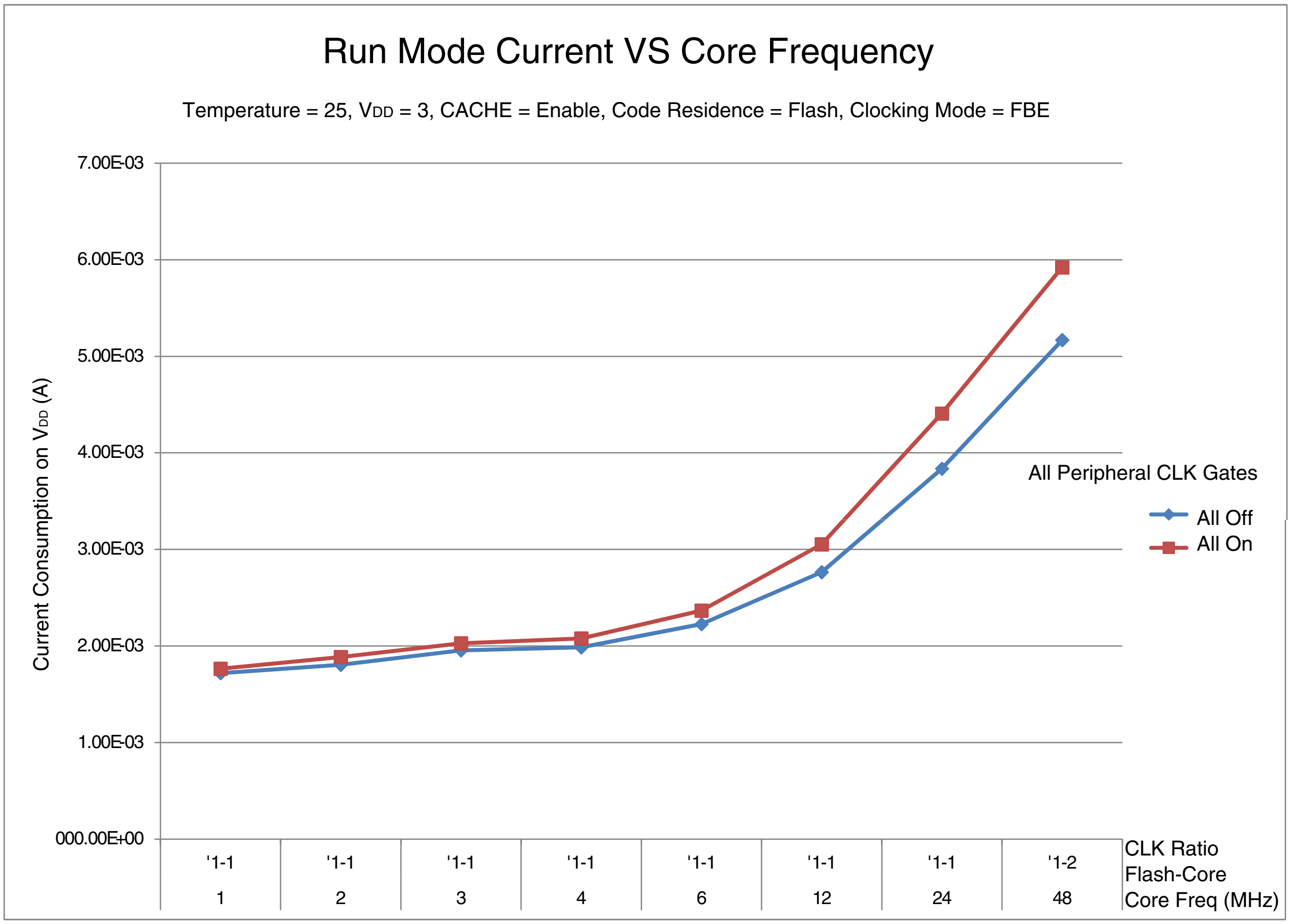


Figure 2. Run mode supply current vs. core frequency

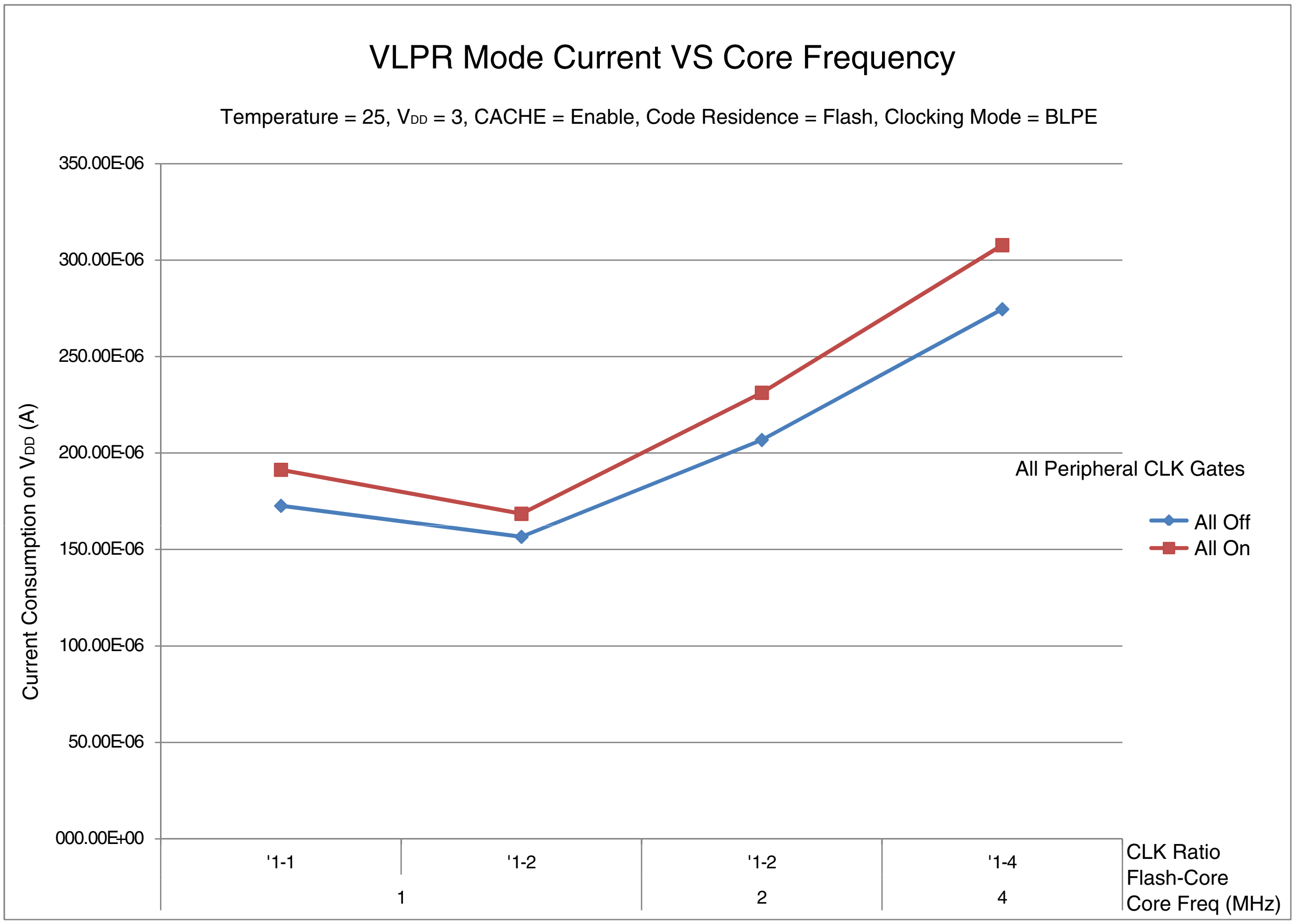


Figure 3. VLPR mode current vs. core frequency

2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on **freescale.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

Table 15. Thermal attributes (continued)

Board type	Symbol	Description	48 LQFP	32 LQFP	32 QFN	24 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	70	74	81	92	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	52	28	36	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	36	35	13	18	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	27	26	2.3	3.7	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	8	8	8	10	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD electricals

Table 16. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	 0	 25	 MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width			

Table continues on the next page...

Table 16. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

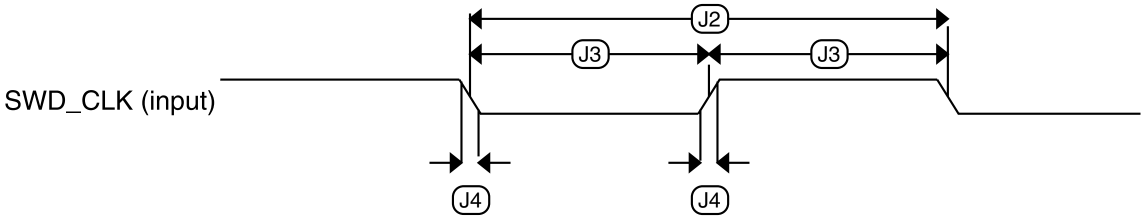


Figure 4. Serial wire clock input timing

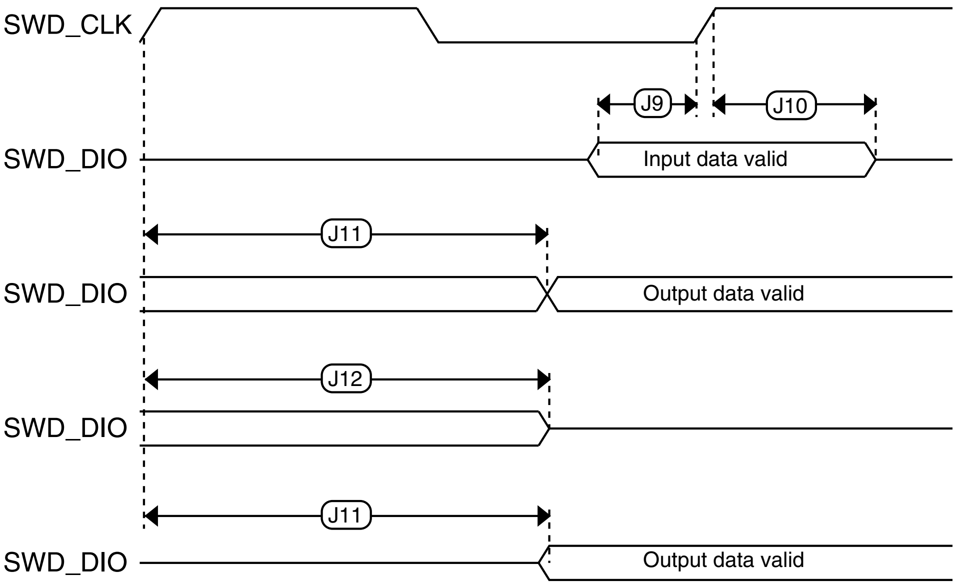


Figure 5. Serial wire data timing

Table 23. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

3.6.1.1 12-bit ADC operating conditions

Table 24. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} – V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} – V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	3
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 8-bit / 10-bit / 12-bit modes	—	4	5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	

Table continues on the next page...

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. ADC conversion clock < 3 MHz

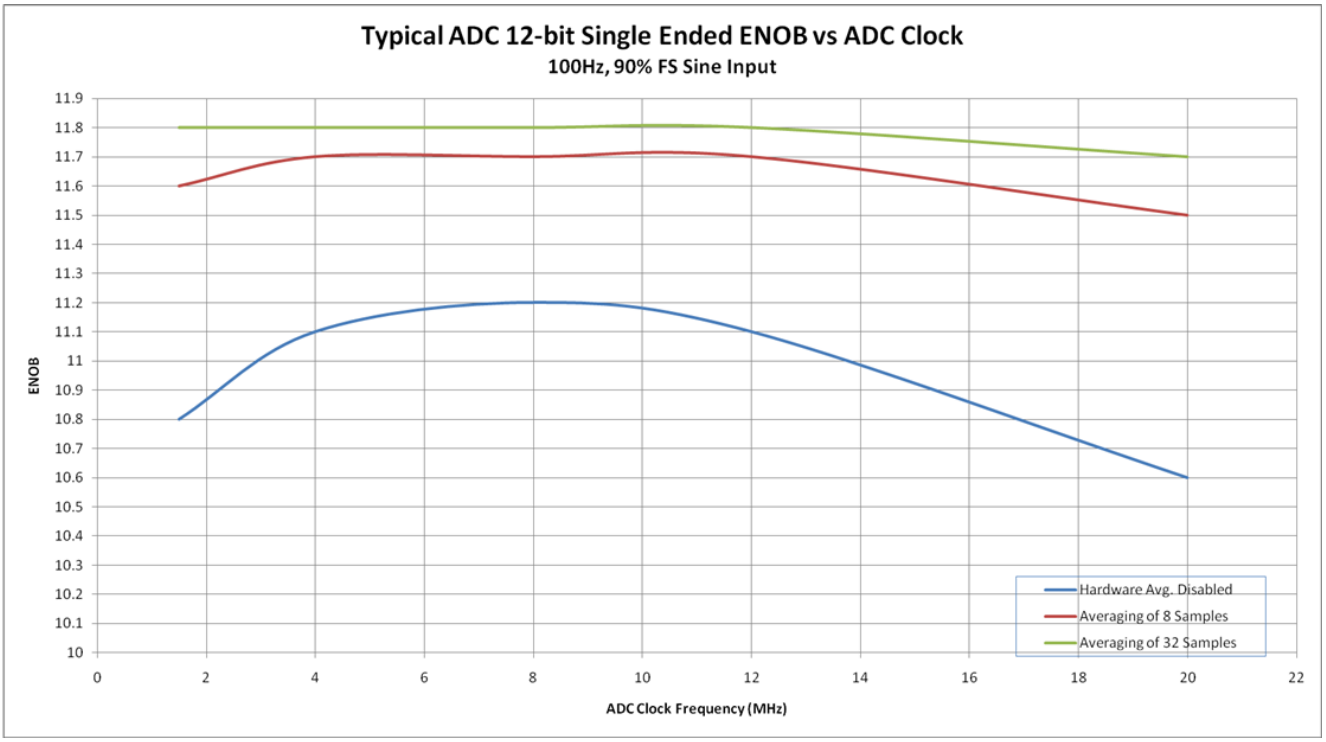


Figure 7. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode

3.6.2 CMP and 6-bit DAC electrical specifications

Table 26. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	μA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	μA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV

Table continues on the next page...

Table 26. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	μs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to $V_{DD} - 0.7$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

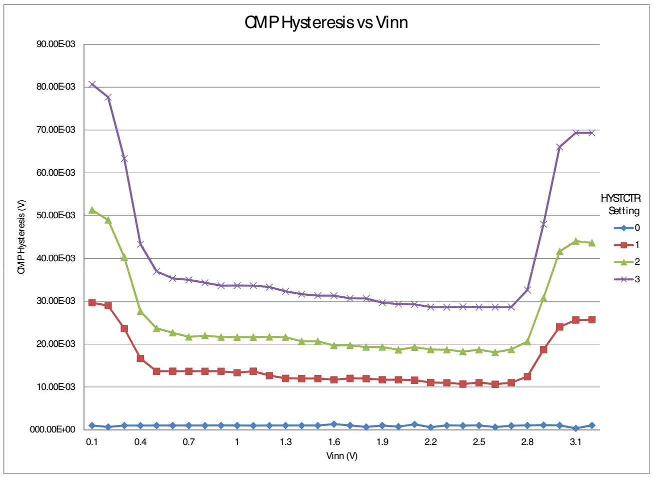


Figure 8. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

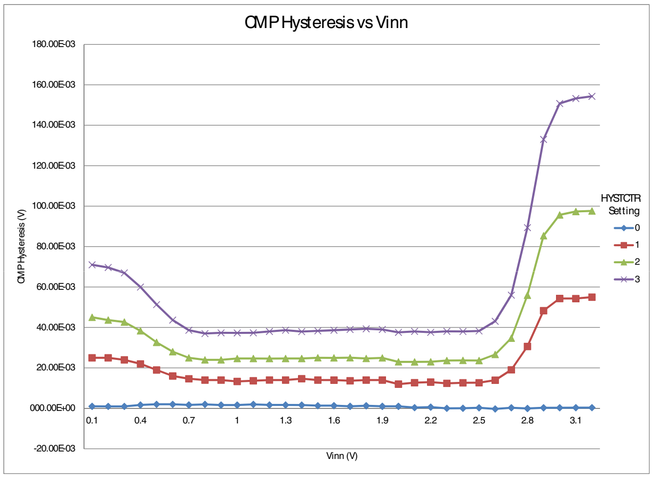


Figure 9. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

3.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 27. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—

Table continues on the next page...

Table 29. SPI slave mode timing on slew rate disabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	22	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 30. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	$t_{periph} - 25$	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0, f_{periph} is the bus clock (f_{BUS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

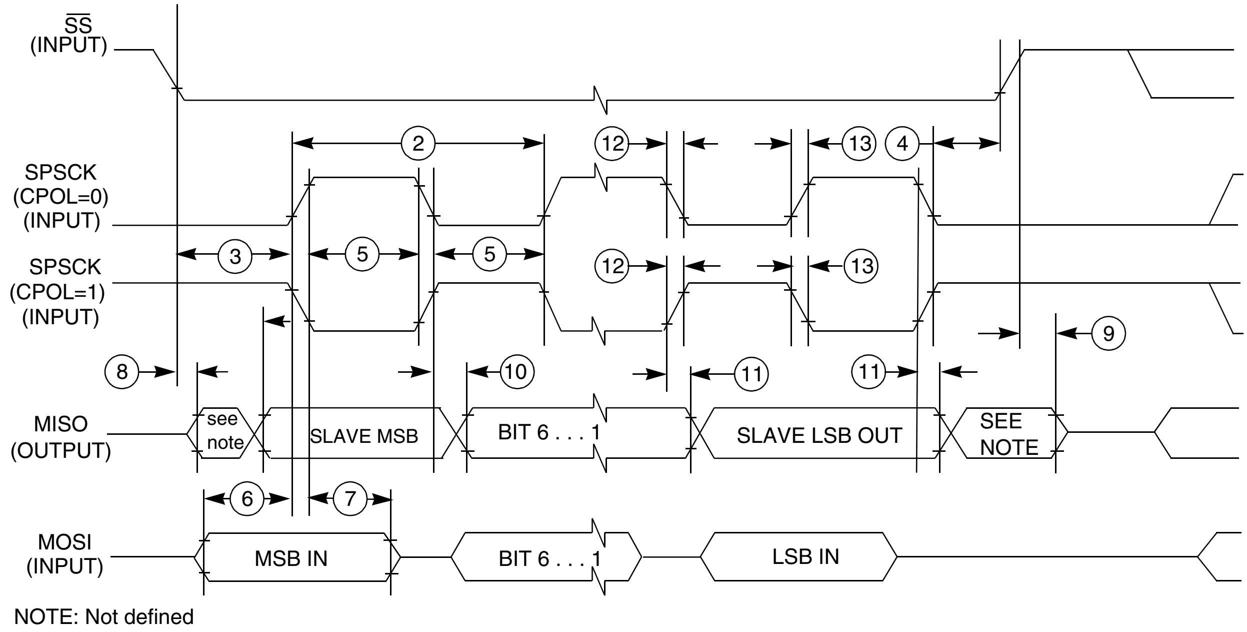


Figure 12. SPI slave mode timing (CPHA = 0)

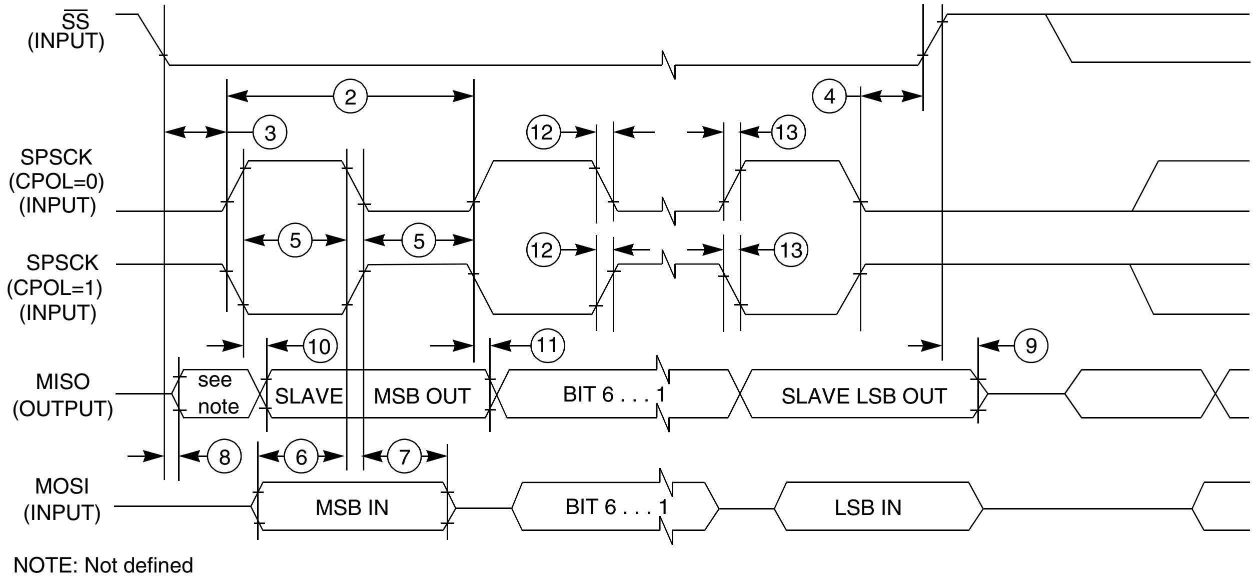


Figure 13. SPI slave mode timing (CPHA = 1)

3.8.2 Inter-Integrated Circuit Interface (I2C) timing

Table 31. I2C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400[1]	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I^{2}C bus devices	t_{HD}; DAT	0[2]	3.45[3]	0[4]	0.9[2]	µs
Data set-up time	t_{SU}; DAT	250[5]	—	100[3, 6]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[7]	300	ns
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[6]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see Voltage and current operating behaviors) or when using the Normal drive pins and VDD ≥ 2.7 V
2. The master mode I^{2}C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I^{2}C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU; DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^{2}C bus specification) before the SCL line is released.
7. C_b = total capacitance of the one bus line in pF.

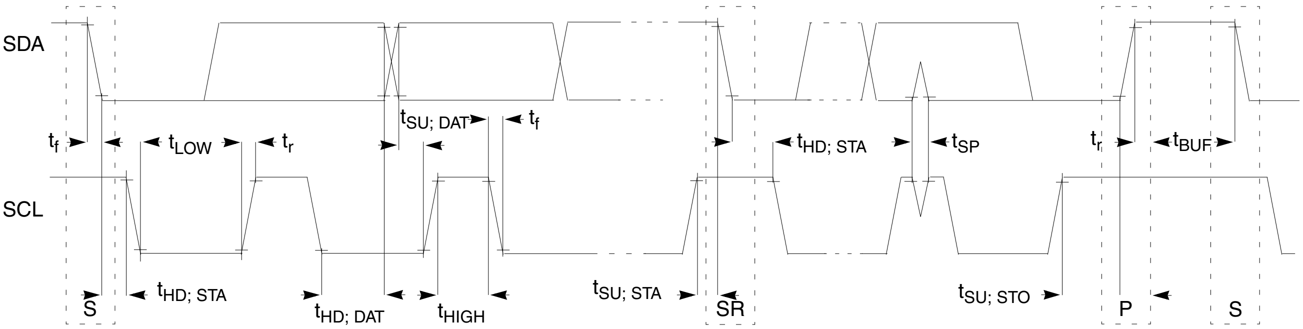


Figure 14. Timing definition for fast and standard mode devices on the I^{2}C bus

48 LQFP	32 QFN	32 LQFP	24 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
33	21	21	—	PTA10/ IRQ_12	DISABLED	DISABLED	PTA10/ IRQ_12		
34	22	22	—	PTA11/ IRQ_13	DISABLED	DISABLED	PTA11/ IRQ_13		
35	23	23	17	PTB3/ IRQ_14	DISABLED	DISABLED	PTB3/ IRQ_14	I2C0_SCL	UART0_TX
36	24	24	18	PTB4/ IRQ_15/ LLWU_P6	DISABLED	DISABLED	PTB4/ IRQ_15/ LLWU_P6	I2C0_SDA	UART0_RX
37	25	25	19	PTB5/ IRQ_16	NMI_b	ADC0_SE1/ CMP0_IN1	PTB5/ IRQ_16	TPM1_CH1	NMI_b
38	26	26	20	PTA12/ IRQ_17/ LPTMR0_ALT2	ADC0_SE0/ CMP0_IN0	ADC0_SE0/ CMP0_IN0	PTA12/ IRQ_17/ LPTMR0_ALT2	TPM1_CH0	TPM_CLKIN0
39	27	27	—	PTA13	DISABLED	DISABLED	PTA13		
40	28	28	—	PTB12	DISABLED	DISABLED	PTB12		
41	—	—	—	PTA19	DISABLED	DISABLED	PTA19		SPI0_SS_b
42	—	—	—	PTB15	DISABLED	DISABLED	PTB15	SPI0_MOSI	SPI0_MISO
43	—	—	—	PTB16	DISABLED	DISABLED	PTB16	SPI0_MISO	SPI0_MOSI
44	—	—	—	PTB17	DISABLED	DISABLED	PTB17	TPM_CLKIN1	SPI0_SCK
45	29	29	21	PTB13	ADC0_SE13	ADC0_SE13	PTB13	TPM1_CH1	RTC_CLKOUT
46	30	30	22	PTA0/ IRQ_0/ LLWU_P7	SWD_CLK	ADC0_SE12/ CMP0_IN2	PTA0/ IRQ_0/ LLWU_P7	TPM1_CH0	SWD_CLK
47	31	31	23	PTA1/ IRQ_1/ LPTMR0_ALT1	RESET_b	DISABLED	PTA1/ IRQ_1/ LPTMR0_ALT1	TPM_CLKIN0	RESET_b
48	32	32	24	PTA2	SWD_DIO	DISABLED	PTA2	CMP0_OUT	SWD_DIO

5.2 KL04 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see KL04 signal multiplexing and pin assignments.

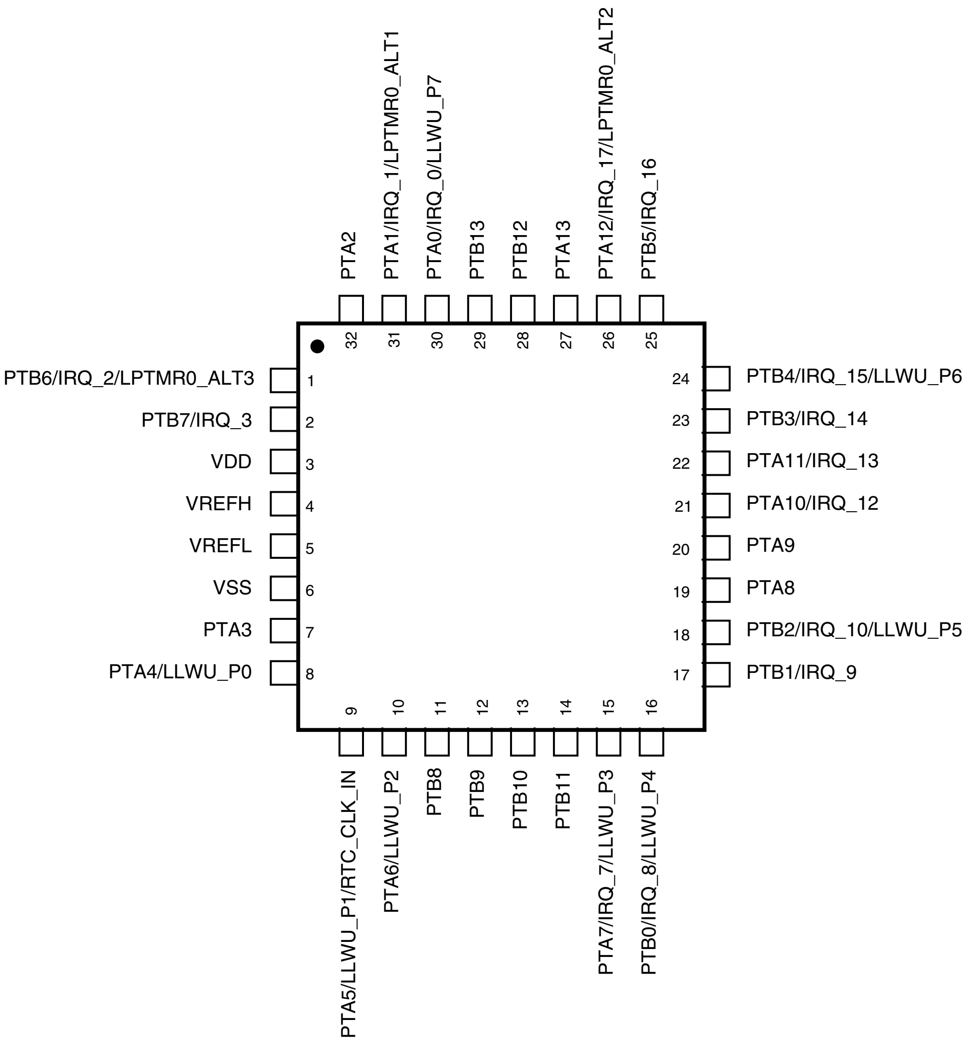


Figure 16. KL04 32-pin LQFP pinout diagram

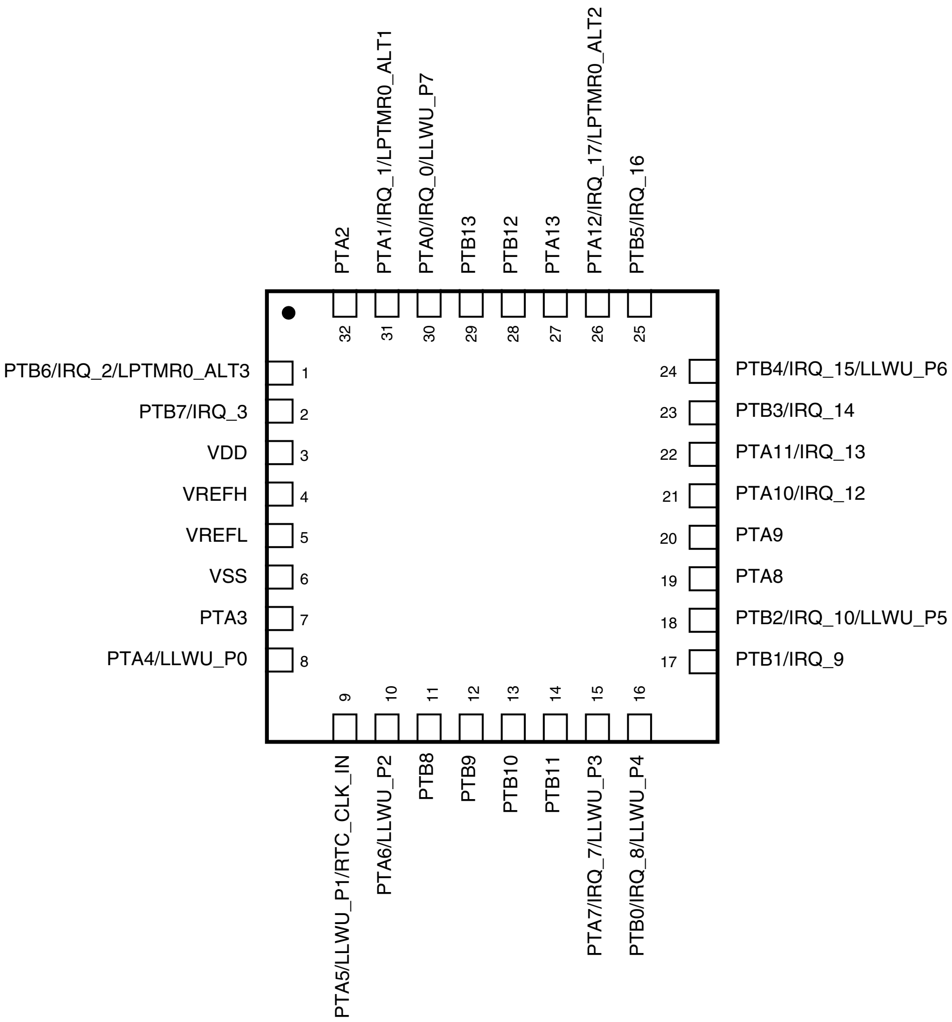


Figure 17. KL04 32-pin QFN pinout diagram

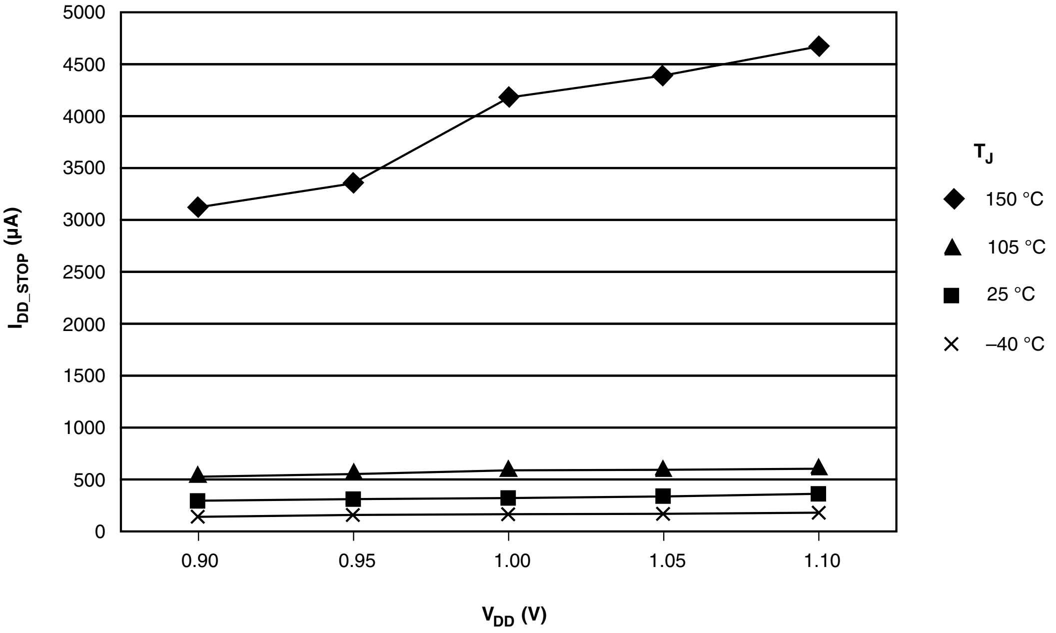
8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):