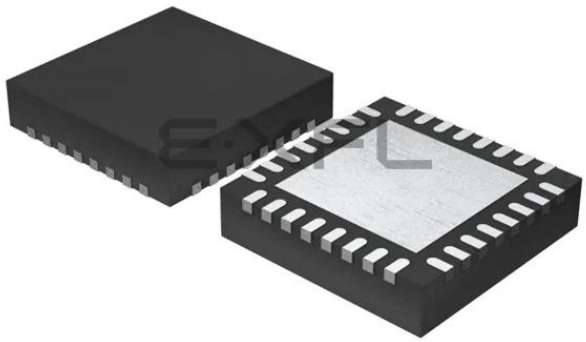

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT |
| Number of I/O | 28 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 3.6V |
| Data Converters | A/D 14x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount, Wettable Flank |
| Package / Case | 32-VFQFN Exposed Pad |
| Supplier Device Package | 32-HVQFN (5x5) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl04z8vfm4 |

## Ordering Information

| Part Number | Memory | | Maximum number of I\O's |
|---|---|---|---|
| | Flash (KB) | SRAM (KB) | |
| MKL04Z8VFK4 | 8 | 1 | 22 |
| MKL04Z16VFK4 | 16 | 2 | 22 |
| MKL04Z32VFK4 | 32 | 4 | 22 |
| MKL04Z8VLC4 | 8 | 1 | 28 |
| MKL04Z16VLC4 | 16 | 2 | 28 |
| MKL04Z32VLC4 | 32 | 4 | 28 |
| MKL04Z8VFM4 | 8 | 1 | 28 |
| MKL04Z16VFM4 | 16 | 2 | 28 |
| MKL04Z32VFM4 | 32 | 4 | 28 |
| MKL04Z16VLF4 | 16 | 2 | 41 |
| MKL04Z32VLF4 | 32 | 4 | 41 |

## Related Resources

| Type | Description |
|---|---|
| Selector Guide | The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector. |
| Product Brief | The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability. |
| Reference Manual | The Reference Manual contains a comprehensive description of the structure and function (operation) of a device. |
| Data Sheet | The Data Sheet includes electrical characteristics and signal connections. |
| Chip Errata | The chip mask set Errata provides additional or corrective information for a particular device mask set. |
| Package drawing | Package dimensions are provided in package drawings. |

## 1.4 Voltage and current operating ratings

**Table 4. Voltage and current operating ratings**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Digital supply voltage | –0.3 | 3.8 | V |
| $I_{DD}$ | Digital supply current | — | 120 | mA |
| $V_{IO}$ | IO pin input voltage | –0.3 | $V_{DD}$ + 0.3 | V |
| $I_D$ | Instantaneous maximum current single pin limit (applies to all port pins) | –25 | 25 | mA |
| $V_{DDA}$ | Analog supply voltage | $V_{DD}$ – 0.3 | $V_{DD}$ + 0.3 | V |

# 2 General

## 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

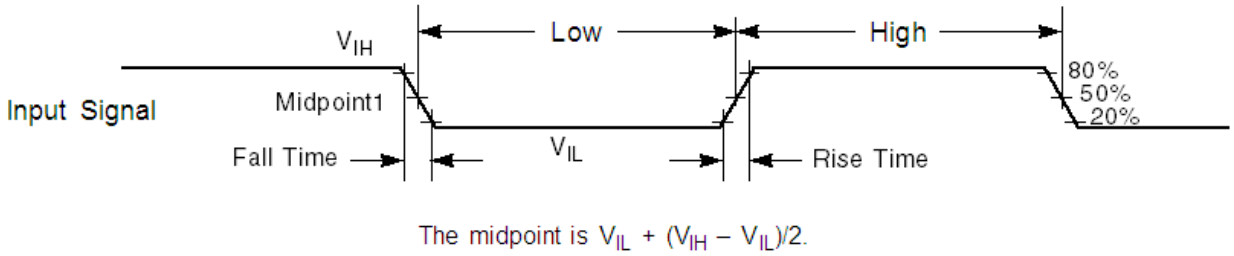



**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L$=30 pF loads
- Slew rate disabled
- Normal drive strength

## 2.2 Nonswitching electrical specifications

**Table 6. $V_{DD}$ supply LVD and POR operating requirements (continued)**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{LVW1H}$ | • Level 1 falling (LVWV = 00) | 2.62 | 2.70 | 2.78 | V | |
| $V_{LVW2H}$ | • Level 2 falling (LVWV = 01) | 2.72 | 2.80 | 2.88 | V | |
| $V_{LVW3H}$ | • Level 3 falling (LVWV = 10) | 2.82 | 2.90 | 2.98 | V | |
| $V_{LVW4H}$ | • Level 4 falling (LVWV = 11) | 2.92 | 3.00 | 3.08 | V | |
| $V_{HYSH}$ | Low-voltage inhibit reset/recover hysteresis — high range | — | ±60 | — | mV | — |
| $V_{LVDL}$ | Falling low-voltage detect threshold — low range (LVDV=00) | 1.54 | 1.60 | 1.66 | V | — |
| | Low-voltage warning thresholds — low range | | | | | 1 |
| $V_{LVW1L}$ | • Level 1 falling (LVWV = 00) | 1.74 | 1.80 | 1.86 | V | |
| $V_{LVW2L}$ | • Level 2 falling (LVWV = 01) | 1.84 | 1.90 | 1.96 | V | |
| $V_{LVW3L}$ | • Level 3 falling (LVWV = 10) | 1.94 | 2.00 | 2.06 | V | |
| $V_{LVW4L}$ | • Level 4 falling (LVWV = 11) | 2.04 | 2.10 | 2.16 | V | |
| $V_{HYSL}$ | Low-voltage inhibit reset/recover hysteresis — low range | — | ±40 | — | mV | — |
| $V_{BG}$ | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | — |
| $t_{LPO}$ | Internal low power oscillator period — factory trimmed | 900 | 1000 | 1100 | µs | — |

1. Rising thresholds are falling threshold + hysteresis voltage

## 2.2.3 Voltage and current operating behaviors

**Table 7. Voltage and current operating behaviors**

| Symbol | Description | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{OH}$ | Output high voltage — Normal drive pad (except $\overline{\text{RESET}}$) | | | | 1, 2 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = –5 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = –1.5 mA | $V_{DD}$ – 0.5 | — | V | |
| $V_{OH}$ | Output high voltage — High drive pad (except RESET_b) | | | | 1, 2 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OH}$ = –18 mA | $V_{DD}$ – 0.5 | — | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OH}$ = –6 mA | $V_{DD}$ – 0.5 | — | V | |
| $I_{OHT}$ | Output high current total for all ports | — | 100 | mA | |
| $V_{OL}$ | Output low voltage — Normal drive pad | | | | 1 |
| | • 2.7 V ≤ $V_{DD}$ ≤ 3.6 V, $I_{OL}$ = 5 mA | — | 0.5 | V | |
| | • 1.71 V ≤ $V_{DD}$ ≤ 2.7 V, $I_{OL}$ = 1.5 mA | — | 0.5 | V | |

*Table continues on the next page...*

2. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode.
6. No brownout

## Table 10. Low power mode peripheral adders — typical value

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| $I_{IREFSTEN4MHz}$ | 4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled. | 56 | 56 | 56 | 56 | 56 | 56 | µA |
| $I_{IREFSTEN32KHz}$ | 32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled. | 52 | 52 | 52 | 52 | 52 | 52 | µA |
| $I_{EREFSTEN4MHz}$ | External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled. | 206 | 228 | 237 | 245 | 251 | 258 | uA |
| $I_{EREFSTEN32KHz}$ | External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.<br>• VLLS1<br>• VLLS3<br>• LLS<br>• VLPS<br>• STOP | <br>440<br>440<br>490<br>510<br>510 | <br>490<br>490<br>490<br>560<br>560 | <br>540<br>540<br>540<br>560<br>560 | <br>560<br>560<br>560<br>560<br>560 | <br>570<br>570<br>570<br>610<br>610 | <br>580<br>580<br>680<br>680<br>680 | nA |
| $I_{CMP}$ | CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption. | 22 | 22 | 22 | 22 | 22 | 22 | µA |
| $I_{RTC}$ | RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption. | 432 | 357 | 388 | 475 | 532 | 810 | nA |
| $I_{UART}$ | UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.<br>• MCGIRCLK (4 MHz internal reference clock)<br>• OSCERCLK (4 MHz external crystal) | <br>66<br>214 | <br>66<br>237 | <br>66<br>246 | <br>66<br>254 | <br>66<br>260 | <br>66<br>268 | µA |

*Table continues on the next page...*

**Table 10. Low power mode peripheral adders — typical value (continued)**

| Symbol | Description | Temperature (°C) | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | -40 | 25 | 50 | 70 | 85 | 105 | |
| $I_{TPM}$ | TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.<br>• MCGIRCLK (4 MHz internal reference clock)<br>• OSCERCLK (4 MHz external crystal) | 86<br>235 | 86<br>256 | 86<br>265 | 86<br>274 | 86<br>280 | 86<br>287 | µA |
| $I_{BG}$ | Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode. | 45 | 45 | 45 | 45 | 45 | 45 | µA |
| $I_{ADC}$ | ADC peripheral adder combining the measured values at $V_{DD}$ and $V_{DDA}$ by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions. | 366 | 366 | 366 | 366 | 366 | 366 | µA |

### 2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

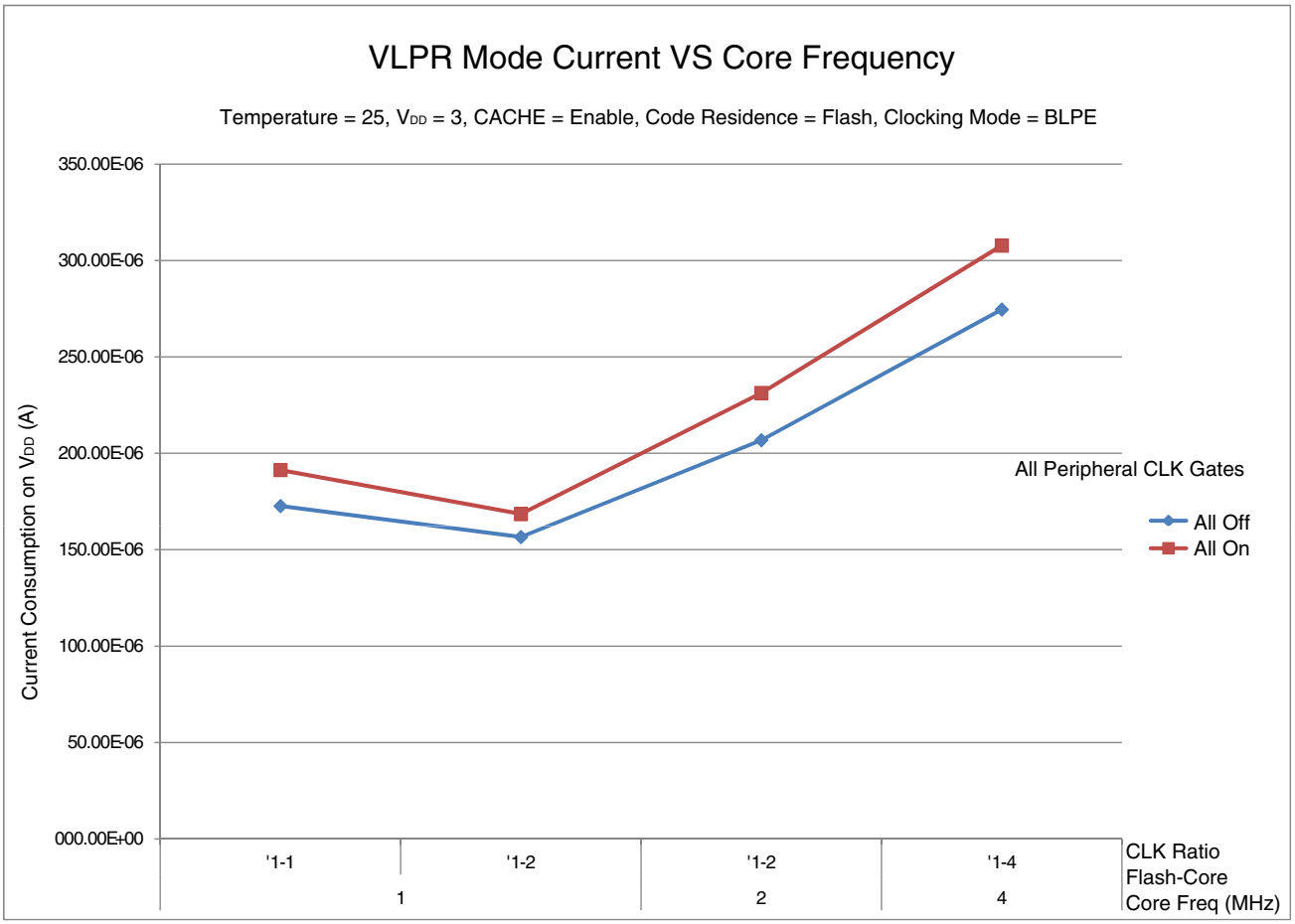



**Figure 3. VLPR mode current vs. core frequency**

## 2.2.6 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on **freescale.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

### 2.2.7 Capacitance attributes

**Table 11. Capacitance attributes**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | — | 7 | pF |

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

**Table 12. Device clock specifications**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| Normal run mode | | | | |
| $f_{SYS}$ | System and core clock | — | 48 | MHz |
| $f_{BUS}$ | Bus clock | — | 24 | MHz |
| $f_{FLASH}$ | Flash clock | — | 24 | MHz |
| $f_{LPTMR}$ | LPTMR clock | — | 24 | MHz |
| VLPR and VLPS modes[1] | | | | |
| $f_{SYS}$ | System and core clock | — | 4 | MHz |
| $f_{BUS}$ | Bus clock | — | 1 | MHz |
| $f_{FLASH}$ | Flash clock | — | 1 | MHz |
| $f_{LPTMR}$ | LPTMR clock[2] | — | 24 | MHz |
| $f_{ERCLK}$ | External reference clock | — | 16 | MHz |
| $f_{LPTMR\_ERCLK}$ | LPTMR external reference clock | — | 16 | MHz |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | — | 16 | MHz |
| $f_{TPM}$ | TPM asynchronous clock | — | 8 | MHz |
| $f_{UART0}$ | UART0 asynchronous clock | — | 8 | MHz |

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

**Table 16. SWD full voltage range electricals (continued)**

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | • Serial wire debug | 20 | — | ns |
| J4 | SWD_CLK rise and fall times | — | 3 | ns |
| J9 | SWD_DIO input data setup time to SWD_CLK rise | 10 | — | ns |
| J10 | SWD_DIO input data hold time after SWD_CLK rise | 0 | — | ns |
| J11 | SWD_CLK high to SWD_DIO data valid | — | 32 | ns |
| J12 | SWD_CLK high to SWD_DIO high-Z | 5 | — | ns |

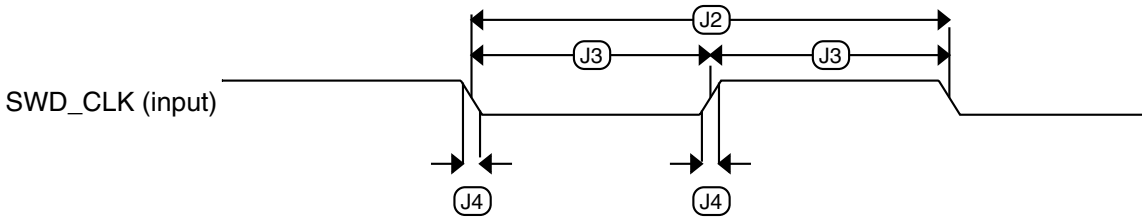



**Figure 4. Serial wire clock input timing**

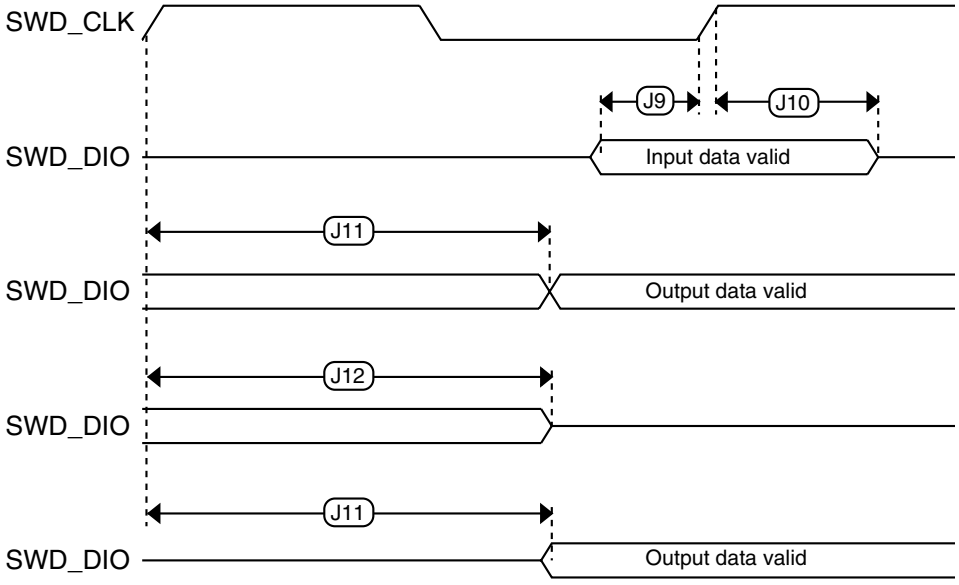



**Figure 5. Serial wire data timing**

## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG specifications

**Table 17. MCG specifications**

| Symbol | Description | | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| $f_{ints\_ft}$ | Internal reference frequency (slow clock) — factory trimmed at nominal $V_{DD}$ and 25 °C | | — | 32.768 | — | kHz | |
| $f_{ints\_t}$ | Internal reference frequency (slow clock) — user trimmed | | 31.25 | — | 39.0625 | kHz | |
| $\Delta_{fdco\_res\_t}$ | Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTRIM] and C4[SCFTRIM] | | — | ± 0.3 | ± 0.6 | $\%f_{dco}$ | 1 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over voltage and temperature | | — | +0.5/-0.7 | ± 3 | $\%f_{dco}$ | 1, 2 |
| $\Delta f_{dco\_t}$ | Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C | | — | ± 0.4 | ± 1.5 | $\%f_{dco}$ | 1, 2 |
| $f_{intf\_ft}$ | Internal reference frequency (fast clock) — factory trimmed at nominal $V_{DD}$ and 25 °C | | — | 4 | — | MHz | |
| $\Delta f_{intf\_ft}$ | Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal $V_{DD}$ and 25 °C | | — | +1/-2 | ± 3 | $\%f_{intf\_ft}$ | 2 |
| $f_{intf\_t}$ | Internal reference frequency (fast clock) — user trimmed at nominal $V_{DD}$ and 25 °C | | 3 | — | 5 | MHz | |
| $f_{loc\_low}$ | Loss of external clock minimum frequency — RANGE = 00 | | (3/5) x $f_{ints\_t}$ | — | — | kHz | |
| $f_{loc\_high}$ | Loss of external clock minimum frequency — | | (16/5) x $f_{ints\_t}$ | — | — | kHz | |
| FLL | | | | | | | |
| $f_{fll\_ref}$ | FLL reference frequency range | | 31.25 | — | 39.0625 | kHz | |
| $f_{dco}$ | DCO output frequency range | Low range (DRS = 00) 640 × $f_{fll\_ref}$ | 20 | 20.97 | 25 | MHz | 3, 4 |
| | | Mid range (DRS = 01) 1280 × $f_{fll\_ref}$ | 40 | 41.94 | 48 | MHz | |
| $f_{dco\_t\_DMX32}$ | DCO output frequency | Low range (DRS = 00) 732 × $f_{fll\_ref}$ | — | 23.99 | — | MHz | 5, 6 |
| | | Mid range (DRS = 01) | — | 47.97 | — | MHz | |

*Table continues on the next page...*

#### 3.3.2.2 Oscillator frequency specifications

**Table 19. Oscillator frequency specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $f_{osc\_lo}$ | Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00) | 32 | — | 40 | kHz | |
| $f_{osc\_hi\_1}$ | Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01) | 3 | — | 8 | MHz | |
| $f_{osc\_hi\_2}$ | Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x) | 8 | — | 32 | MHz | |
| $f_{ec\_extal}$ | Input clock frequency (external clock mode) | — | — | 48 | MHz | 1, 2 |
| $t_{dc\_extal}$ | Input clock duty cycle (external clock mode) | 40 | 50 | 60 | % | |
| $t_{cst}$ | Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0) | — | | — | ms | 3, 4 |
| | Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1) | — | | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0) | — | 0.6 | — | ms | |
| | Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1) | — | 1 | — | ms | |

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

## 3.4 Memories and memory interfaces

### 3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. ADC conversion clock < 3 MHz

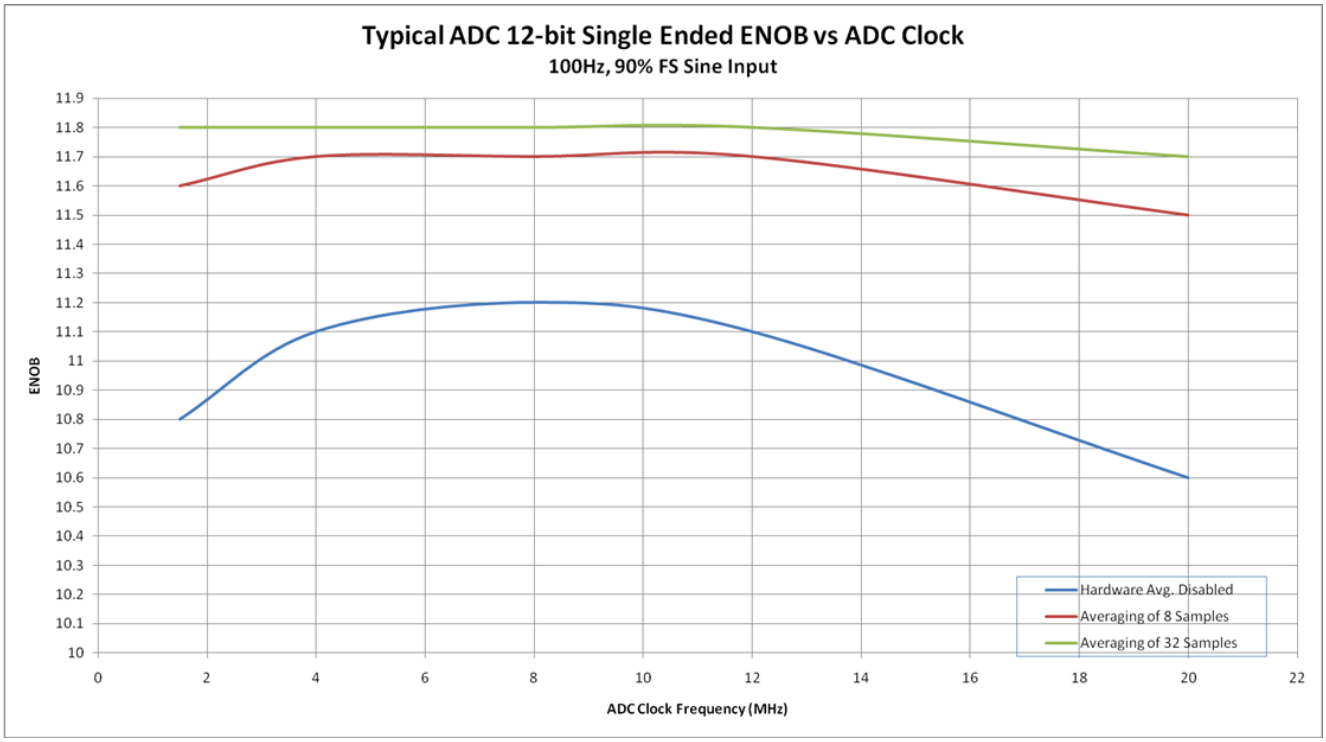


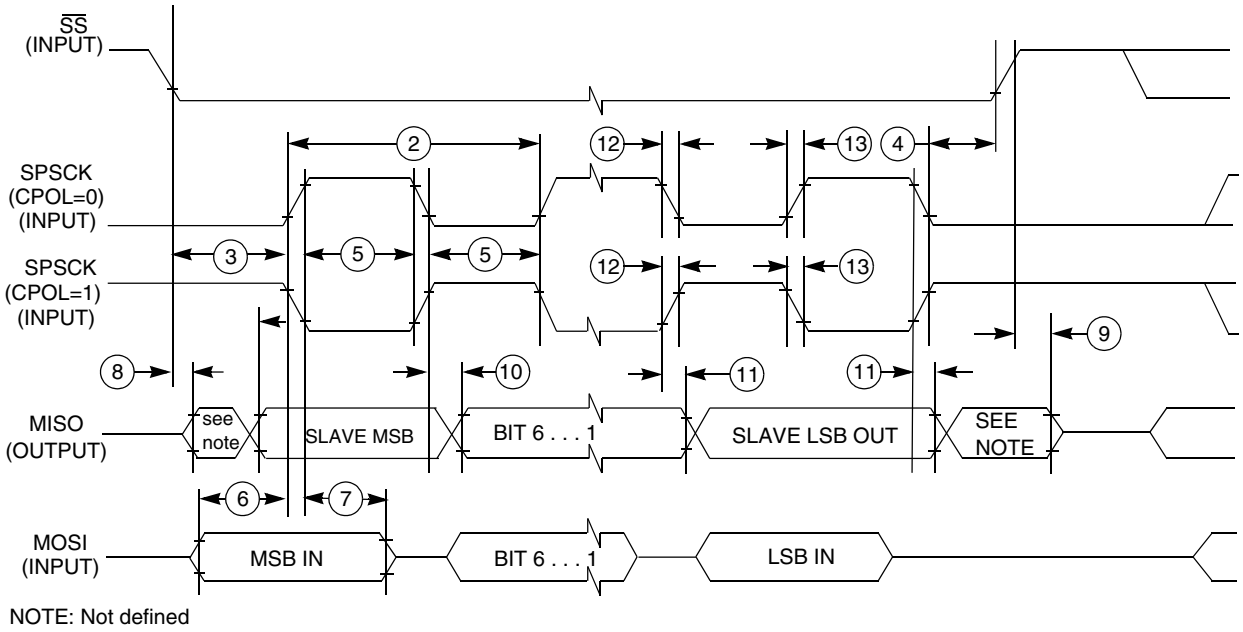

**Figure 7. Typical ENOB vs. ADC_CLK for 12-bit single-ended mode**

## 3.6.2 CMP and 6-bit DAC electrical specifications

**Table 26. Comparator and 6-bit DAC electrical specifications**

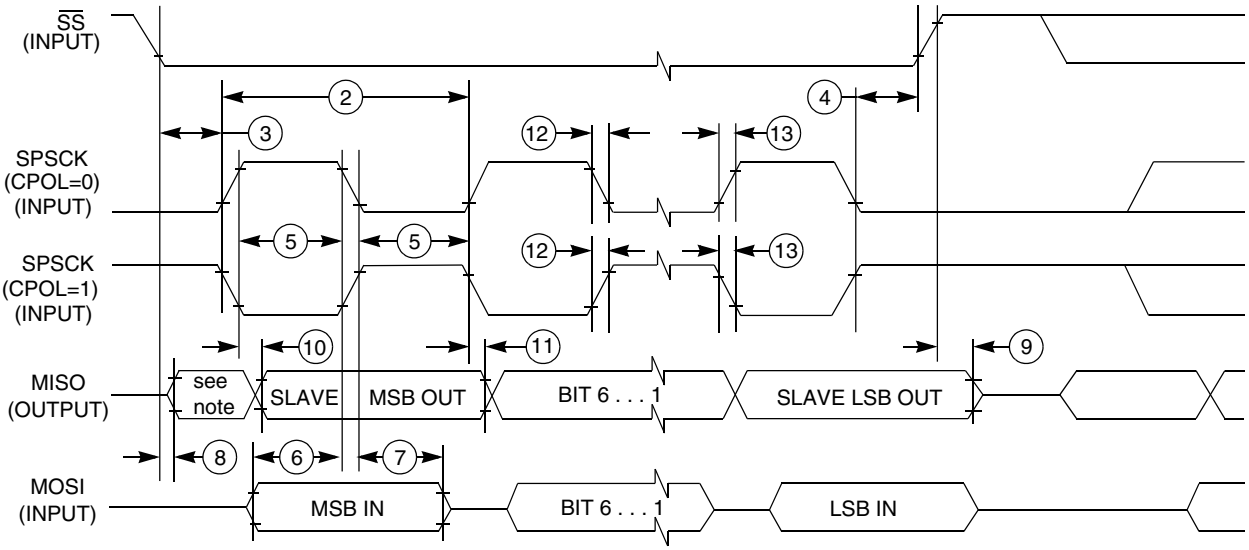
| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.71 | — | 3.6 | V |
| $I_{DDHS}$ | Supply current, high-speed mode (EN = 1, PMODE = 1) | — | — | 200 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN = 1, PMODE = 0) | — | — | 20 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS}$ | — | $V_{DD}$ | V |
| $V_{AIO}$ | Analog input offset voltage | — | — | 20 | mV |
| $V_H$ | Analog comparator hysteresis[1] | | | | |
| | • CR0[HYSTCTR] = 00 | — | 5 | — | mV |
| | • CR0[HYSTCTR] = 01 | — | 10 | — | mV |

*Table continues on the next page...*




NOTE: Not defined

**Figure 12. SPI slave mode timing (CPHA = 0)**




NOTE: Not defined

**Figure 13. SPI slave mode timing (CPHA = 1)**

## 3.8.2 Inter-Integrated Circuit Interface (I2C) timing

**Table 31. I2C timing**

| Characteristic | Symbol | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| SCL Clock Frequency | $f_{SCL}$ | 0 | 100 | 0 | 400[1] | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated. | $t_{HD}$; STA | 4 | — | 0.6 | — | µs |
| LOW period of the SCL clock | $t_{LOW}$ | 4.7 | — | 1.3 | — | µs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 4 | — | 0.6 | — | µs |
| Set-up time for a repeated START condition | $t_{SU}$; STA | 4.7 | — | 0.6 | — | µs |
| Data hold time for I²C bus devices | $t_{HD}$; DAT | 0[2] | 3.45[3] | 0[4] | 0.9[2] | µs |
| Data set-up time | $t_{SU}$; DAT | 250[5] | — | 100[3], [6] | — | ns |
| Rise time of SDA and SCL signals | $t_r$ | — | 1000 | 20 +0.1$C_b$[7] | 300 | ns |
| Fall time of SDA and SCL signals | $t_f$ | — | 300 | 20 +0.1$C_b$[6] | 300 | ns |
| Set-up time for STOP condition | $t_{SU}$; STO | 4 | — | 0.6 | — | µs |
| Bus free time between STOP and START condition | $t_{BUF}$ | 4.7 | — | 1.3 | — | µs |
| Pulse width of spikes that must be suppressed by the input filter | $t_{SP}$ | N/A | N/A | 0 | 50 | ns |

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only achieved when using the High drive pins (see Voltage and current operating behaviors) or when using the Normal drive pins and VDD ≥ 2.7 V
2. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I²C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.
7. $C_b$ = total capacitance of the one bus line in pF.

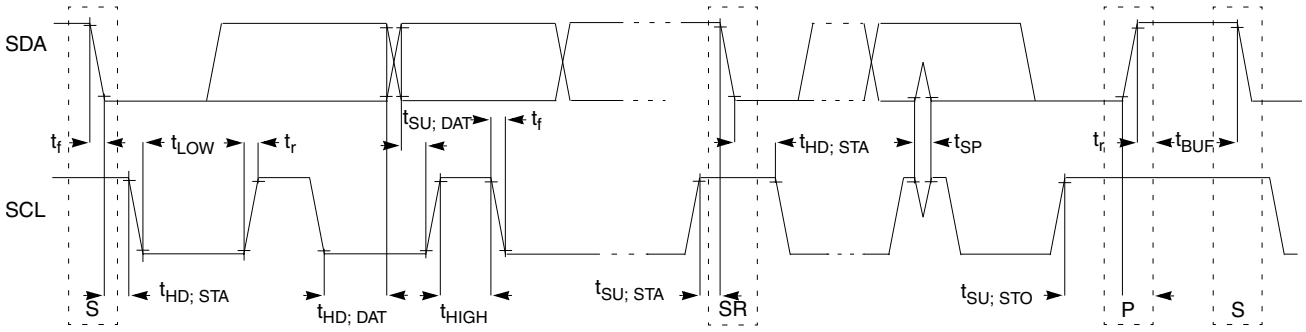



**Figure 14. Timing definition for fast and standard mode devices on the I²C bus**

### 3.8.3 UART

See General switching specifications.

# 4 Dimensions

## 4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **freescale.com** and perform a keyword search for the drawing's document number:

| If you want the drawing for this package | Then use this document number |
|---|---|
| 24-pin QFN | 98ASA00474D |
| 32-pin QFN | 98ASA00473D |
| 32-pin LQFP | 98ASH70029A |
| 48-pin LQFP | 98ASH00962A |

# 5 Pinout

## 5.1 KL04 signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

| 48 LQFP | 32 QFN | 32 LQFP | 24 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | PTB6/ IRQ_2/ LPTMR0_ALT3 | DISABLED | DISABLED | PTB6/ IRQ_2/ LPTMR0_ALT3 | TPM0_CH3 | TPM_CLKIN1 |
| 2 | 2 | 2 | 2 | PTB7/ IRQ_3 | DISABLED | DISABLED | PTB7/ IRQ_3 | TPM0_CH2 | |
| 3 | – | – | – | PTA14 | DISABLED | DISABLED | PTA14 | | TPM_CLKIN0 |
| 4 | – | – | – | PTA15 | DISABLED | DISABLED | PTA15 | | CLKOUT |

| 48 LQFP | 32 QFN | 32 LQFP | 24 QFN | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 |
|---|---|---|---|---|---|---|---|---|---|
| 33 | 21 | 21 | — | PTA10/<br>IRQ_12 | DISABLED | DISABLED | PTA10/<br>IRQ_12 | | |
| 34 | 22 | 22 | — | PTA11/<br>IRQ_13 | DISABLED | DISABLED | PTA11/<br>IRQ_13 | | |
| 35 | 23 | 23 | 17 | PTB3/<br>IRQ_14 | DISABLED | DISABLED | PTB3/<br>IRQ_14 | I2C0_SCL | UART0_TX |
| 36 | 24 | 24 | 18 | PTB4/<br>IRQ_15/<br>LLWU_P6 | DISABLED | DISABLED | PTB4/<br>IRQ_15/<br>LLWU_P6 | I2C0_SDA | UART0_RX |
| 37 | 25 | 25 | 19 | PTB5/<br>IRQ_16 | NMI_b | ADC0_SE1/<br>CMP0_IN1 | PTB5/<br>IRQ_16 | TPM1_CH1 | NMI_b |
| 38 | 26 | 26 | 20 | PTA12/<br>IRQ_17/<br>LPTMR0_ALT2 | ADC0_SE0/<br>CMP0_IN0 | ADC0_SE0/<br>CMP0_IN0 | PTA12/<br>IRQ_17/<br>LPTMR0_ALT2 | TPM1_CH0 | TPM_CLKIN0 |
| 39 | 27 | 27 | — | PTA13 | DISABLED | DISABLED | PTA13 | | |
| 40 | 28 | 28 | — | PTB12 | DISABLED | DISABLED | PTB12 | | |
| 41 | — | — | — | PTA19 | DISABLED | DISABLED | PTA19 | | SPI0_SS_b |
| 42 | — | — | — | PTB15 | DISABLED | DISABLED | PTB15 | SPI0_MOSI | SPI0_MISO |
| 43 | — | — | — | PTB16 | DISABLED | DISABLED | PTB16 | SPI0_MISO | SPI0_MOSI |
| 44 | — | — | — | PTB17 | DISABLED | DISABLED | PTB17 | TPM_CLKIN1 | SPI0_SCK |
| 45 | 29 | 29 | 21 | PTB13 | ADC0_SE13 | ADC0_SE13 | PTB13 | TPM1_CH1 | RTC_CLKOUT |
| 46 | 30 | 30 | 22 | PTA0/<br>IRQ_0/<br>LLWU_P7 | SWD_CLK | ADC0_SE12/<br>CMP0_IN2 | PTA0/<br>IRQ_0/<br>LLWU_P7 | TPM1_CH0 | SWD_CLK |
| 47 | 31 | 31 | 23 | PTA1/<br>IRQ_1/<br>LPTMR0_ALT1 | RESET_b | DISABLED | PTA1/<br>IRQ_1/<br>LPTMR0_ALT1 | TPM_CLKIN0 | RESET_b |
| 48 | 32 | 32 | 24 | PTA2 | SWD_DIO | DISABLED | PTA2 | CMP0_OUT | SWD_DIO |

## 5.2 KL04 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see KL04 signal multiplexing and pin assignments.

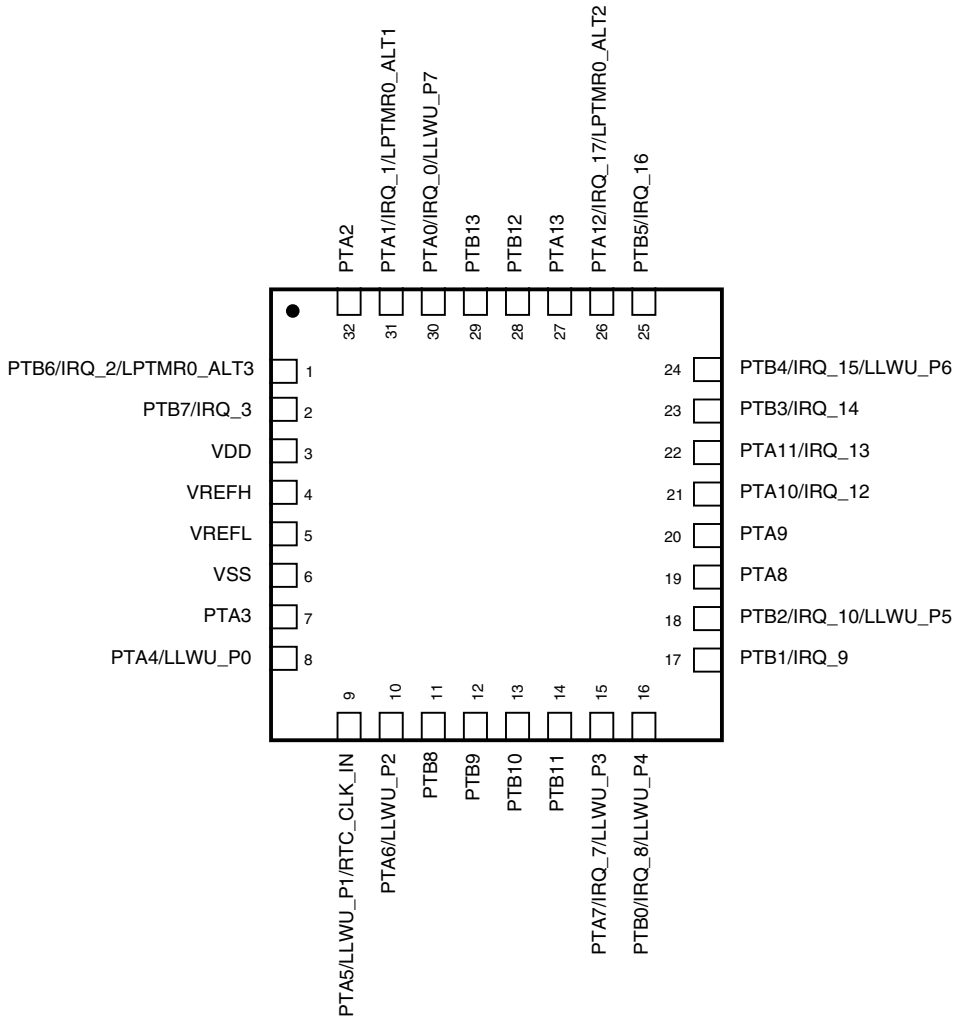



**Figure 17. KL04 32-pin QFN pinout diagram**

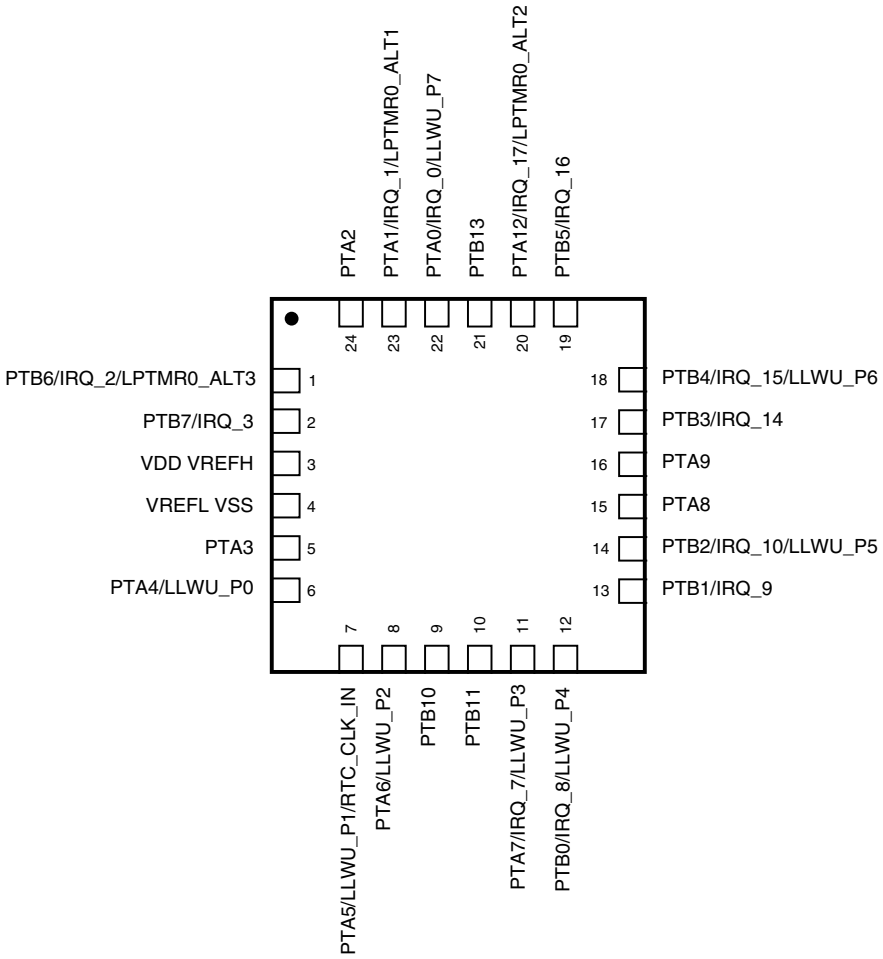



**Figure 18. KL04 24-pin QFN pinout diagram**

# 6 Ordering parts

## 6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: PKL04 and MKL04

# 7 Part identification

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

## 8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

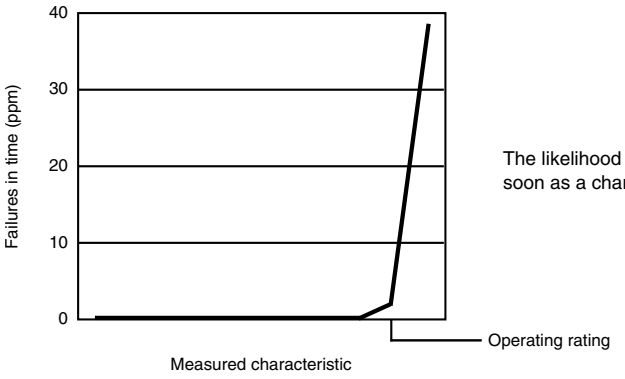
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 8.4.1 Example

This is an example of an operating rating:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 8.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

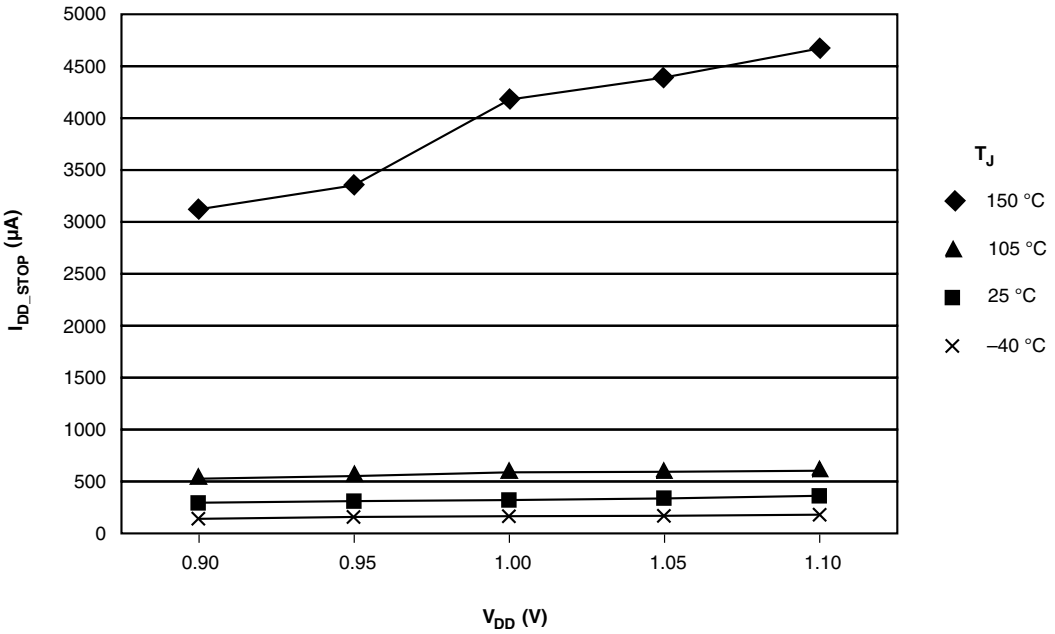
### 8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{WP}$ | Digital I/O weak pullup/pulldown current | 10 | 70 | 130 | µA |

### 8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:




## 8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

**Table 33. Typical value conditions**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient temperature | 25 | °C |
| $V_{DD}$ | 3.3 V supply voltage | 3.3 | V |

# 9 Revision history

The following table provides a revision history for this document.

**Table 34. Revision history**

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| 2 | 9/2012 | Initial public release. |
| 3 | 11/2012 | Completed all the TBDs. |
| 4 | 3/2014 | • Updated the front page and restructured the chapters<br>• Added a note to the $I_{LAT}$ in the ESD handling ratings<br>• Updated Voltage and current operating ratings<br>• Added $V_{ODPU}$ in the Voltage and current operating requirements<br>• Updated Voltage and current operating behaviors<br>• Updated Power mode transition operating behaviors<br>• Updated Power consumption operating behaviors<br>• Updated Capacitance attributes<br>• Updated footnote in the Device clock specifications<br>• Updated $t_{ersall}$ in the Flash timing specifications — commands<br>• Updated Temp sensor slope and voltage and added a note to them in the 12-bit ADC electrical characteristics<br>• Removed $T_A$ in the 12-bit DAC operating requirements<br>• Added Inter-Integrated Circuit Interface (I2C) timing |