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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	Audio Record/Playback
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (145kB)
Controller Series	-
RAM Size	12K x 8
Interface	I ² C, IrDA, LIN, SPI, UART/USART
Number of I/O	8
Voltage - Supply	2.5V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/isd9160cfi

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2 FEATURES

- Core
 - ARM® Cortex™-M0 core runs up to 49MHz.
 - One 24-bit System tick timer for operating system support.
 - Supports a variety of low power sleep and power down modes.
 - Single-cycle 32-bit hardware multiplier.
 - NVIC (Nested Vector Interrupt Controller) for 32 interrupt inputs, each with 4-levels of priority.
 - Serial Wire Debug (SWD) support with 2 watchpoints/4 breakpoints.
- Power Management
 - Wide operating voltage range from 2.4V to 5.5V.
 - Power management Unit (PMU) providing four levels of power control.
 - Deep Power Down (DPD) mode with sub micro-amp leakage (<1μA).
 - Wakeup from Deep Power Down via dedicated WAKEUP pin or timed operation from internal low power 16kHz oscillator.
 - Standby mode with limited RAM retention and RTC operation (<10μA).
 - Wakeup from Standby can be from any GPIO interrupt, RTC or BOD.
 - Sleep mode with minimal dynamic power consumption.
 - 3V LDO for operation of external 3V devices such as serial flash.
- Flash EPROM Memory
 - 68/100/145K bytes Flash EPROM for program code and data storage.
 - 4KB of flash can be configured as boot sector for ISP loader.
 - Support In-system program (ISP) and In-circuit program (ICP) application code update
 - 1K byte page erase for flash
 - Configurable boundary to delineate code and data flash.
 - Support 2 wire In-circuit Programming (ICP) update from SWD ICE interface
- SRAM Memory
 - 12K bytes embedded SRAM.
- Clock Control
 - One high speed and two low speed oscillators providing flexible selection for different applications. No external components necessary.
 - Built-in trimmable oscillator with range of 16-49MHz. Factory trimmed within 1% to settings of 49.152MHz and 32.768MHz. User trimmable with in-built frequency measurement block (OSCFM) using reference clock of 32kHz crystal or external reference source.
 - Ultra-low power (<1uA) 16kHz oscillator for watchdog and wakeup from power-down or sleep operation.
 - External 32kHz crystal input for RTC function and low power system operation.
- GPIO
 - Four I/O modes:
 - ◆ Quasi bi-direction
 - ◆ Push-Pull output
 - ◆ Open-Drain output
 - ◆ Input only with high impedance
 - TTL/Schmitt trigger input selectable.
 - I/O pin can be configured as interrupt source with edge/level setting.
 - Switchable pull-up.
- Audio Analog to Digital converter
 - Sigma Delta ADC with configurable decimation filter and 16 bit output.
 - 92dB Signal-to-Noise (SNR) performance.
 - Programmable gain amplifier with 32 steps from -12 to 35.25dB in 0.75dB steps.
 - Boost gain stage of 26dB, giving maximum total gain of 61dB.

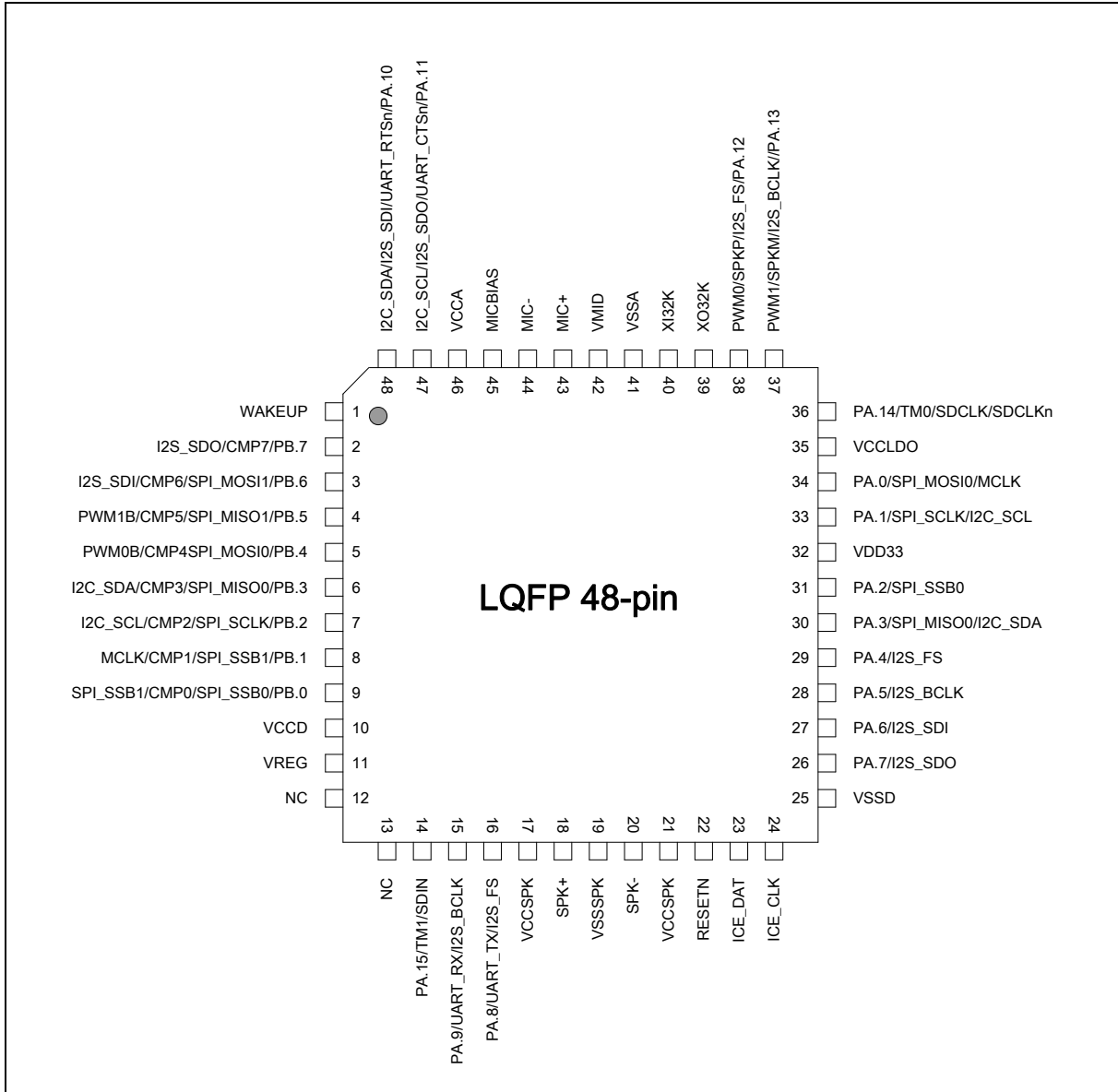
- Input selectable from dedicated MIC pins or analog enabled GPIO.
- Programmable biquad filter to support multiple sample rates from 8-32kHz.
- DMA support for minimal CPU intervention.
- Differential Audio PWM Output (DPWM)
 - Direct connection of speaker
 - 1W drive capability into 8Ω load.
 - High efficiency 88%
 - Configurable up-sampling to support sample rates from 8-32kHz.
 - DMA support for minimal CPU intervention.
- Timers
 - Two timers with 8-bit pre-scaler and 24-bit resolution.
 - Counter auto reload.
- Watch Dog Timer
 - Default ON/OFF by configuration setting
 - Multiple clock sources
 - 8 selectable time out period from micro seconds to seconds (depending on clock source)
 - WDT can wake up power down/sleep.
 - Interrupt or reset selectable on watchdog time-out.
- RTC
 - Real Time Clock counter (second, minute, hour) and calendar counter (day, month, year)
 - Alarm registers (second, minute, hour, day, month, year)
 - Selectable 12-hour or 24-hour mode
 - Automatic leap year recognition
 - Time tick and alarm interrupts.
 - Device wake up function.
 - Supports software compensation of crystal frequency by compensation register (FCR)
- PWM/Capture
 - Built-in up to two 16-bit PWM generators provide two PWM outputs or one complementary paired PWM outputs.
 - The PWM generator equipped with a clock source selector, a clock divider, an 8-bit pre-scaler and Dead-Zone generator for complementary paired PWM.
 - PWM interrupt synchronous to PWM period.
 - 16-bit digital Capture timers (shared with PWM timers) provide rising/falling capture inputs.
 - Support Capture interrupt
- UART
 - UART ports with flow control (TX, RX, CTS and RTS)
 - 8-byte FIFO.
 - Support IrDA (SIR) and LIN function
 - Programmable baud-rate generator up to 1/16 of system clock.
- SPI
 - Master up to 20 Mbps / Slave up to 10 Mbps.
 - Support MICROWIRE/SPI master/slave mode (SSP)
 - Full duplex synchronous serial data transfer
 - Variable length of transfer data from 1 to 32 bits
 - MSB or LSB first data transfer
 - 2 slave/device select lines when used in master mode.
 - Hardware CRC calculation module available for CRC calculation of data stream.
 - DMA support for burst transfers.
- I2C
 - Master/Slave up to 1Mbit/s
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master).

- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Programmable clock allowing versatile rate control.
- I2C-bus controller supports multiple address recognition.
- I²S
 - Interface with external audio CODEC.
 - Operate as either master or slave.
 - Capable of handling 8, 16, 24 and 32 bit word sizes
 - Mono and stereo audio data supported
 - I²S and MSB justified data format supported
 - Two 8 word FIFO data buffers are provided, one for transmit and one for receive
 - Generates interrupt requests when buffer levels cross a programmable boundary
 - Supports DMA requests, for transmit and receive
- Brown-out detector
 - With 8 levels: 2.1V, 2.2V, 2.4V, 2.5V, 2.625V, 2.8V, 3.0V, and 4.6V
 - Supports time-multiplex operation to minimize power consumption.
 - Supports Brownout Interrupt and Reset option
- Built in Low Dropout Voltage Regulator (LDO)
 - Capable of delivering 30mA load current.
 - Configurable for output voltage of 1.8V, 2.4V, 3.0V and 3.3V
 - Eight GPIO (GPIOA<7:0>) operate from LDO voltage domain allowing direct interface to, for example, 3V SPI Flash.
 - Can be bypassed and voltage domain supplied directly from system power.
- Additional Features
 - Over temperature alarm. Can generate interrupt if device exceeds safe operating temperature.
 - Temperature proportional voltage source which can be routed to ADC for temperature measurements.
 - Digital Microphone interface.
- Operating Temperature: -40C~85C
- Package:
 - All Green package (RoHS)
 - ◆ LQFP 48-pin
 - ◆ QFN 33-pin

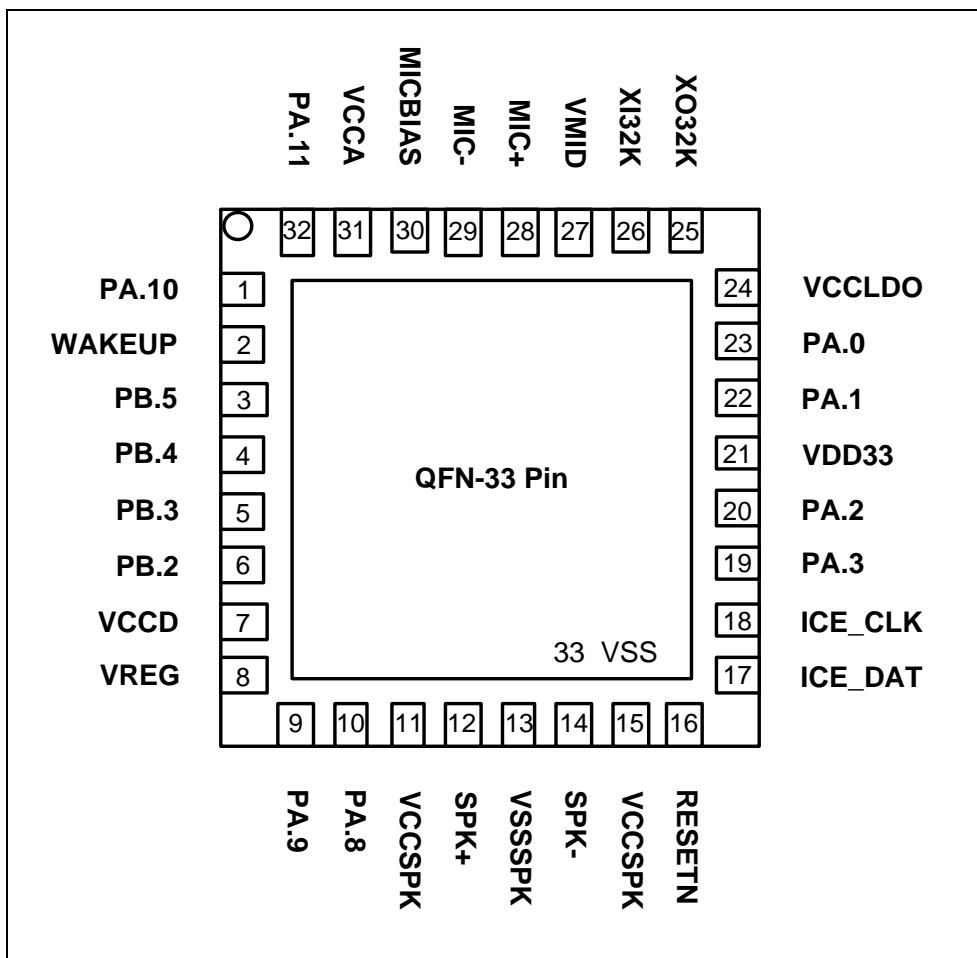
3 PART INFORMATION AND PIN CONFIGURATION

3.1 Pin Configuration

3.1.1 ISD9100 LQFP 48 pin



3.1.2 ISD9100 QFN 33 pin



3.1.3 Pin Description

The ISD9100 is a low pin count device where many pins are configurable to alternative functions. All General Purpose Input/Output (GPIO) pins can be configured to alternate functions as described in the table below.

Pin No.		Pin Name	Pin Type	Alt CFG	Description
LQFP 48	QFN 33				
1	2	WAKEUP	I		Pull low to wake part from deep power down
2	-	PB.7	A/I/O	0	General purpose input/output pin, analog capable; Port B, bit 7
		I2S_SDO	O	1	Serial Data Output for I2S interface
		CMP7	AIO	2	Configure as relaxation oscillator for capacitive touch sensing
3	-	PB.6	A/I/O	0	General purpose input/output pin, analog capable; Port B, bit 6
		I2S_SDI	I	1	Serial Data Input for I2S interface
		CMP6	AIO	2	Configure as relaxation oscillator for capacitive touch sensing
		SPI_MOSI1	O	3	Master Out, Slave In channel 1 for SPI interface
4	3	PB.5	A/I/O	0	General purpose input/output pin, analog capable; Port B, bit 5
		PWM1B	O	1	PWM channel 1 complementary output pin
		CMP5	AIO	2	Configure as relaxation oscillator for capacitive touch sensing
		SPI_MISO1	I	3	Master In, Slave Out channel 1 for SPI interface
5	4	PB.4	A/I/O	0	General purpose input/output pin, analog capable; Port B, bit 4
		PWM0B	O	1	PWM channel 0 complementary output pin
		CMP4	AIO	2	Configure as relaxation oscillator for capacitive touch sensing
		SPI_MOSI0	O	3	Master Out, Slave In channel 0 for SPI interface
6	5	PB.3	A/I/O	0	General purpose input/output pin, analog capable; Port B, bit 3
		I2C_SDA	I/O	1	Serial Data, I2C interface
		CMP3	AIO	2	Configure as relaxation oscillator for capacitive touch sensing
		SPI_MISO0	I	3	Master In, Slave Out channel 0 for SPI interface
7	6	PB.2	A/I/O	0	General purpose input/output pin, analog capable; Port B, bit 2
		I2C_SCL	I/O	1	Serial Clock, I2C interface
		CMP2	AIO	2	Configure as relaxation oscillator for capacitive touch sensing
		SPI_SCLK	I/O	3	Serial Clock for SPI interface
8	-	PB.1	A/I/O	0	General purpose input/output pin, analog capable; Port B, bit 1. Triggers external interrupt 1 (EINT1/IRQ3)
		MCLK	O	1	Master clock output for synchronizing external device
		CMP1	AIO	2	Configure as relaxation oscillator for capacitive touch sensing
		SPI_SSB1	O	3	Slave Select Bar 1 for SPI interface

Pin No.		Pin Name	Pin Type	Alt CFG	Description
LQFP 48	QFN 33				
9	-	PB.0	A/I/O	0	General purpose input/output pin, analog capable; Port B, bit 0. Triggers external interrupt 0 (EINT0/IRQ2)
		SPI_SSB1	O	3	Slave Select Bar 1 for SPI interface
		CMP0	AIO	2	Configure as relaxation oscillator for capacitive touch sensing
		SPI_SSB0	I/O	3	Slave Select Bar 0 for SPI interface
10	7	VCCD	P		Main Digital Supply for Chip. Supplies all IO except analog, Speaker Driver and PA<7:0>
11	8	VREG	P		Logic regulator output decoupling pin. A 1µF capacitor returning to VSSD must be placed on this pin.
12	-	NC			Should remain unconnected.
13	-	NC			Should remain unconnected.
14	-	PA.15	I/O	0	General purpose input/output pin; Port A, bit 15
		TM1	I	1	External input to Timer 1
		SDIN	I	2	Sigma Delta bit stream input for digital MIC mode
15	9	PA.9	I/O	0	General purpose input/output pin; Port A, bit 9
		UART_RX	I	1	Receive channel of UART
		I2S_BCLK	I/O	2	Bit Clock for I2S interface
16	10	PA.8	I/O	0	General purpose input/output pin; Port A, bit 8
		UART_TX	O	1	Transmit channel of UART
		I2S_FS	I/O	2	Frame Sync Clock for I2S interface
17	11	VCCSPK	P		Power Supply for PWM Speaker Driver
18	12	SPK+	O		Positive Speaker Driver Output
19	13	VSSSPK	P		Ground for PWM Speaker Driver
20	14	SPK-	O		Negative Speaker Driver Output
21	15	VCCSPK	P		Power Supply for PWM Speaker Driver
22	16	RESETN	I		External reset input. Pull this pin low to reset device to initial state. Has internal weak pull-up.
23	17	ICE_DAT	I/O		Serial Wire Debug port data pin. Has internal weak pull-up.
24	18	ICE_CLK	I		Serial Wire Debug port clock pin. Has internal weak pull-up.
25	-	VSSD	P		Digital Ground.
26	-	PA.7	I/O	0	General purpose input/output pin; Port A, bit 7
		I2S_SDO	O	1	Serial Data Out for I2S interface
27	-	PA.6	I/O	0	General purpose input/output pin; Port A, bit 6

Pin No.		Pin Name	Pin Type	Alt CFG	Description
LQFP 48	QFN 33				
		I2S_SDI	I	1	Serial Data In for I2S interface
28	-	PA.5	I/O	0	General purpose input/output pin; Port A, bit 5
		I2S_BCLK	I/O	1	Bit Clock for I2S interface
29	-	PA.4	I/O	0	General purpose input/output pin; Port A, bit 4
		I2S_FS	I/O	1	Frame Sync Clock for I2S interface
30	19	PA.3	I/O	0	General purpose input/output pin; Port A, bit 3
		SPI_MISO0	I	1	Master In, Slave Out channel 0 for SPI interface
		I2C_SDA	I/O	2	Serial Data, I2C interface
31	20	PA.2	I/O	0	General purpose input/output pin; Port A, bit 2
		SPI_SSB0	I/O	1	Slave Select Bar 0 for SPI interface
32	21	VDD33	P		LDO Regulator Output. If used, a 1 μ F capacitor must be placed to ground. If not used then tie to VCCD.
33	22	PA.1	I/O	0	General purpose input/output pin; Port A, bit 1
		SPI_SCLK	I/O	1	Serial Clock for SPI interface
		I2C_SCL	I/O	2	Serial Clock, I2C interface
34	23	PA.0	I/O	0	General purpose input/output pin; Port A, bit 2
		SPI_MOSI0	O	1	Master Out, Slave In channel 0 for SPI interface
		MCLK	O	2	Master clock output.
35	24	VCCLDO	P		Power Supply for LDO, should be connected to VCCD
36	-	PA.14	I/O	0	General purpose input/output pin; Port A, bit 14
		SDCLK	O	1	Clock output for digital microphone mode.
		SDCLKn	O	2	Inverse Clock output for digital microphone mode.
37	-	PA.13	I/O	0	General purpose input/output pin; Port A, bit 13
		PWM1	O	1	PWM1 Output.
		SPKM	O	2	Equivalent to SPK-.
		I2S_BCLK	I/O	3	Bit Clock for I2S interface
38	-	PA.12	I/O	0	General purpose input/output pin; Port A, bit 12
		PWM0	O	1	PWM0 Output.
		SPKP	O	2	Equivalent to SPK+
		I2S_FS	I/O	3	Frame Sync Clock for I2S interface
39	25	XO32K	O		32.768kHz Crystal Oscillator Output
40	26	XI32K	I		32.768kHz Crystal Oscillator Input. Max Voltage 1.8V

Pin No.		Pin Name	Pin Type	Alt CFG	Description
LQFP 48	QFN 33				
41		VSSA	AP		Ground for analog circuitry.
42	27	VMID	O		Mid rail reference. Connect 4.7μF to VSSA.
43	28	MIC+	AI		Positive microphone input.
44	29	MIC-	AI		Negative microphone input.
45	30	MICBIAS	AO		Microphone bias output.
46	31	VCCA	AP		Analog power supply.
47	32	PA.11	I/O	0	General purpose input/output pin; Port A, bit 11
		I2C_SCL	I/O	1	Serial Clock, I2C interface
		I2S_SDO	O	2	Serial Data Out I2S interface
		UART_CTSn	I	3	UART Clear to Send Input.
48	-	PA.10	I/O	0	General purpose input/output pin; Port A, bit 10
		I2C_SDA	I/O	1	Serial Data, I2C interface
		I2S_SDI	I	2	Serial Data In I2S interface
		UART_RTSn	O	3	UART Request to Send Output.
-	33	VSS	P		Ground for both digital and analog. Center pad underneath.

Note:

- Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

4 BLOCK DIAGRAM

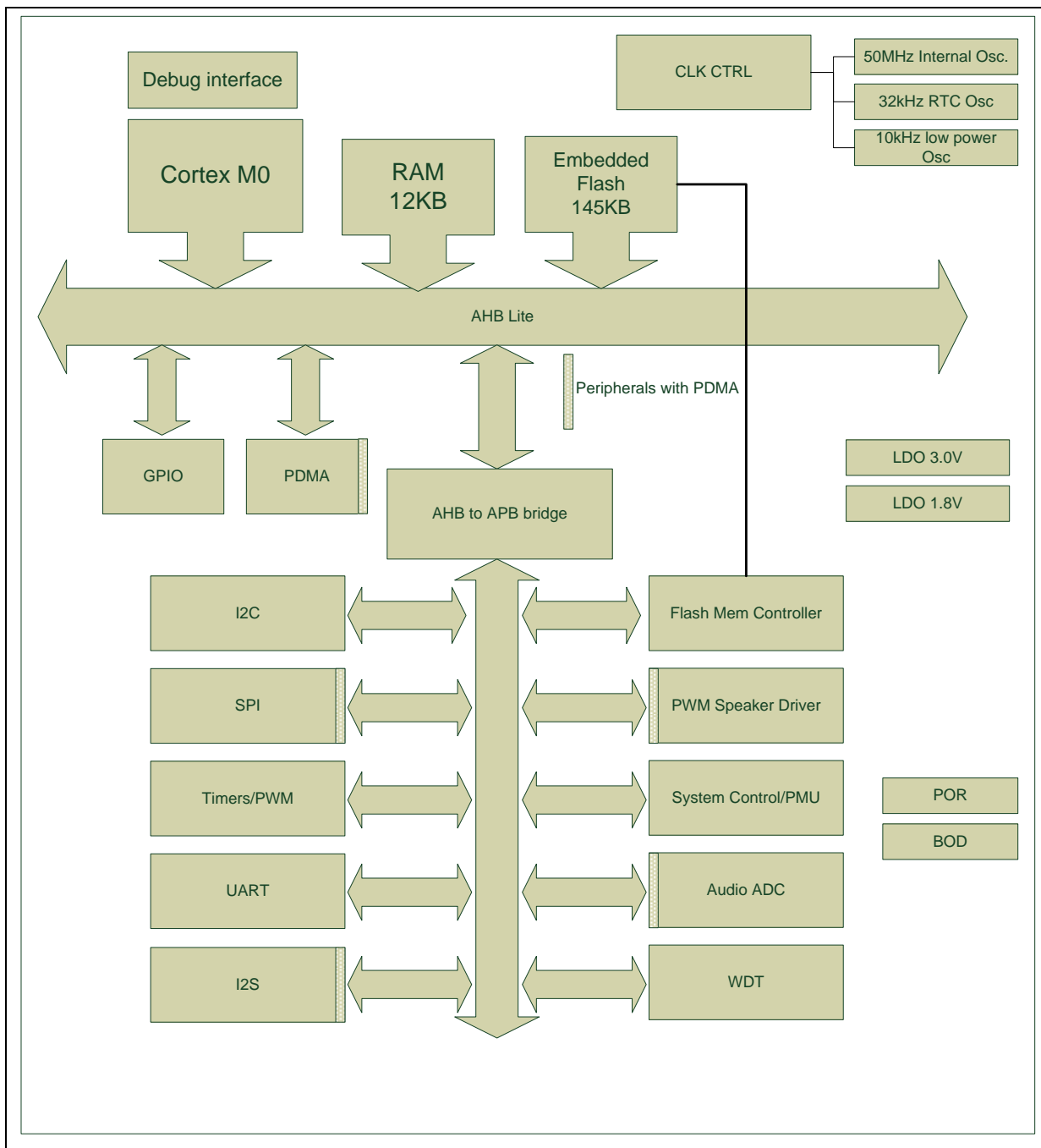
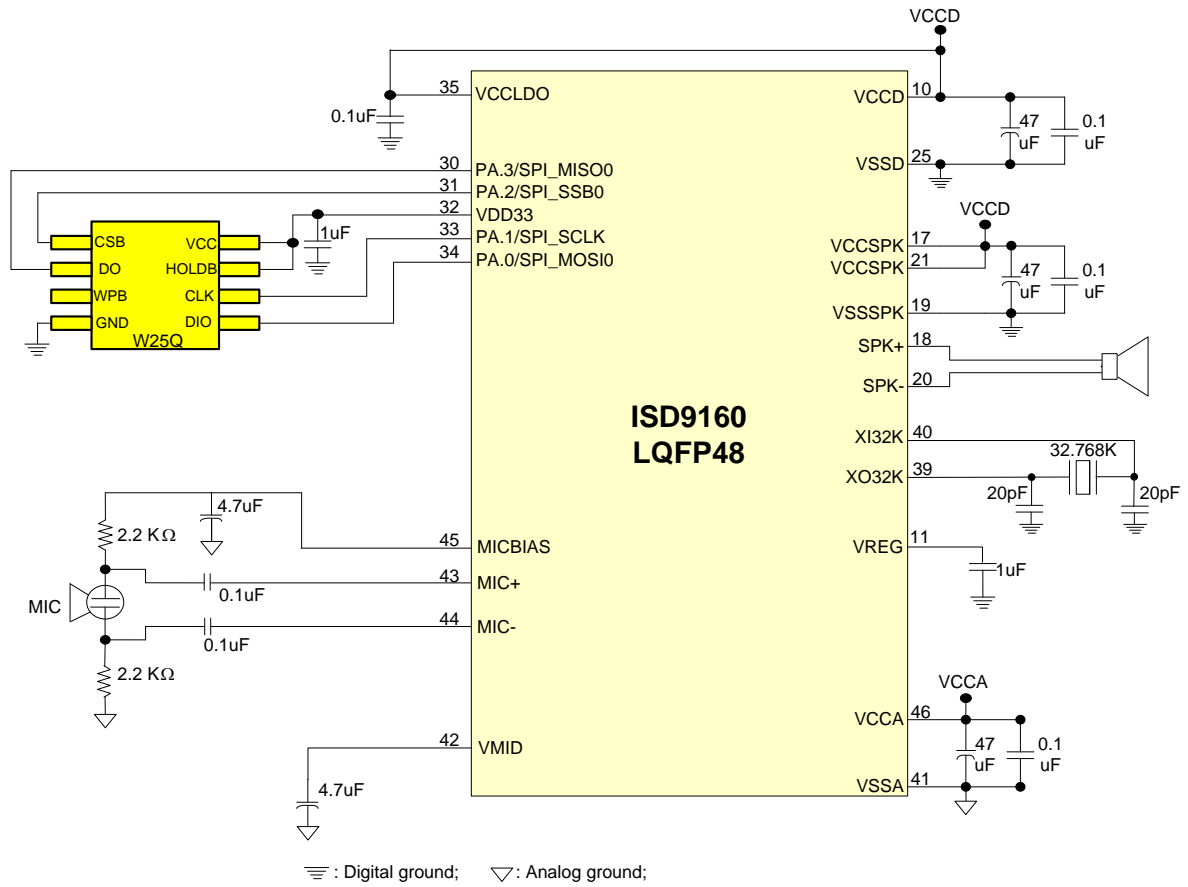


Figure 4-1 ISD9100 Block Diagram

5 APPLICATION DIAGRAM



6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD-VSS	-0.3	+6.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	1/t _{CLCL}	0	40	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V _{DD}		-	120	mA
Maximum Current out of V _{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

6.2 DC Electrical Characteristics

(V_{DD}-V_{SS}=3.3V, T_A = 25°C, F_{OSC} = 49.152 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V _{DD}	2.4		5.5	V	V _{DD} = 2.4V ~ 5.5V up to 49 MHz
Power Ground	V _{SS} AV _{SS}	-0.3			V	
Analog Operating Voltage	AV _{DD}	0		V _{DD}	V	
Analog Reference Voltage	V _{ref}	0		AV _{DD}	V	
Operating Current Normal Run Mode @ 49.152 MHz	I _{DD1}		24.8		mA	V _{DD} = 5.5V, Enable all IP.
	I _{DD2}		19.7		mA	V _{DD} = 5.5V, disable all IP
	I _{DD3}		23.6		mA	V _{DD} = 3V, enable all IP
	I _{DD4}		18.3		mA	V _{DD} = 3V, disable all IP
Operating Current Normal Run Mode @ 32.768Mhz	I _{DD5}		18.8		mA	V _{DD} = 5.5V, Enable all IP.
	I _{DD6}		15.0		mA	V _{DD} = 5.5V, Disable all IP.
	I _{DD7}		17.6		mA	V _{DD} = 3V, Enable all IP.
	I _{DD8}		13.8		mA	V _{DD} = 3V, Disable all IP.

Input Current PA, PB (Quasi-bidirectional mode)	I_{IN1}	-60	-	+15	μA	$V_{DD} = 5.5\text{V}, V_{IN} = 0\text{V}$ or $V_{IN} = V_{DD}$
Input Current at /RESET ^[1]	I_{IN2}	-55	-45	-30	μA	$V_{DD} = 3.3\text{V}, V_{IN} = 0.45\text{V}$
Input Leakage Current PA, PB	I_{LK}	-2	-	+2	μA	$V_{DD} = 5.5\text{V}, 0 < V_{IN} < V_{DD}$
Logic 1 to 0 Transition Current PA~PB (Quasi-bidirectional mode)	$I_{TL}^{[3]}$	-650	-	-200	μA	$V_{DD} = 5.5\text{V}, V_{IN} < 2.0\text{V}$
Input Low Voltage PA, PB (TTL input)	V_{IL1}	-0.3	-	0.8	V	$V_{DD} = 4.5\text{V}$
		-0.3	-	0.6		$V_{DD} = 2.5\text{V}$
Input High Voltage PA, PB (TTL input)	V_{IH1}	2.0	-	$V_{DD} + 0.2$	V	$V_{DD} = 5.5\text{V}$
		1.5	-	$V_{DD} + 0.2$		$V_{DD} = 3.0\text{V}$
Input Low Voltage XT1 ^[*2]	V_{IL3}	0	-	0.8	V	$V_{DD} = 4.5\text{V}$
		0	-	0.4		$V_{DD} = 3.0\text{V}$
Input High Voltage XT1 ^[*2]	V_{IH3}	3.5	-	$V_{DD} + 0.2$	V	$V_{DD} = 5.5\text{V}$
		2.4	-	$V_{DD} + 0.2$		$V_{DD} = 3.0\text{V}$
Input Low Voltage X32I ^[*2]	V_{IL4}	0	-	0.4	V	
Input High Voltage X32I ^[*2]	V_{IH4}	1.7		2.5	V	
Negative going threshold (Schmitt input), /REST	V_{ILS}	-0.5	-	$0.3V_{DD}$	V	
Positive going threshold (Schmitt input), /REST	V_{IHS}	$0.7V_{DD}$	-	$V_{DD} + 0.5$	V	
Hysteresis voltage of PA~PB(Schmitt input)	V_{HY}		$0.2V_{DD}$		V	

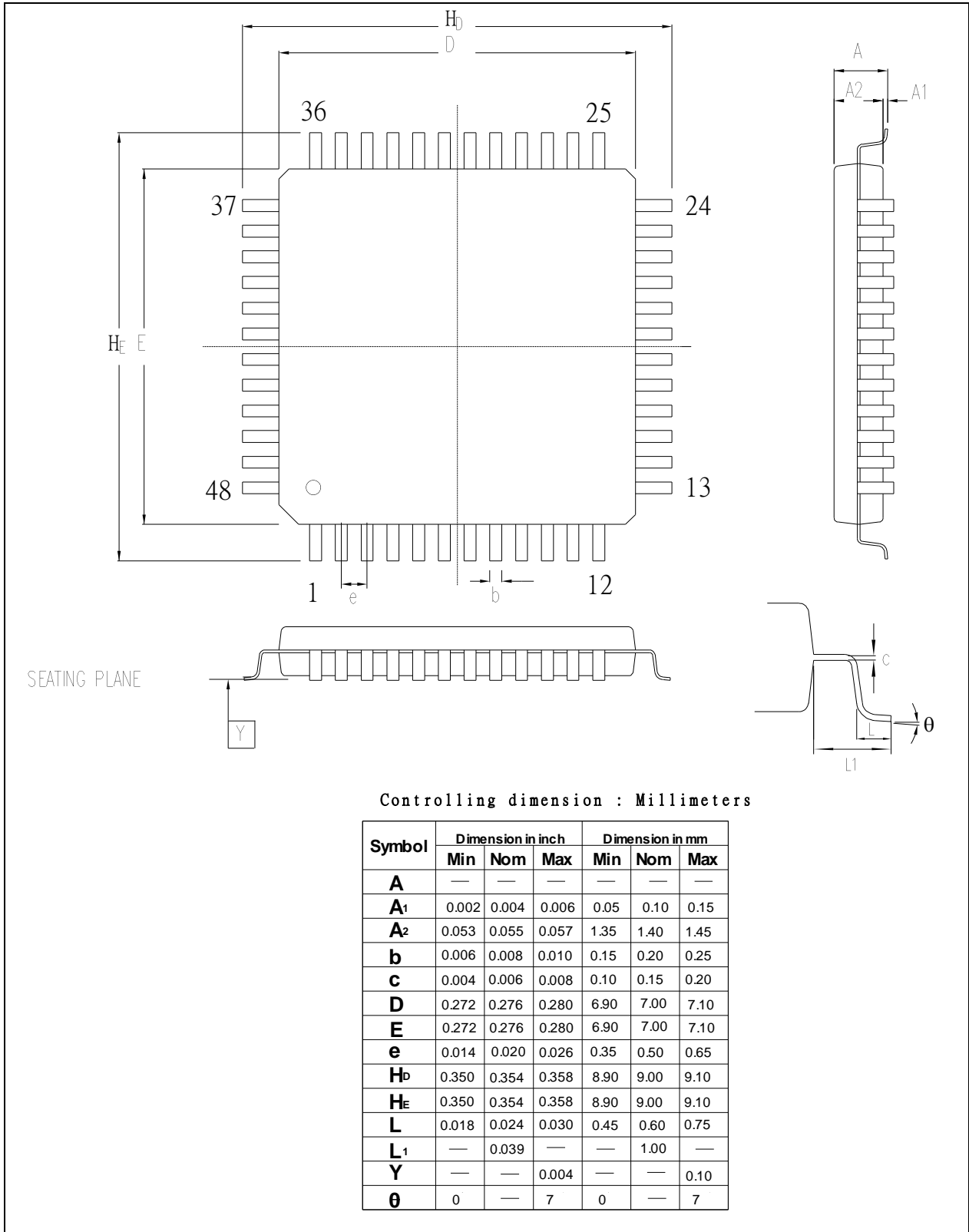
Source Current PA, PB Quasi-bidirectional Mode)	I _{SR11}	-300	-370	-450	μA	V _{DD} = 4.5V, V _S = 2.4V
	I _{SR12}	-50	-70	-90	μA	V _{DD} = 2.7V, V _S = 2.2V
	I _{SR12}	-40	-60	-80	μA	V _{DD} = 2.5V, V _S = 2.0V
Source Current PA, PB (Push-pull Mode)	I _{SR21}	-20	-24	-28	mA	V _{DD} = 4.5V, V _S = 2.4V
	I _{SR22}	-4	-6	-8	mA	V _{DD} = 2.7V, V _S = 2.2V
	I _{SR22}	-3	-5	-7	mA	V _{DD} = 2.5V, V _S = 2.0V
Sink Current PA, PB (Quasi-bidirectional and Push-pull Mode)	I _{SK1}	10	16	20	mA	V _{DD} = 4.5V, V _S = 0.45V
	I _{SK1}	7	10	13	mA	V _{DD} = 2.7V, V _S = 0.45V
	I _{SK1}	6	9	12	mA	V _{DD} = 2.5V, V _S = 0.45V
Brownout voltage with BOV_VL [2:0] =000b	V _{BO2.1}		2.15		V	
Brownout voltage with BOV_VL [2:0] =001b	V _{BO2.2}		2.25		V	
Brownout voltage with BOV_VL [2:0] =010b	V _{BO2.4}		2.45		V	
Brownout voltage with BOV_VL [2:0] =011b	V _{BO2.5}		2.55		V	
Brownout voltage with BOV_VL [2:0] =100b	V _{BO2.7}		2.7		V	
Brownout voltage with BOV_VL [2:0] =101b	V _{BO2.8}		2.8		V	
Brownout voltage with BOV_VL [2:0] =110b	V _{BO3.0}		3.0		V	
Brownout voltage with BOV_VL [2:0] =111b	V _{BO4.5}		4.55		V	

Notes:

1. /REST pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{in} approximates to 2V.

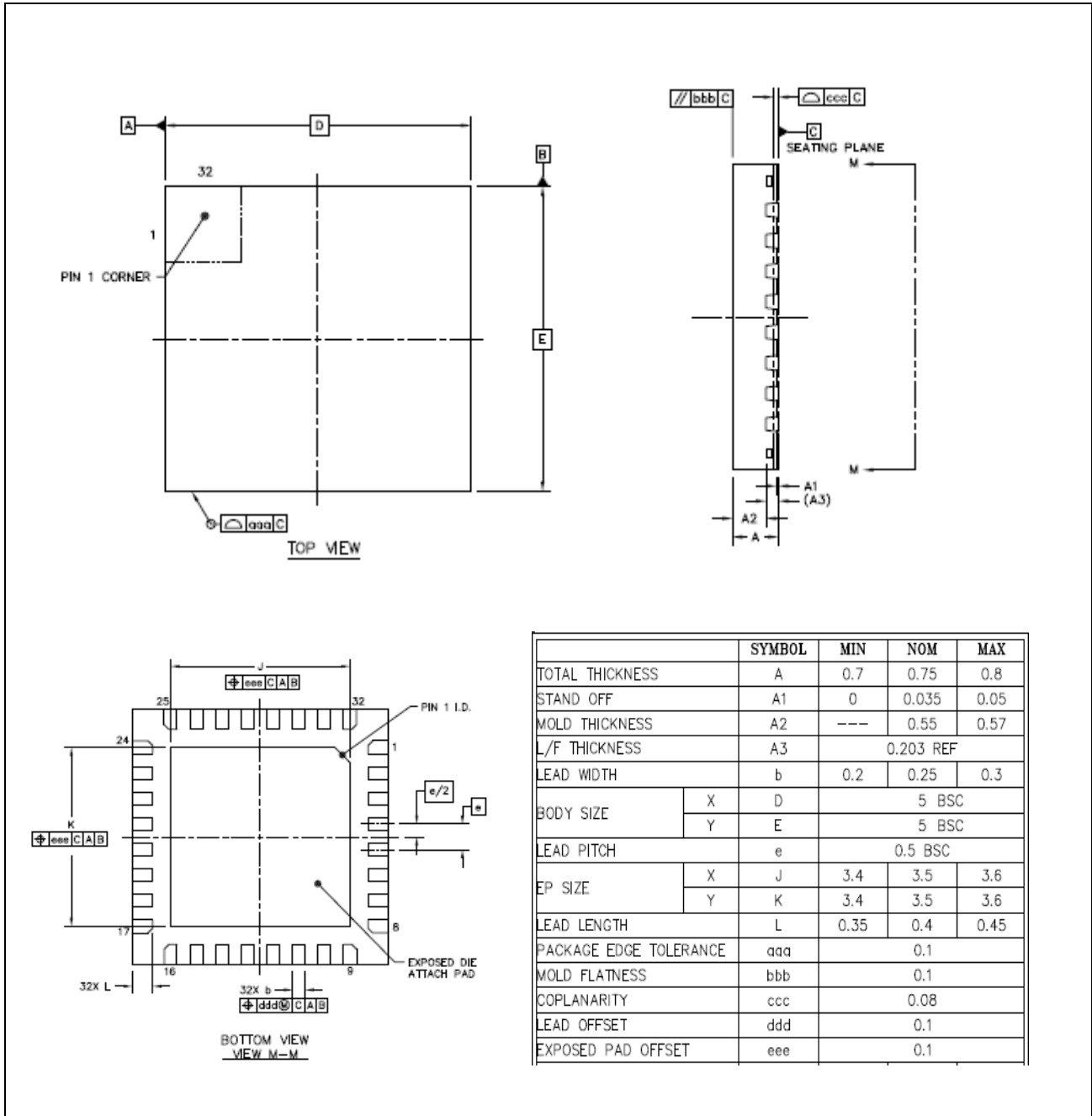
7 PACKAGE DIMENSIONS

7.1.1 48L LQFP (7x7x1.4mm footprint 2.0mm)



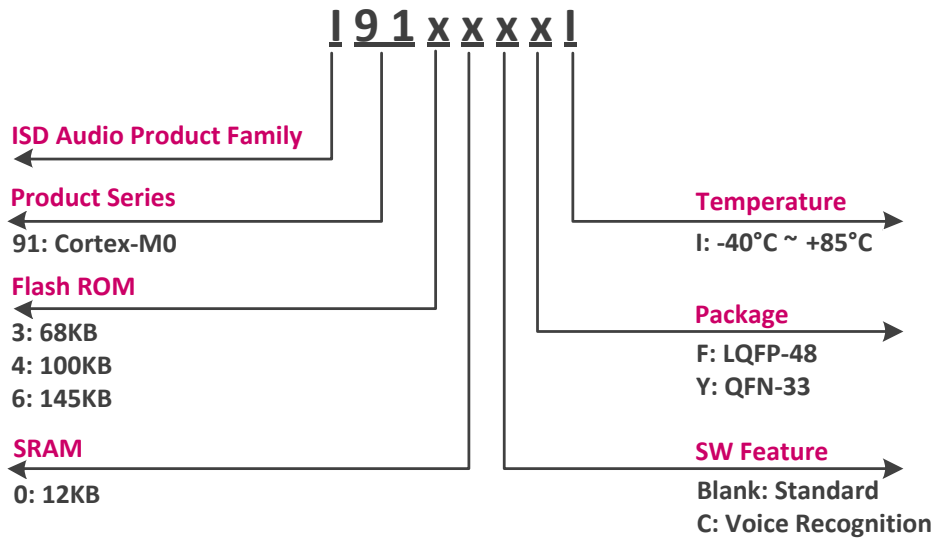
7.1.2 33-pin QFN

5x5 mm², Thickness 0.8mm (MAX), Pitch 0.5 mm (SAW Type), EP SIZE 3.5X3.5 mm



	SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS	A	0.7	0.75	0.8
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	---	0.55	0.57
L/F THICKNESS	A3	0.203 REF		
LEAD WIDTH	b	0.2	0.25	0.3
BODY SIZE	X	D		
	Y	E		
LEAD PITCH	e	0.5 BSC		
EP SIZE	X	J	3.4	3.5
	Y	K	3.4	3.5
LEAD LENGTH	L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.1		
COPLANARITY	ccc	0.08		
LEAD OFFSET	ddd	0.1		
EXPOSED PAD OFFSET	eee	0.1		

8 ORDERING INFORMATION



9 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V0.1	May 25, 2011	-	First Release.
V1.01	Sep 6, 2011	-	<ul style="list-style-type: none"> • Add better description of EINT0/1 and PB0/1 interrupts. • Unify the naming of capacitive touch sensing.
V1.10	Sep 30, 2011	-	<ul style="list-style-type: none"> • Revise the level value of Brown-out detector in Feature. • Correct the maximum voltage of DC Power Supply in section 6.1 Absolute Maximum Ratings
V1.22	Nov 17, 2011	-	<ul style="list-style-type: none"> • Update DC spec. • Add ordering information.
V1.23	Sep 10, 2012		<ul style="list-style-type: none"> • Remove "Preliminary" • Change internal oscillation 10K to 16K • Change minimum voltage (to 2.4V) in chapter 9 Electrical Characteristics
V1.24	July 17, 2013		<ul style="list-style-type: none"> • Change SNR to 92dB • Add RESET low specification in DC characteristic.
V1.25	July 31, 2013		<ul style="list-style-type: none"> • Update RESET timing spec.
V1.30	Oct 24, 2014		<ul style="list-style-type: none"> • Add ISD9130 and ISD9140 into the ISD9100 series.
V1.40	July 20, 2015		<ul style="list-style-type: none"> • Add QFN-33 pin package.
V1.41	Jan 8, 2016		<ul style="list-style-type: none"> • Fix ordering info, QFN-33 pin dimension data.