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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	68
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l38amnfa-v1

1.1.3 Specifications

Tables 1.4 to 1.6 list the Specifications.

Table 1.4 Specifications (1)

Item	Function		Specification
CPU	Central processing unit		R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM/RAM Data flash		Refer to **Tables 1.7 to 1.10 Product Lists**.
Power Supply Voltage Detection	Voltage detection circuit		• Power-on reset • Voltage detection 3 (detection level of voltage detection 0 and voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	R8C/L35M Group	• CMOS I/O ports: 41, selectable pull-up resistor • High current drive ports: 5
		R8C/L36M Group	• CMOS I/O ports: 52, selectable pull-up resistor • High current drive ports: 8
		R8C/L38M Group	• CMOS I/O ports: 68, selectable pull-up resistor • High current drive ports: 8
		R8C/L3AM Group	• CMOS I/O ports: 88, selectable pull-up resistor • High current drive ports: 16
Clock	Clock generation circuits		4 circuits: XIN clock oscillation circuit XCIN clock oscillation circuit (32 kHz) High-speed on-chip oscillator (with frequency adjustment function) Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Division ratio selectable from 1, 2, 4, 8, and 16 • Low-power-consumption modes: Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode, power-off mode
			Real-time clock (timer RE)
Interrupts		R8C/L35M Group	• Number of interrupt vectors: 69 • External Interrupt: 9 ($\overline{\text{INT}}$ × 5, key input × 4) • Priority levels: 7 levels
		R8C/L36M Group	• Number of interrupt vectors: 69 • External Interrupt: 12 ($\overline{\text{INT}}$ × 8, key input × 4) • Priority levels: 7 levels
		R8C/L38M Group	• Number of interrupt vectors: 69 • External Interrupt: 16 ($\overline{\text{INT}}$ × 8, key input × 8) • Priority levels: 7 levels
		R8C/L3AM Group	• Number of interrupt vectors: 69 • External Interrupt: 16 ($\overline{\text{INT}}$ × 8, key input × 8) • Priority levels: 7 levels
Watchdog Timer			• 14 bits × 1 (with prescaler) • Selectable reset start function • Selectable low-speed on-chip oscillator for watchdog timer
DTC (Data Transfer Controller)			• 1 channel • Activation sources: 38 • Transfer modes: 2 (normal mode, repeat mode)

Table 1.5 Specifications (2)

Item	Function	Specification	
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode	
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode	
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)	
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output: 6 pins, sawtooth wave modulation), complementary PWM mode (three-phase waveform output: 6 pins, triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)	
	Timer RE	8 bits × 1 Real-time clock mode (counting of seconds, minutes, hours, days of week), output compare mode	
	Timer RG	16 bits × 1 Phase-counting mode, timer mode (output compare function, input capture function), PWM mode (output: 1 pin)	
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART × 2 channels	
	UART2	Clock synchronous serial I/O/UART, I^2C mode (I^2C-bus), multiprocessor communication function	
Synchronous Serial Communication Unit (SSU)		1 (shared with I^2C-bus)	
I^2C bus		1 (shared with SSU)	
LIN Module		Hardware LIN: 1 channel (timer RA, UART0 used)	
A/D Converter	R8C/L35M Group	10-bit resolution × 12 channels, including sample and hold function, with sweep mode	
	R8C/L36M Group	10-bit resolution × 12 channels, including sample and hold function, with sweep mode	
	R8C/L38M Group	10-bit resolution × 16 channels, including sample and hold function, with sweep mode	
	R8C/L3AM Group	10-bit resolution × 20 channels, including sample and hold function, with sweep mode	
D/A Converter		8-bit resolution × 2 circuits	
Comparator A		• 2 circuits (sheared with voltage monitor 1 and voltage monitor 2) • External reference voltage input available	
Comparator B		2 circuits	
LCD Drive Control Circuit	R8C/L35M Group	Common output: Max. 4 pins Segment output: Max. 24 pins	Bias: 1/2, 1/3 Duty: static, 1/2, 1/3, 1/4
	R8C/L36M Group	Common output: Max. 8 pins Segment output: Max. 32 pins (1)	Bias: 1/2, 1/3, 1/4 Duty: static, 1/2, 1/3, 1/4, 1/8
	R8C/L38M Group	Common output: Max. 8 pins Segment output: Max. 48 pins (1)	
	R8C/L3AM Group	Common output: Max. 8 pins Segment output: Max. 56 pins (1)	
		Voltage multiplier and dedicated regulator integrated	

Note:
1. This applies when four pins are selected for common output.

Table 1.8 Product List for R8C/L36M Group **Current of Jun 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L367MNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	N Version
R5F2L367MNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368MNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368MNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36AMNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36AMNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CMNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CMNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L367MDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	D Version
R5F2L367MDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368MDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368MDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36AMDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36AMDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CMDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CMDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	

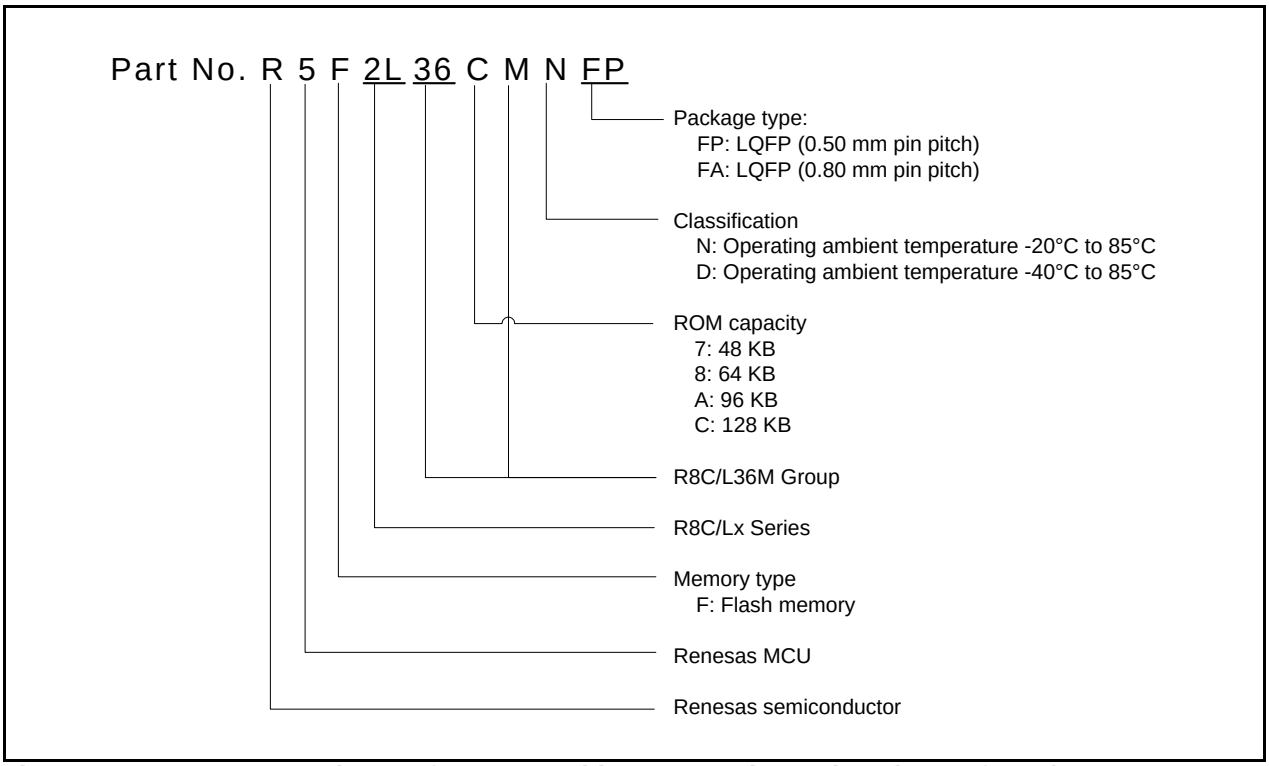


Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/L36M Group

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/L35M Group. Figure 1.6 shows a Block Diagram of R8C/L36M Group. Figure 1.7 shows a Block Diagram of R8C/L38M Group. Figure 1.8 shows a Block Diagram of R8C/L3AM Group.

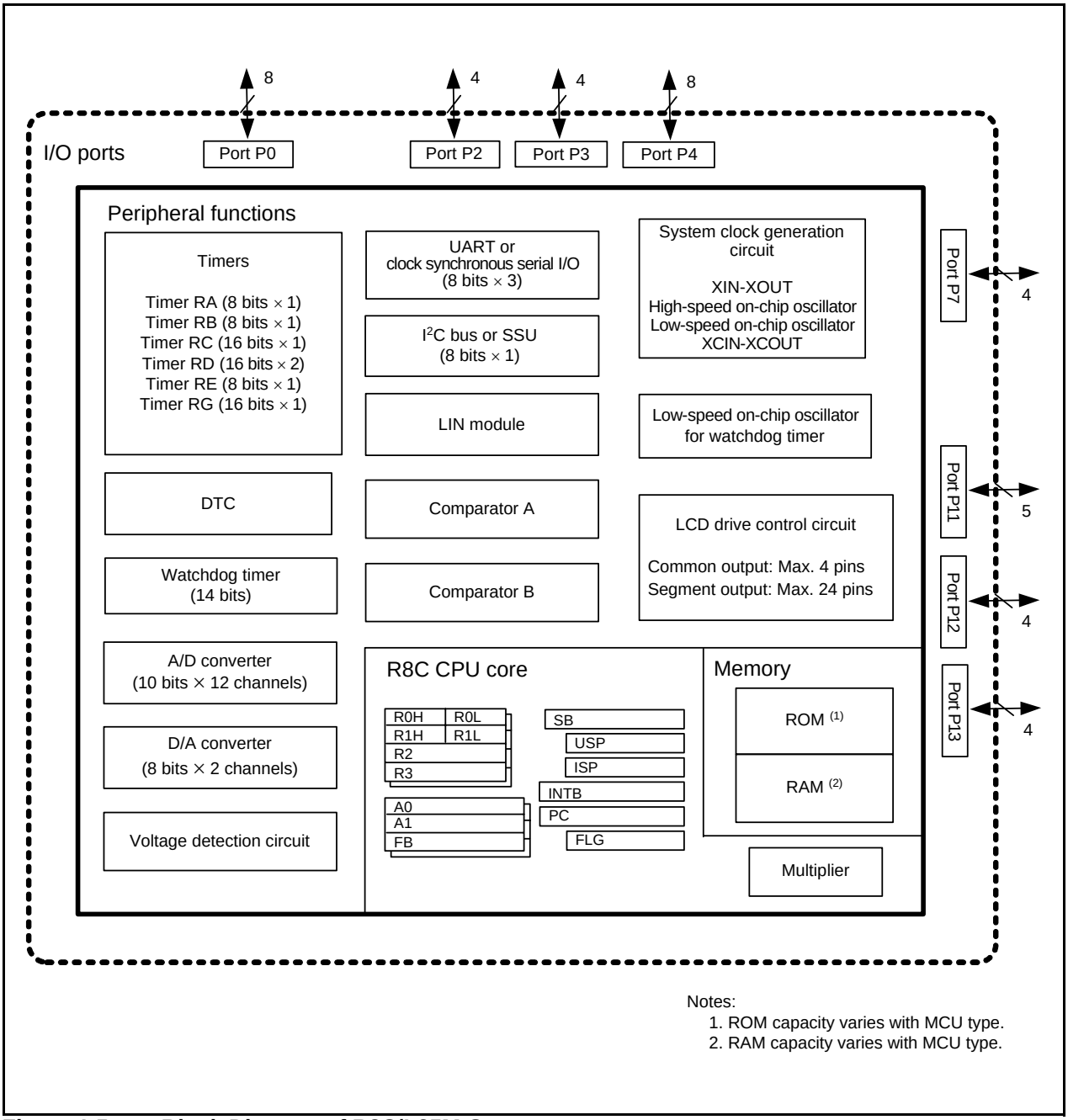


Figure 1.5 Block Diagram of R8C/L35M Group

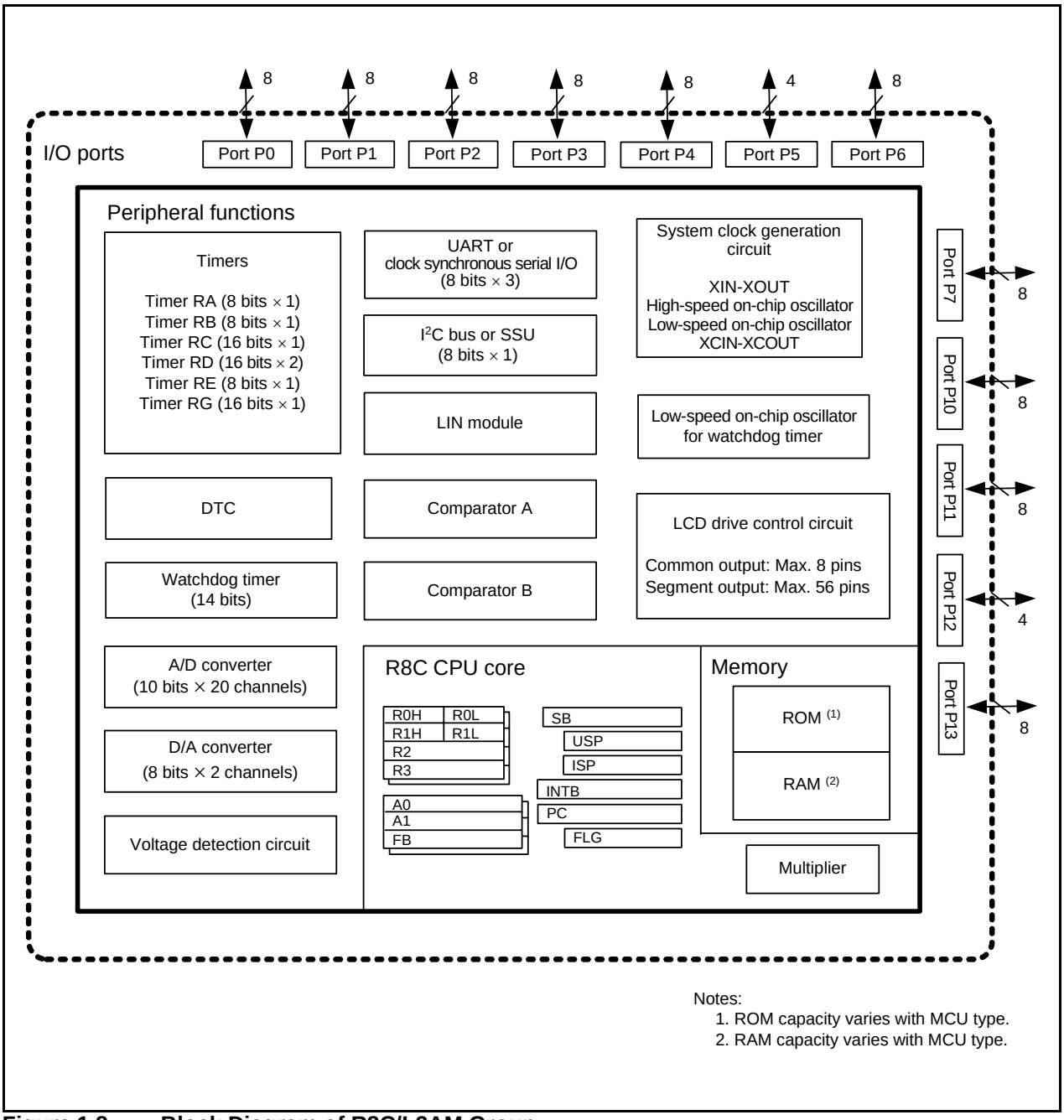
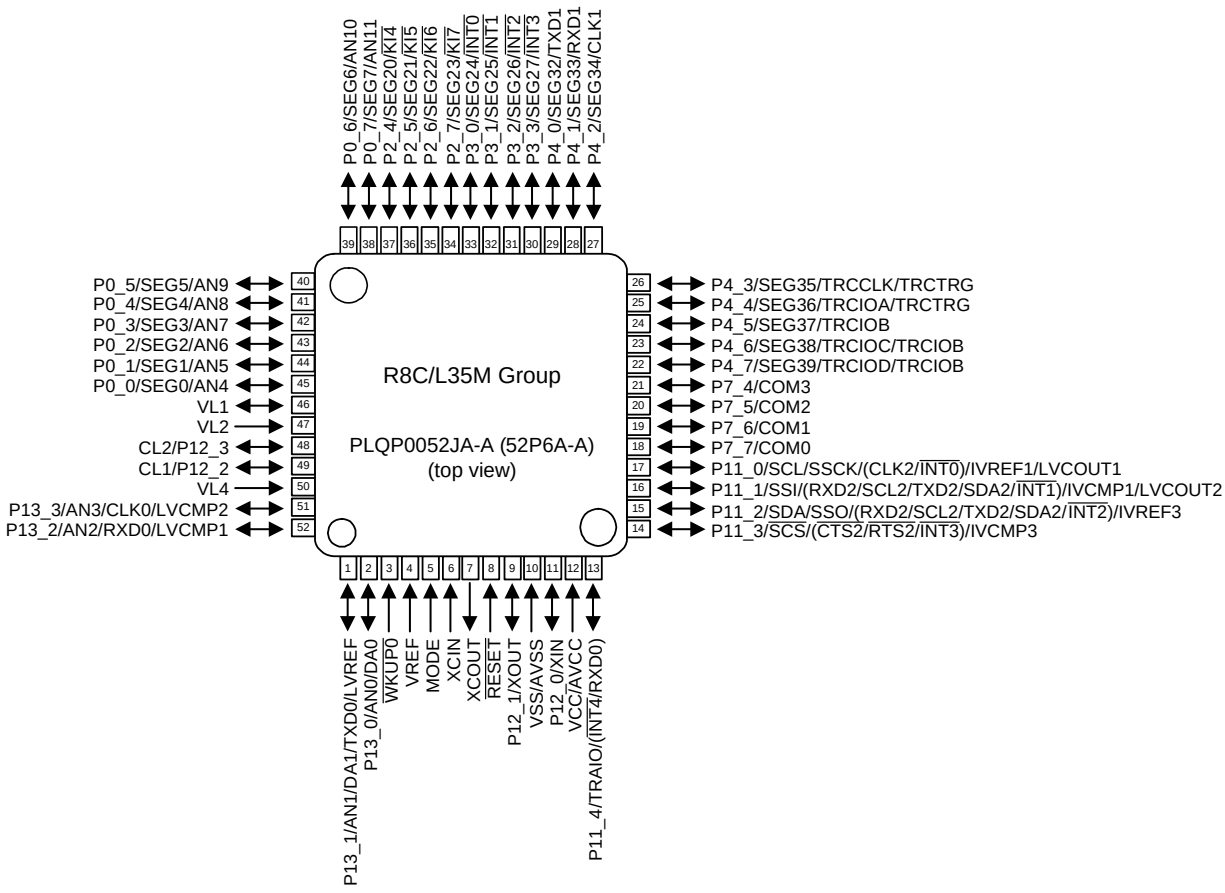


Figure 1.8 Block Diagram of R8C/L3AM Group

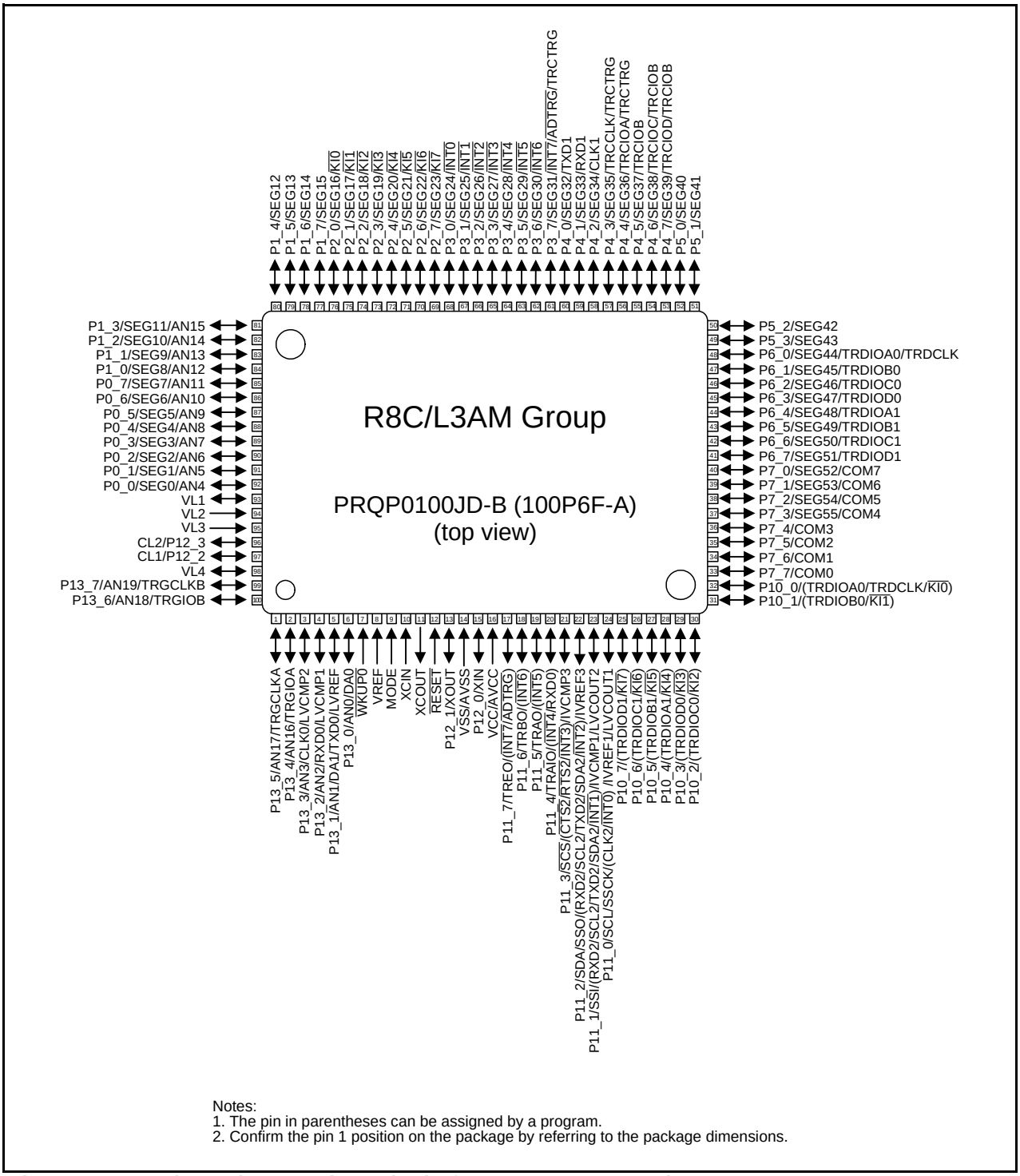
1.4 Pin Assignments

Figures 1.9 to 1.13 show Pin Assignments (Top View). Tables 1.11 to 1.13 list the Pin Name Information by Pin Number.



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.9 Pin Assignment (Top View) of PLQP0052JA-A Package



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.13 Pin Assignment (Top View) of PRQP0100JD-B Package

Table 1.15 Pin Functions for R8C/L3AM Group (2)

Item	Pin Name	I/O Type	Description
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{SCS}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter and the D/A converter
A/D converter	AN0 to AN11	I	A/D converter analog input pins
	$\overline{ADTRG}$	I	A/D external trigger input pin
D/A converter	DA0, DA1	O	D/A converter output pins
Comparator A	LVCMP1, LVCMP2	I	Comparator A analog voltage input pins
	LVREF	I	Comparator A reference voltage input pin
	LVCOUT1, LVCOUT2	O	Comparator A analog output pins
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
Voltage detection circuit	LVCMP2	I	Detection target voltage input pin for voltage detection 2
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0, P5_3, P6_0 to P6_7 P7_0 to P7_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_3, P13_0 to P13_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. Ports P10_0 to P10_7 and P11_0 to P11_7 can be used as LED drive ports.
Segment output	SEG0 to SEG55	O	LCD segment output pins
Common output	COM0 to COM7	O	LCD common output pins
Voltage multiplier capacity connect pins	CL1, CL2	O	Connect pins for the LCD control voltage multiplier
LCD power supply	VL1	I/O	Apply the voltage: $0 \leq VL1 \leq VL2 \leq VL3 \leq VL4$. VL1 can be used as the reference potential input or output pin when setting the voltage multiplier.
	VL2 to VL4	I	

I: Input O: Output I/O: Input and output

Note:

1. Contact the oscillator manufacturer for oscillation characteristics.

Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	After Reset
003Ah	Voltage Monitor 2 Circuit Control Register	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h			
0043h	INT7 Interrupt Control Register	INT7IC	XX00X000b
0044h	INT6 Interrupt Control Register	INT6IC	XX00X000b
0045h	INT5 Interrupt Control Register	INT5IC	XX00X000b
0046h	INT4 Interrupt Control Register	INT4IC	XX00X000b
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h	Timer RD0 Interrupt Control Register	TRD0IC	XXXXX000b
0049h	Timer RD1 Interrupt Control Register	TRD1IC	XXXXX000b
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh	UART2 Transmit Interrupt Control Register	S2TIC	XXXXX000b
004Ch	UART2 Receive Interrupt Control Register	S2RIC	XXXXX000b
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register / IIC bus Interrupt Control Register (2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	INT2 Interrupt Control Register	INT2IC	XX00X000b
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch			
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	UART2 Bus Collision Detection Interrupt Control Register	U2BCNIC	XXXXX000b
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh	Timer RG Interrupt Control Register	TRGIC	XXXXX000b
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h	Voltage monitor 1 / Comparator A1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Voltage monitor 2 / Comparator A2 Interrupt Control Register	VCMP2IC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

Notes:
1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h			
0187h	Timer RG Pin Select Register	TRGPSR	00h
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh	Key Input Pin Select Register	KISR	00h
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR/ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR/ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH/ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL/ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR/ICMR	00010000b/00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER/ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR/ICSR	00h/0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2/SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. Blank spaces are reserved. No access is allowed.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	After Reset
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
01C9h			
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h			
01D1h			
01D2h			
01D3h			
01D4h			
01D5h			
01D6h			
01D7h			
01D8h			
01D9h			
01DAh			
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			
01E0h	Port P0 Pull-Up Control Register	P0PUR	00h
01E1h	Port P1 Pull-Up Control Register	P1PUR	00h
01E2h	Port P2 Pull-Up Control Register	P2PUR	00h
01E3h	Port P3 Pull-Up Control Register	P3PUR	00h
01E4h	Port P4 Pull-Up Control Register	P4PUR	00h
01E5h	Port P5 Pull-Up Control Register	P5PUR	00h
01E6h	Port P6 Pull-Up Control Register	P6PUR	00h
01E7h	Port P7 Pull-Up Control Register	P7PUR	00h
01E8h			
01E9h			
01EAh	Port 10 Pull-Up Control Register	P10PUR	00h
01EBh	Port 11 Pull-Up Control Register	P11PUR	00h
01ECh	Port 12 Pull-Up Control Register	P12PUR	00h
01EDh	Port 13 Pull-Up Control Register	P13PUR	00h
01EEh			
01EFh			
01F0h	Port P10 Drive Capacity Control Register	P10DRR	00h
01F1h	Port P11 Drive Capacity Control Register	P11DRR	00h
01F2h			
01F3h			
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h	Input Threshold Control Register 2	VLT2	00h
01F8h	Comparator B Control Register 0	INTCMP	00h
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh	External Input Enable Register 1	INTEN1	00h
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh	INT Input Filter Select Register 1	INTF1	00h
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KIEN1	00h

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After Reset
0240h	LCD Display Data Register	LRA48L	XXh
0241h		LRA49L	XXh
0242h		LRA50L	XXh
0243h		LRA51L	XXh
0244h		LRA52L	XXh
0245h		LRA53L	XXh
0246h		LRA54L	XXh
0247h		LRA55L	XXh
0248h			
0249h			
024Ah			
024Bh			
024Ch			
024Dh			
024Eh			
024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh			
025Fh			
0260h			
0261h			
0262h			
0263h			
0264h			
0265h			
0266h			
0267h			
0268h			
0269h			
026Ah			
026Bh			
026Ch			
026Dh			
026Eh			
026Fh			
0270h	LCD Display Control Data Register	LRA0H	XXh
0271h		LRA1H	XXh
0272h		LRA2H	XXh
0273h		LRA3H	XXh
0274h		LRA4H	XXh
0275h		LRA5H	XXh
0276h		LRA6H	XXh
0277h		LRA7H	XXh
0278h		LRA8H	XXh
0279h		LRA9H	XXh
027Ah		LRA10H	XXh
027Bh		LRA11H	XXh
027Ch		LRA12H	XXh
027Dh		LRA13H	XXh
027Eh		LRA14H	XXh
027Fh		LRA15H	XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
02C0h			
02C1h			
02C2h			
02C3h			
02C4h			
02C5h			
02C6h			
02C7h			
02C8h			
02C9h			
02CAh			
02CBh			
02CCh			
02CDh			
02CEh			
02CFh			
02D0h			
02D1h			
02D2h			
02D3h			
02D4h			
02D5h			
02D6h			
02D7h			
02D8h			
02D9h			
02DAh			
02DBh			
02DCh			
02DDh			
02DEh			
02DFh			
02E0h			
02E1h			
02E2h			
02E3h			
02E4h			
02E5h			
02E6h			
02E7h			
02E8h			
02E9h			
02EAh			
02EBh			
02ECh			
02EDh			
02EEh			
02EFh			
02F0h			
02F1h			
02F2h			
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh			
02FFh			

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 5.20 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output "H" voltage	Port P10, P11 (1)	I_{OH} = –5 mA	V_{CC} – 0.5	—	V_{CC}	V
		Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	—	—	V
V_{OL}	Output "L" voltage	Port P10, P11 (1)	I_{OL} = 5 mA	—	—	0.5	V
		Other pins	I_{OL} = 1 mA	—	—	0.5	V
		XOUT	I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{INT5}$, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRGCLKA, TRGCLKB, $\overline{TRGIOA}$, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO		0.05	0.4	—	V
		$\overline{RESET}$, $\overline{WKUP0}$		0.1	0.8	—	V
I_{IH}	Input "H" current		VI = 3.0 V, V_{CC} = 3.0 V	—	—	5.0	μA
I_{IL}	Input "L" current		VI = 0 V, V_{CC} = 3.0 V	—	—	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3.0 V	30	100	170	kΩ
R_{fXIN}	Feedback resistance	XIN		—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN		—	14	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.21 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition									Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other		Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed								
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—			—	7.0	14.5	mA
			10 MHz	Off	Off	125 kHz	No division	—			—	3.6	10	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—			—	3.0	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—			—	1.5	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—			—	7.0	14.5	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	—			—	3.0	—	mA
			Off	Off	10 MHz	125 kHz	No division	—			—	4.0	—	mA
			Off	Off	10 MHz	125 kHz	Divide-by-8	—			—	1.7	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1			—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0			—	85	390	μA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0			—	90	400	μA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM		—	50	—	μA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation		—	15	90	μA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off		—	5	80	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	5	—	μA
										LCD drive control circuit (5) When the internal voltage multiplier is used	—	11	—	μA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	μA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2	5.0	μA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off		—	13.0	—	μA
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 Topr = 25°C		—	0.02	0.2	μA
			Off	Off	Off	Off	—	—	Power-off 0 Topr = 85°C		—	0.3	—	μA
			Off	32 kHz	Off	Off	—	—	Power-off 1 Topr = 25°C		—	1.4	2.8	μA
			Off	32 kHz	Off	Off	—	—	Power-off 1 Topr = 85°C		—	1.8	—	μA

Notes:
1. Vcc = 2.7 V to 4.0 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 3.0 V
4. VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
5. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

5.5 AC Characteristics

Table 5.24 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (1)
		Slave		—	—	1	μs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (1)
		Slave		—	—	1	μs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_{H}	SSO, SSI data input hold time			1	—	—	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1	t_{CYC} (1)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

Table 5.26 External Clock Input (XIN, XCIN)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		V_{CC} = 2.2V, Topr = 25°C		V_{CC} = 3V, Topr = 25°C		V_{CC} = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	—	50	—	50	—	ns
$t_{WH(XIN)}$	XIN input “H” width	90	—	24	—	24	—	ns
$t_{WL(XIN)}$	XIN input “L” width	90	—	24	—	24	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	—	14	—	14	—	μs
$t_{WH(XCIN)}$	XCIN input “H” width	7	—	7	—	7	—	μs
$t_{WL(XCIN)}$	XCIN input “L” width	7	—	7	—	7	—	μs

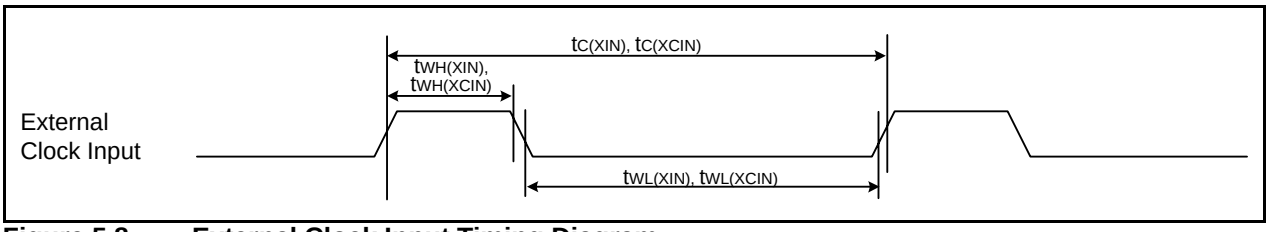


Figure 5.8 External Clock Input Timing Diagram

Table 5.27 Timing Requirements of TRAIO
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		V_{CC} = 2.2V, Topr = 25°C		V_{CC} = 3V, Topr = 25°C		V_{CC} = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	300	—	100	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	120	—	40	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	120	—	40	—	ns

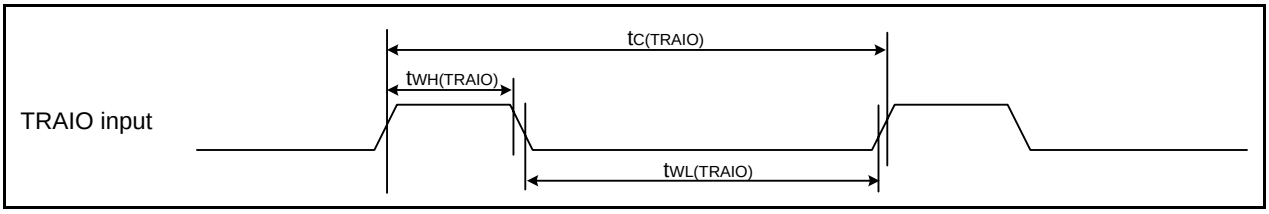


Figure 5.9 Input Timing of TRAIO

Table 5.28 Timing Requirements of Serial Interface
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		V_{CC} = 2.2V, Topr = 25°C		V_{CC} = 3V, Topr = 25°C		V_{CC} = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	300	—	200	—	ns
$t_{W(CKH)}$	CLKi input "H" width	400	—	150	—	100	—	ns
$t_{W(CKL)}$	CLKi input "L" width	400	—	150	—	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	—	80	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	0	—	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	70	—	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	90	—	90	—	ns

i = 0 to 2

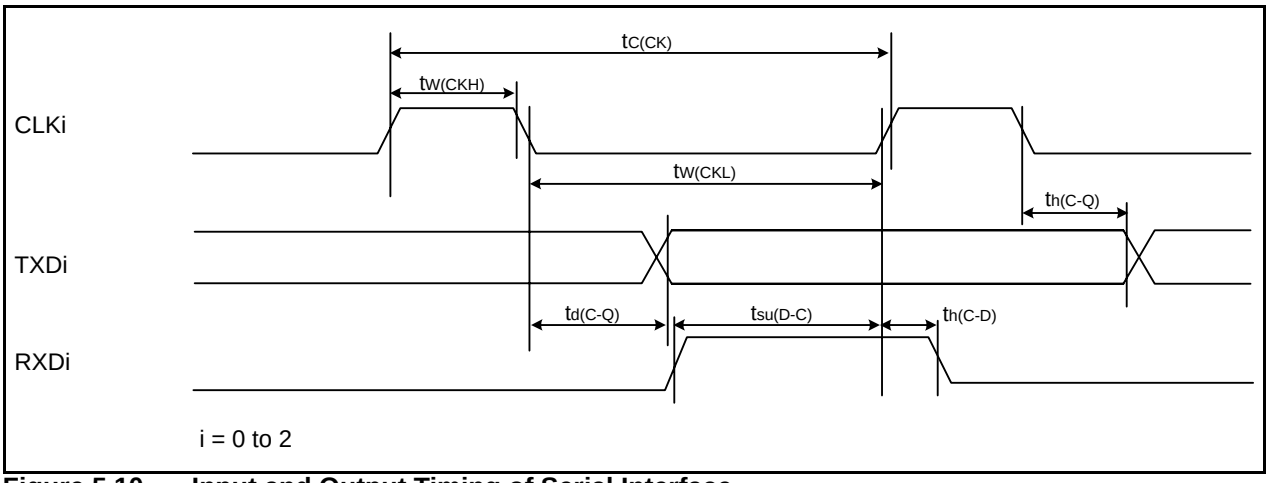


Figure 5.10 Input and Output Timing of Serial Interface

Table 5.29 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 7) and Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Standard						Unit
		V_{CC} = 2.2V, Topr = 25°C		V_{CC} = 3V, Topr = 25°C		V_{CC} = 5V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input "H" width, $\overline{KIi}$ input "H" width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input "L" width, $\overline{KIi}$ input "L" width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

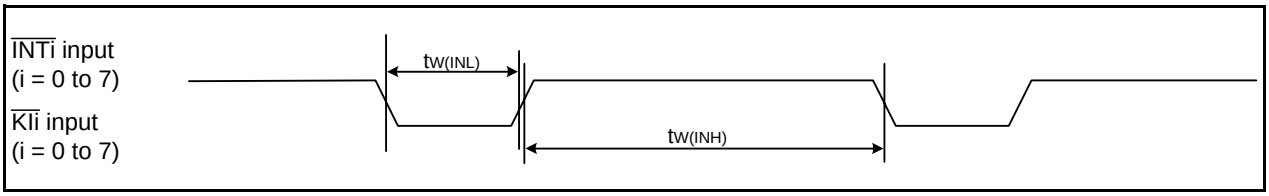
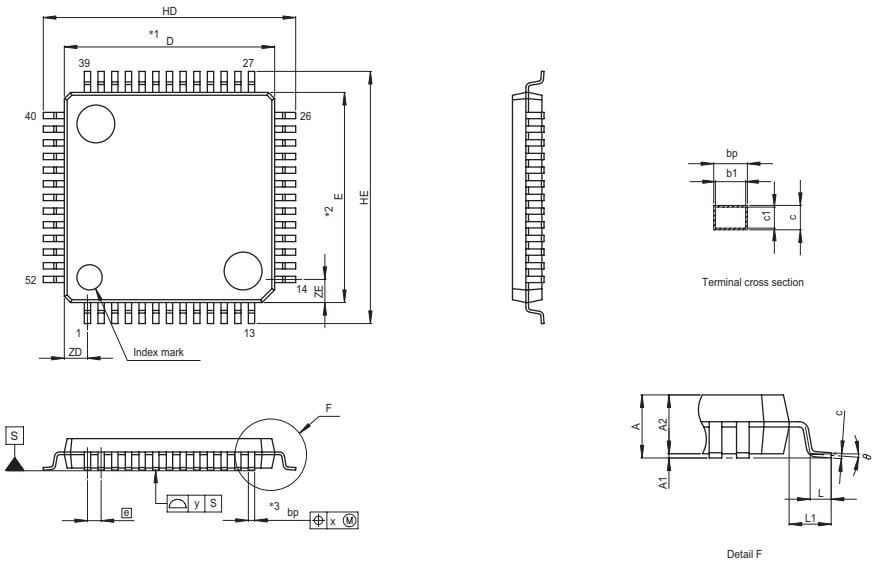


Figure 5.11 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

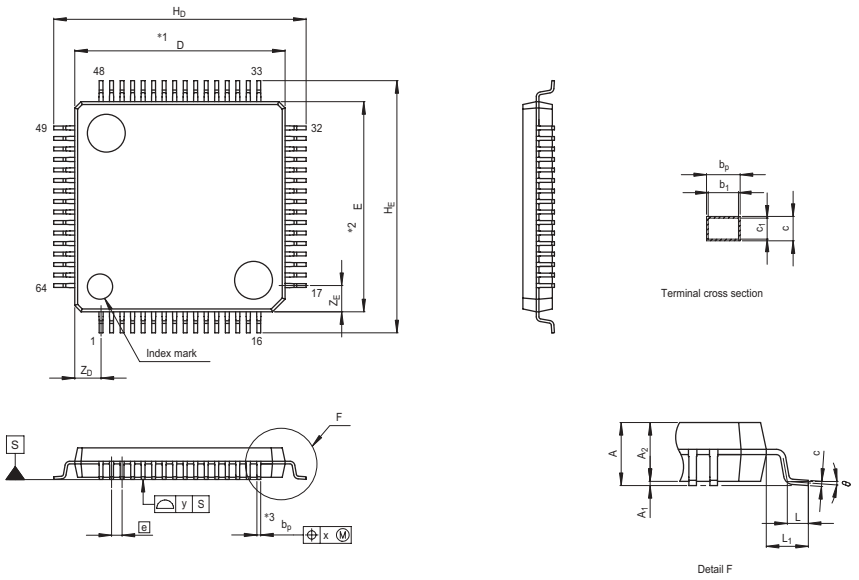
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

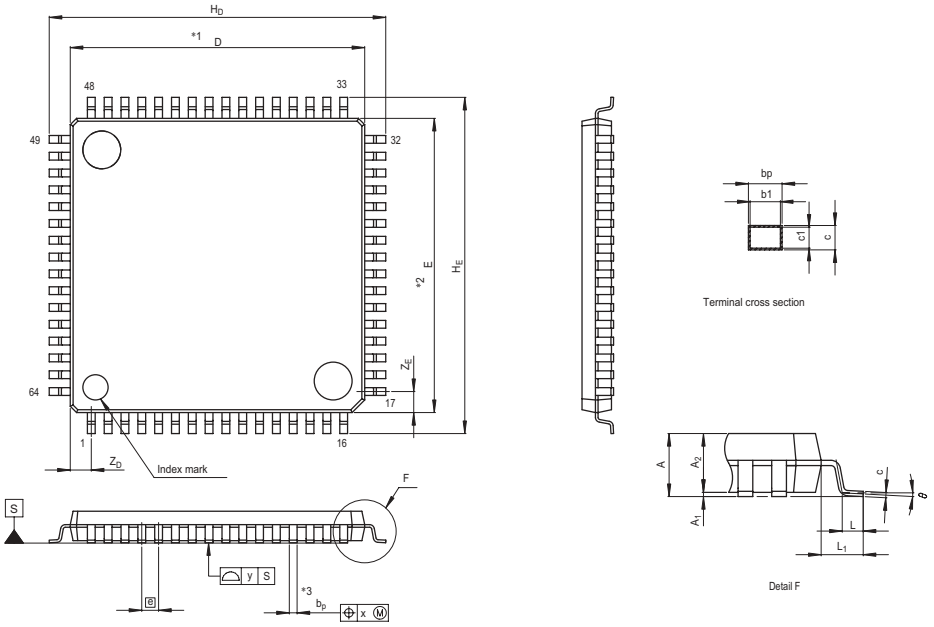
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—