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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	68
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l38cmnfa-v0

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Table 1.2 lists the Programmable I/O Ports Provided for Each Group, and Table 1.3 lists the LCD Display Function Pins Provided for Each Group. Figures 1.9 to 1.13 show the Pin Assignment for Each Group, and Tables 1.7 to 1.10 list Product Information.

The explanations in the chapters which follow apply to the R8C/L3AM Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/L35M Group	R8C/L36M Group	R8C/L38M Group	R8C/L3AM Group
I/O Ports	Programmable I/O ports	41 pins	52 pins	68 pins	88 pins
	High current drive ports	5 pins	8 pins	8 pins	16 pins
Interrupts	INT interrupt pins	5 pins	8 pins	8 pins	8 pins
	Key input interrupt pins	4 pins	4 pins	8 pins	8 pins
Timer RA	Timer RA output pin	None	1 pin	1 pin	1 pin
Timer RB	Timer RB output pin	None	1 pin	1 pin	1 pin
Timer RD	Timer RD I/O pin	None	None	8 pins	8 pins
Timer RE	Timer RE output pin	None	1 pin	1 pin	1 pin
Timer RG	Timer RG I/O pin	None	None	None	2 pins
	Timer RG output pin	None	None	None	2 pins
A/D Converter	Analog input pin	12 pins	12 pins	16 pins	20 pins
LCD Drive Control Circuit	LCD power supply	3 pins (VL1, VL2, VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)
	Common output pins	Max. 4 pins	Max. 8 pins	Max. 8 pins	Max. 8 pins
	Segment output pins	Max. 24 pins	Max. 32 pins	Max. 48 pins	Max. 56 pins
Packages		52-pin LQFP	64-pin LQFP	80-pin LQFP	100-pin LQFP/ 100-pin QFP

Note:

1. I/O ports are shared with I/O functions, such as interrupts or timers.
Refer to **Tables 1.11 to 1.13, Pin Name Information by Pin Number**, for details.

Table 1.6 Specifications (3)

Item	Specification
Flash Memory	<ul style="list-style-type: none"> • Programming and erasure voltage: $V_{CC} = 2.7$ to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • On-chip debug functions • On-board flash rewrite function • Background operation (BGO) function
Operating Frequency/ Supply Voltage	$f(XIN) = 20$ MHz ($V_{CC} = 2.7$ to 5.5 V) $f(XIN) = 5$ MHz ($V_{CC} = 1.8$ to 5.5 V)
Current Consumption	Typ. 7 mA ($V_{CC} = 5.0$ V, $f(XIN) = 20$ MHz) Typ. 3.6 mA ($V_{CC} = 3.0$ V, $f(XIN) = 10$ MHz) Typ. 3.5 μ A ($V_{CC} = 3.0$ V, wait mode ($f(XCIN) = 32$ kHz)) Typ. 2 μ A ($V_{CC} = 3.0$ V, stop mode) Typ. 1.4 μ A ($V_{CC} = 3.0$ V, power-off mode, timer RE enabled) Typ. 0.02 μ A ($V_{CC} = 3.0$ V, power-off mode, timer RE disabled)
Operating Ambient Temperature	-20 to 85°C (N version) -40 to 85°C (D version) ⁽¹⁾

Note:

1. Specify the D version if D version functions are to be used.

1.2 Product Lists

Tables 1.7 to 1.10 list Product List for Each Group. Figures 1.1 to 1.4 show the Correspondence of Part No., with Memory Size and Package for Each Group.

Table 1.7 Product List for R8C/L35M Group

Current of Jun 2011

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L357MNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0052JA-A	N Version
R5F2L358MNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0052JA-A	
R5F2L35AMNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	
R5F2L35CMNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	
R5F2L357MDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0052JA-A	D Version
R5F2L358MDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0052JA-A	
R5F2L35AMDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	
R5F2L35CMDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0052JA-A	

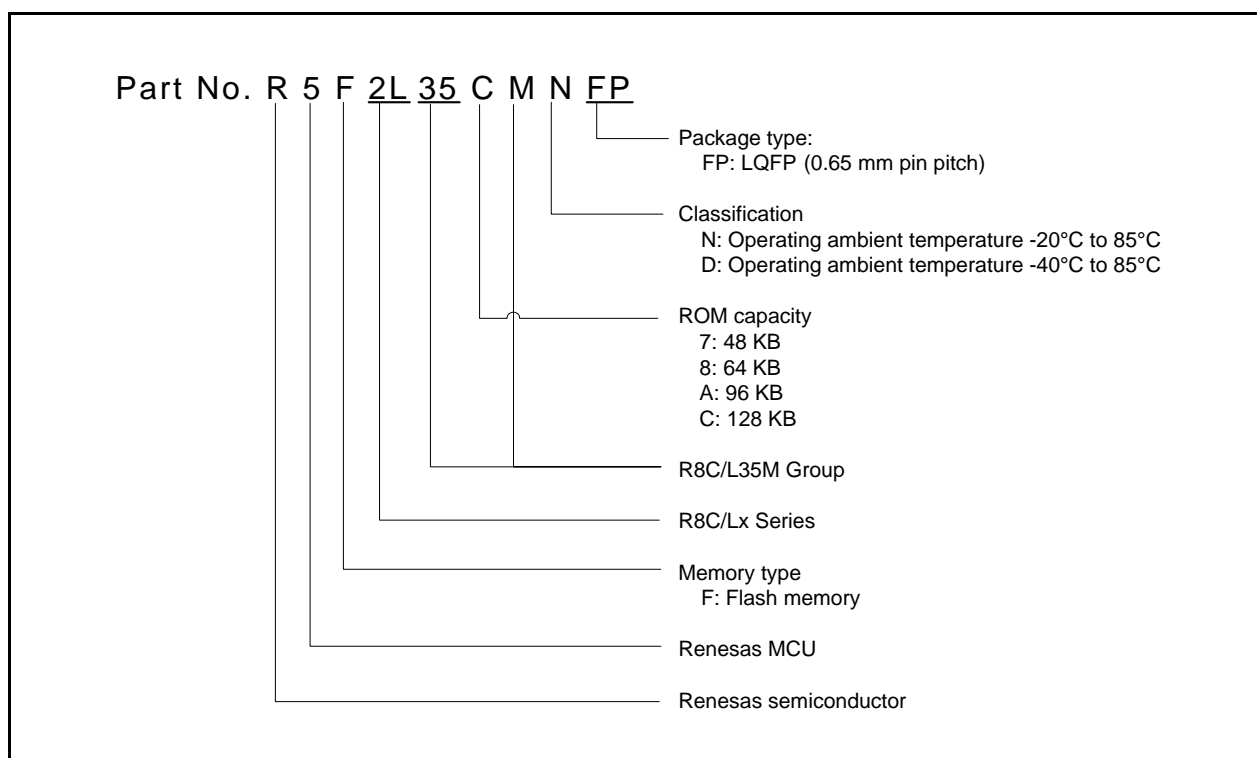
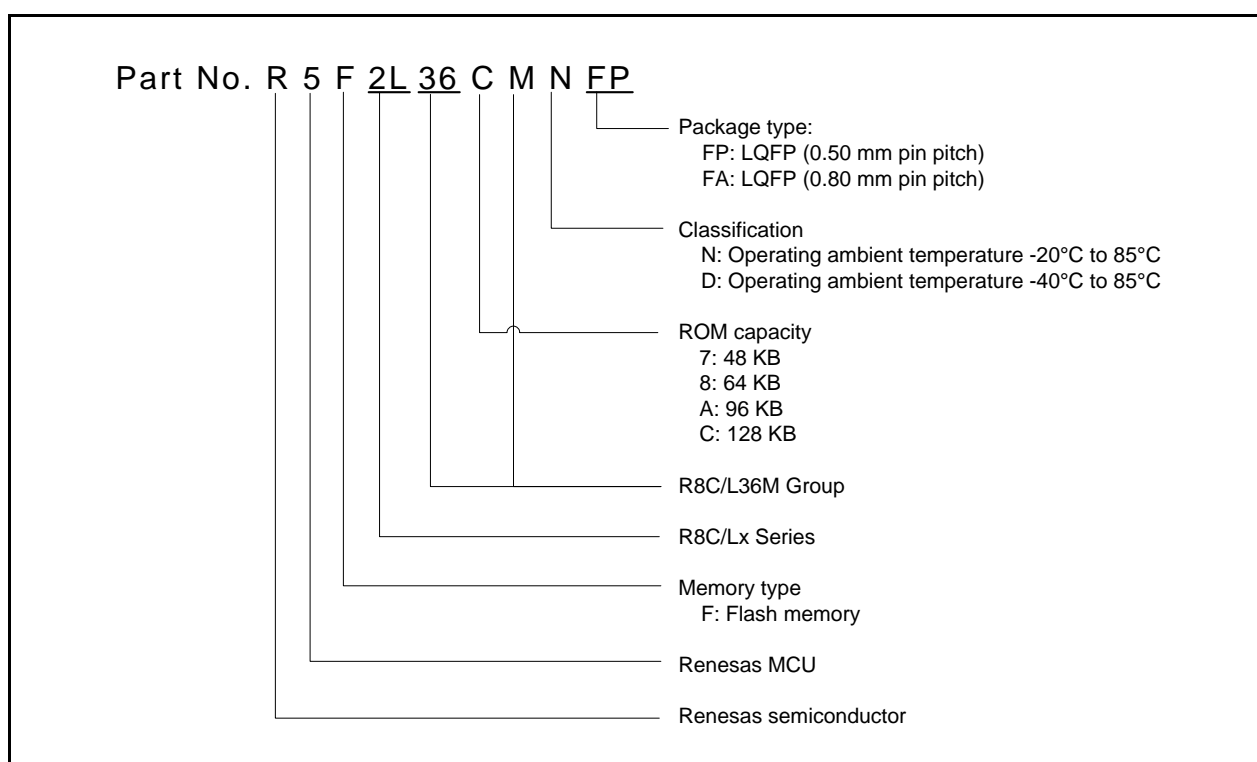


Figure 1.1 Correspondence of Part No., with Memory Size and Package of R8C/L35M Group

Table 1.8 Product List for R8C/L36M Group**Current of Jun 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L367MNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	N Version
R5F2L367MNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368MNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368MNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36AMNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36AMNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CMNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CMNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L367MDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	D Version
R5F2L367MDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368MDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368MDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36AMDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36AMDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CMDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CMDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	

**Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/L36M Group**

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/L35M Group. Figure 1.6 shows a Block Diagram of R8C/L36M Group. Figure 1.7 shows a Block Diagram of R8C/L38M Group. Figure 1.8 shows a Block Diagram of R8C/L3AM Group.

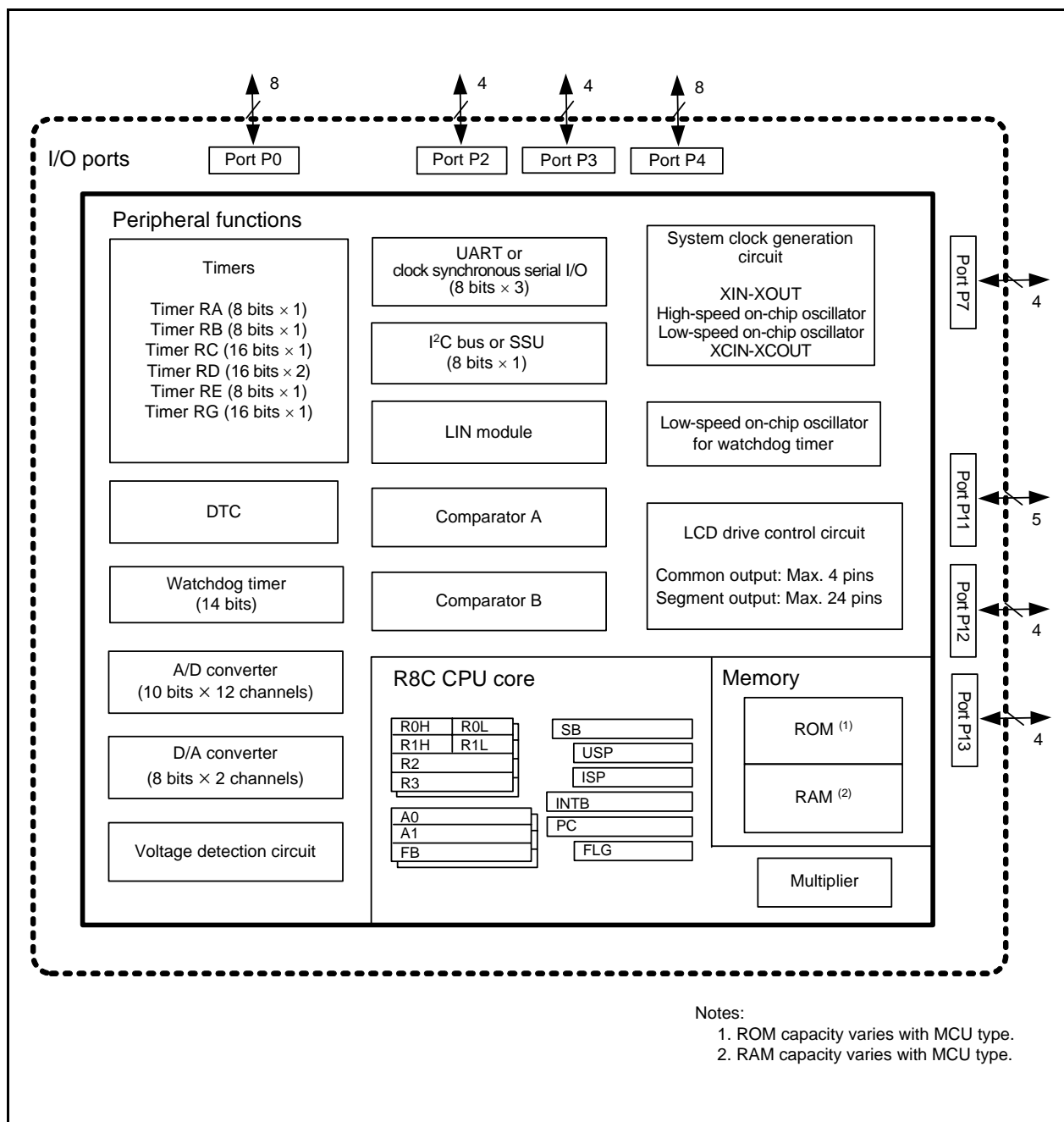
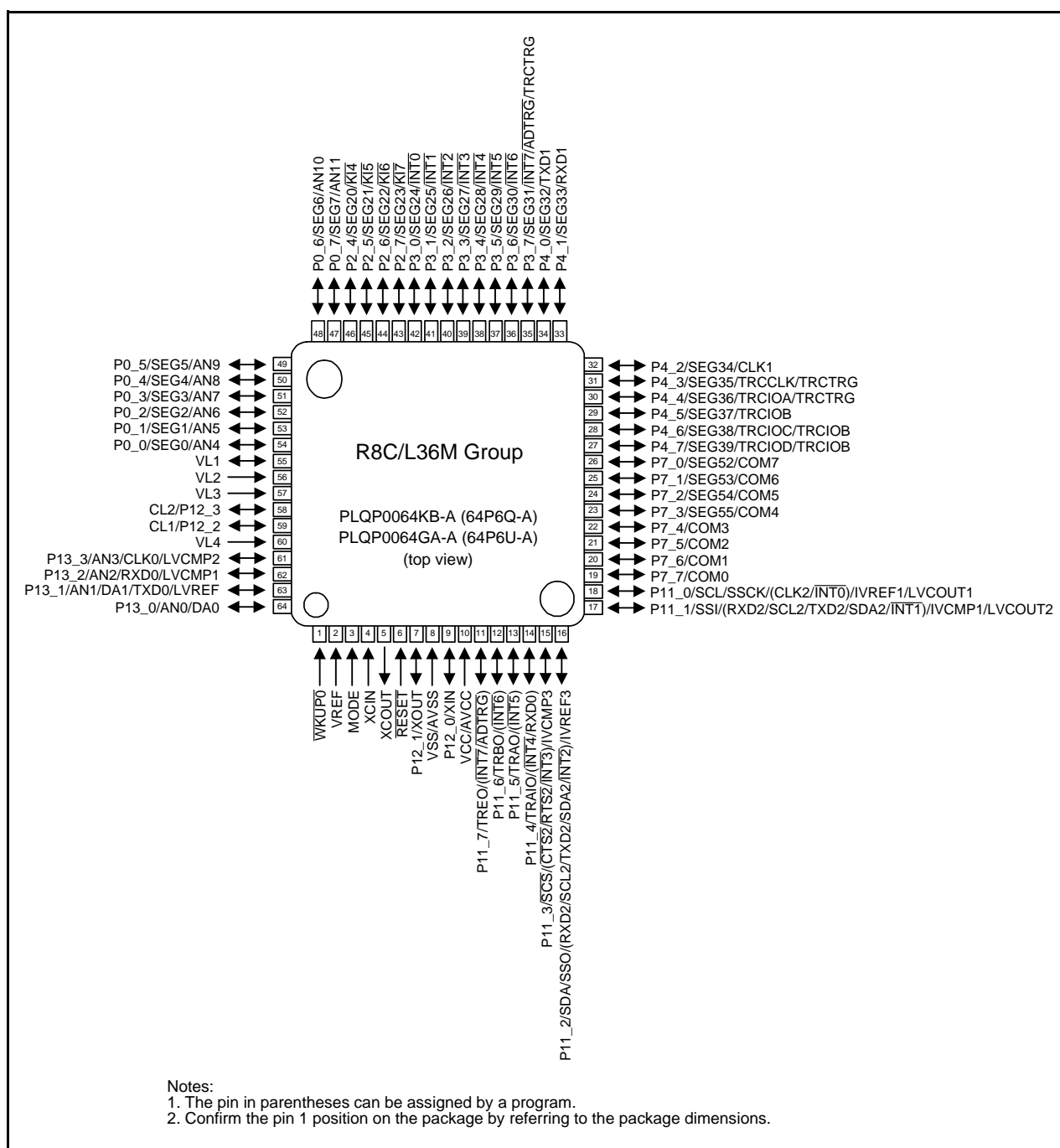


Figure 1.5 Block Diagram of R8C/L35M Group

**Figure 1.10 Pin Assignment (Top View) of PLQP0064KB-A and PLQP0064GA-A Packages**

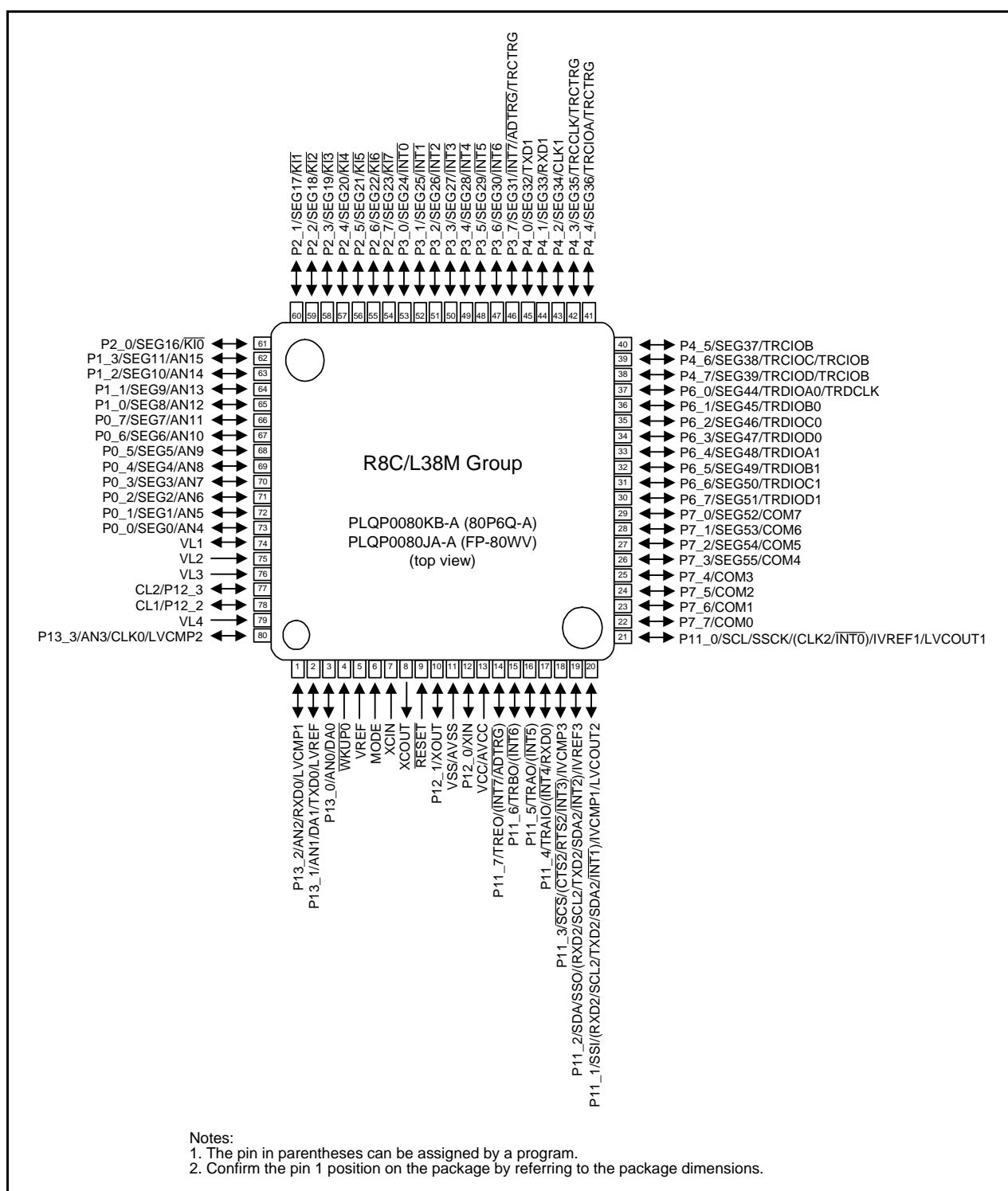


Figure 1.11 Pin Assignment (Top View) of PLQP0080KB-A and PLQP0080JA-A Packages

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register banks.

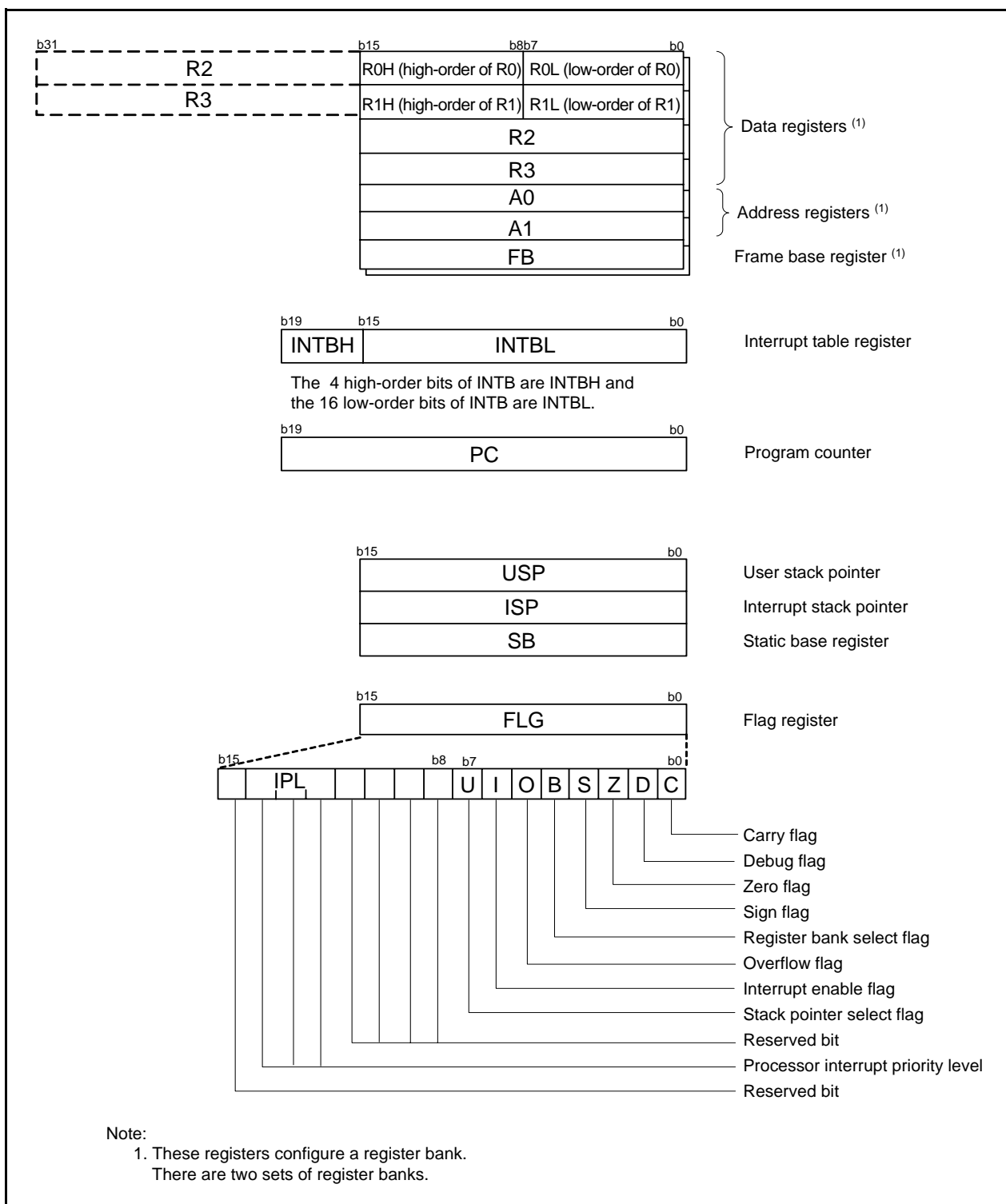


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Timer RE Counter Data Register	TRESEC	XXh
0119h	Timer RE Minute Data Register / Timer RE Compare Data Register	TREMIN	XXh
011Ah	Timer RE Hour Data Register	TREHR	XXh
011Bh	Timer RE Day of Week Data Register	TREWK	XXh
011Ch	Timer RE Control Register 1	TRECR1	XXXXXX0XXb
011Dh	Timer RE Control Register 2	TRECR2	XXh
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h	Timer RD Control Expansion Register	TRDECR	00h
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
0280h	LCD Display Control Data Register	LRA16H	XXh
0281h		LRA17H	XXh
0282h		LRA18H	XXh
0283h		LRA19H	XXh
0284h		LRA20H	XXh
0285h		LRA21H	XXh
0286h		LRA22H	XXh
0287h		LRA23H	XXh
0288h		LRA24H	XXh
0289h		LRA25H	XXh
028Ah		LRA26H	XXh
028Bh		LRA27H	XXh
028Ch		LRA28H	XXh
028Dh		LRA29H	XXh
028Eh		LRA30H	XXh
028Fh		LRA31H	XXh
0290h		LRA32H	XXh
0291h		LRA33H	XXh
0292h		LRA34H	XXh
0293h		LRA35H	XXh
0294h		LRA36H	XXh
0295h		LRA37H	XXh
0296h		LRA38H	XXh
0297h		LRA39H	XXh
0298h		LRA40H	XXh
0299h		LRA41H	XXh
029Ah		LRA42H	XXh
029Bh		LRA43H	XXh
029Ch		LRA44H	XXh
029Dh		LRA45H	XXh
029Eh		LRA46H	XXh
029Fh		LRA47H	XXh
02A0h		LRA48H	XXh
02A1h		LRA49H	XXh
02A2h		LRA50H	XXh
02A3h		LRA51H	XXh
02A4h		LRA52H	XXh
02A5h		LRA53H	XXh
02A6h		LRA54H	XXh
02A7h		LRA55H	XXh
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V _{cc} /AV _{cc}	Supply voltage			−0.3 to 6.5	V
V _i	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) ⁽¹⁾	−0.3 to 1.65	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) ⁽¹⁾	−0.3 to V _{cc} + 0.3	V
		VL1		−0.3 to VL2	V
		VL2	R8C/L35M	VL1 to VL4	V
			R8C/L36M, R8C/L38M, R8C/L3AM	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		VL3 to 6.5	V
		Other pins		−0.3 to V _{cc} + 0.3	V
V _o	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) ⁽¹⁾	−0.3 to 1.65	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) ⁽¹⁾	−0.3 to V _{cc} + 0.3	V
		VL1		−0.3 to VL2 ⁽²⁾	V
		VL2	R8C/L35M	VL1 to VL4	V
			R8C/L36M, R8C/L38M, R8C/L3AM	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		−0.3 to 6.5	V
		CL1, CL2		−0.3 to 6.5	V
		COM0 to COM7		−0.3 to VL4	V
		SEG0 to SEG55		−0.3 to VL4	V
		Other pins		−0.3 to V _{cc} + 0.3	V
P _d	Power dissipation		−40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature			−20 to 85 (N version) / −40 to 85 (D version)	°C
T _{stg}	Storage temperature			−65 to 150	°C

Notes:

- For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
- The VL1 voltage should be VCC or below.

Table 5.11 Voltage Detection 2 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det2}	Voltage detection level V _{det2_0} ⁽¹⁾	At the falling of V _{CC}	3.70	4.00	4.30	V
	Voltage detection level V _{det2_EXT} ⁽¹⁾	At the falling of LVCMP2	1.24	1.34	1.44	V
—	Hysteresis width at the rising of V _{CC} in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time ⁽²⁾	At the falling of V _{CC} from 5 V to (V _{det2_0} – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, V _{CC} = 5.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.12 Power-on Reset Circuit Characteristics ⁽¹⁾
(T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{rth}	External power V _{CC} rise gradient		0	—	50000	mV/msec

Note:

1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

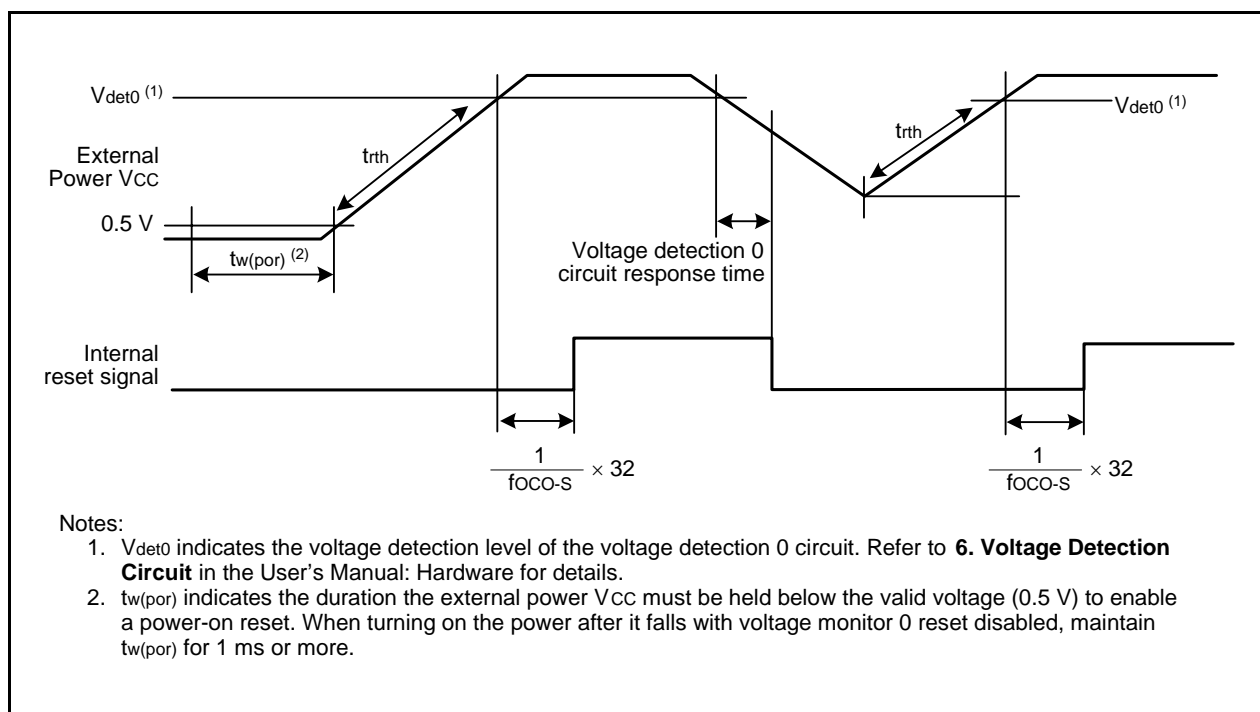


Figure 5.3 Power-on Reset Circuit Characteristics

Table 5.25 Timing Requirements of I²C bus Interface ⁽¹⁾
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12tcyc + 600 ⁽¹⁾	—	—	ns
t _{SCLH}	SCL input "H" width		3tcyc + 300 ⁽¹⁾	—	—	ns
t _{SCLL}	SCL input "L" width		5tcyc + 500 ⁽¹⁾	—	—	ns
t _{sf}	SCL, SDA input fall time		—	—	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		—	—	1tcyc ⁽¹⁾	ns
t _{BUF}	SDA input bus-free time		5tcyc ⁽¹⁾	—	—	ns
t _{STAH}	Start condition input hold time		3tcyc ⁽¹⁾	—	—	ns
t _{STAS}	Retransmit start condition input setup time		3tcyc ⁽¹⁾	—	—	ns
t _{STOP}	Stop condition input setup time		3tcyc ⁽¹⁾	—	—	ns
t _{SDAS}	Data input setup time		1tcyc + 40 ⁽¹⁾	—	—	ns
t _{SDAH}	Data input hold time		10	—	—	ns

Note:

1. 1tcyc = 1/f₁(s)

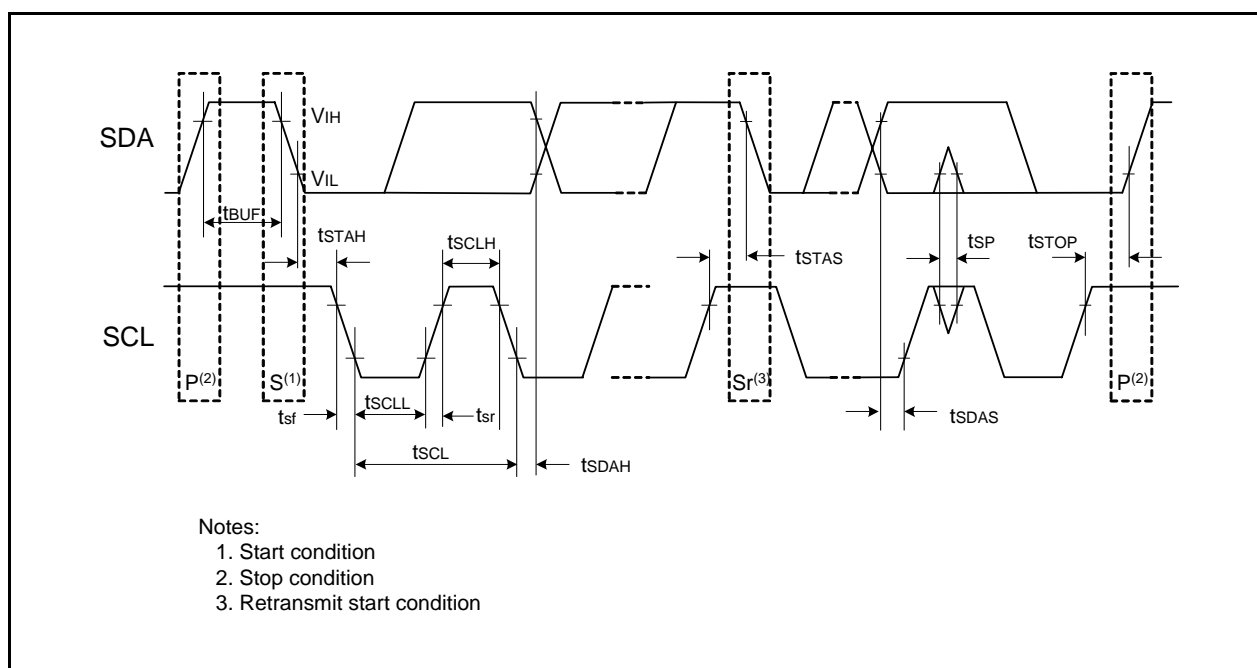
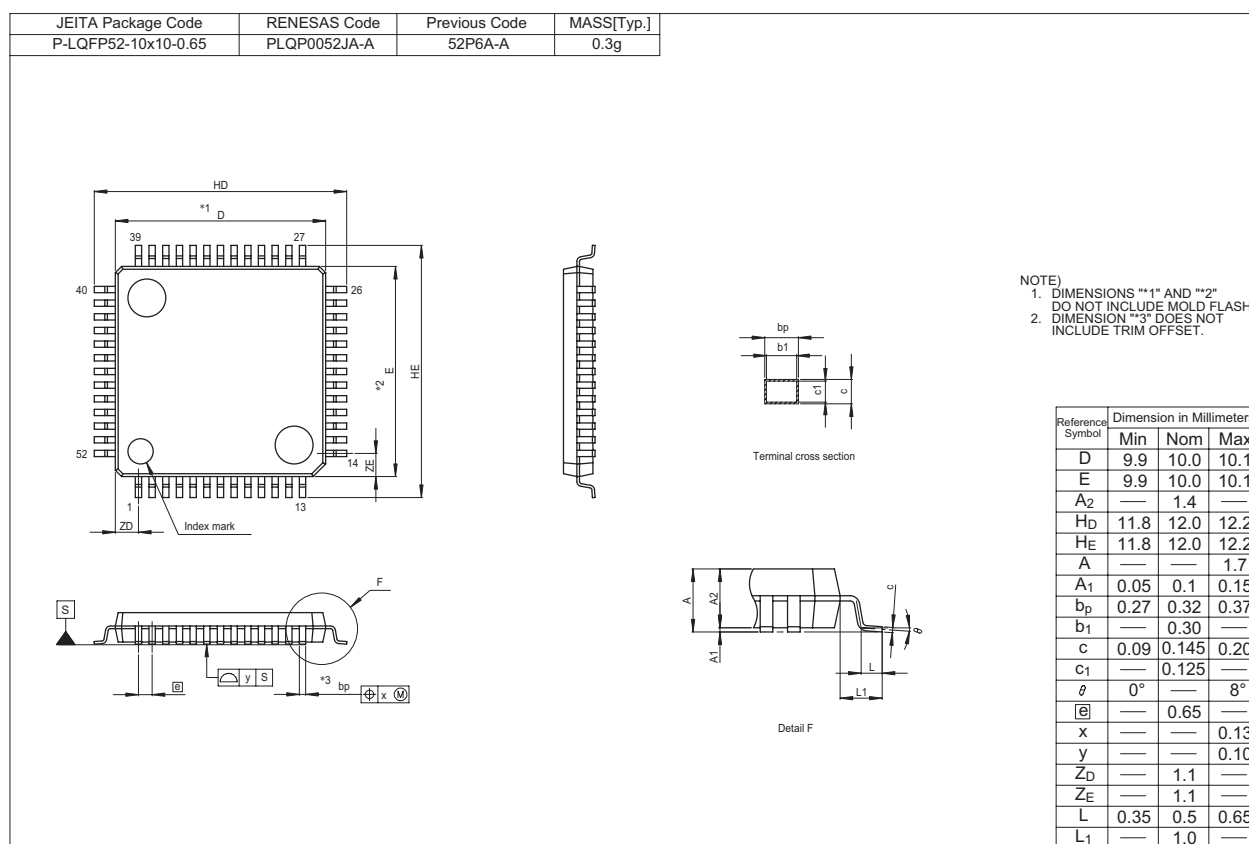
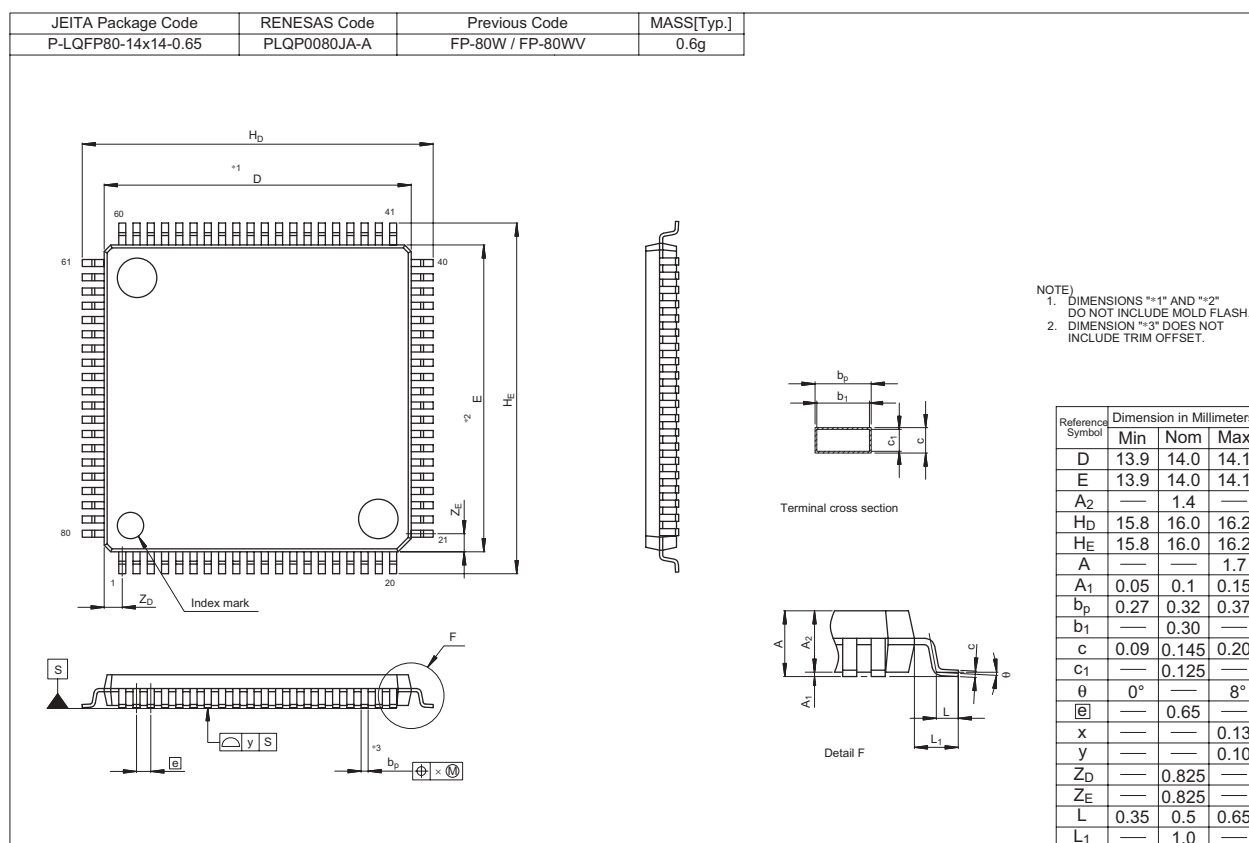
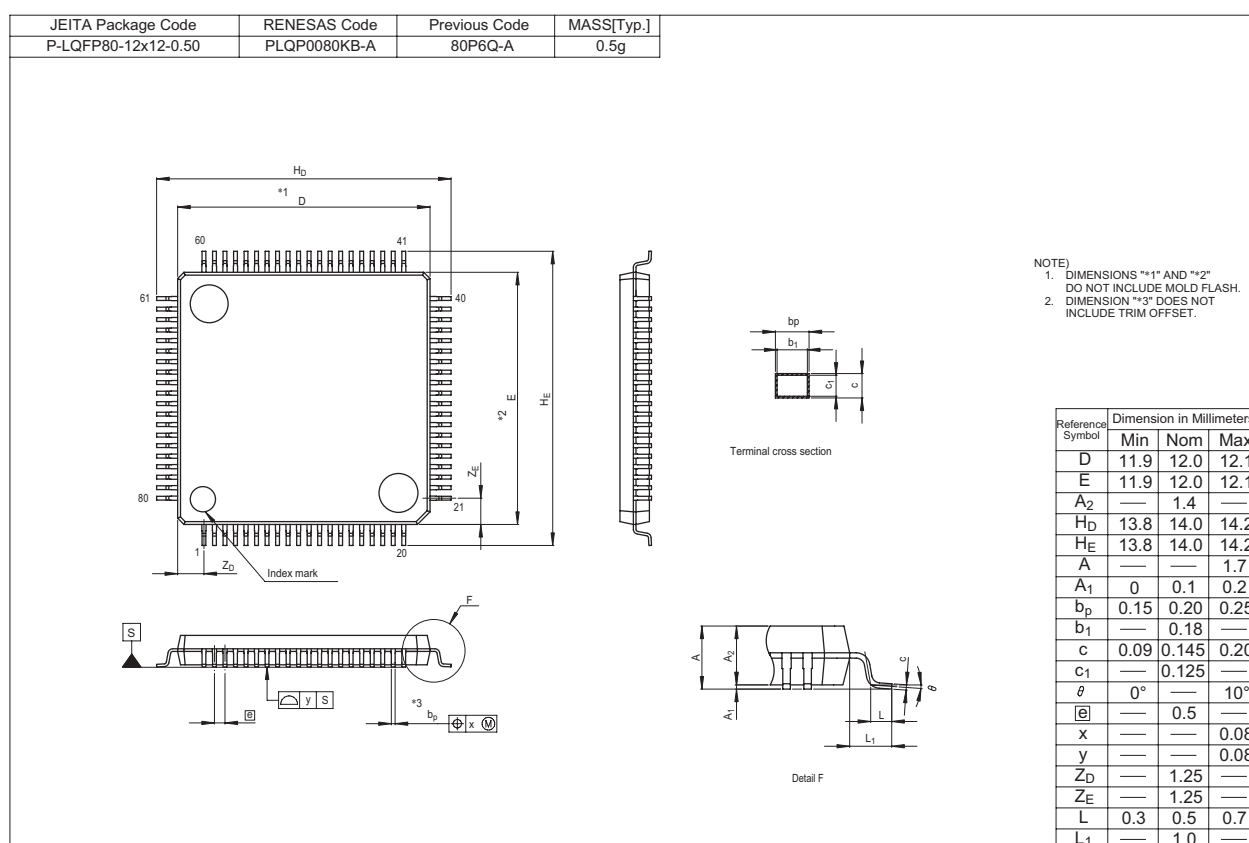


Figure 5.7 I/O Timing of I²C bus Interface

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.





REVISION HISTORY

R8C/L35M Group, R8C/L36M Group, R8C/L38M Group, R8C/L3AM Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Sep 30, 2010	—	First Edition issued
0.02	Nov 02, 2010	All 29 45 to 68	“Preliminary” is added Table 4.1 0030h “Voltage Monitor Circuit Control Register” → “Voltage Monitor Circuit/Comparator A Control Register” “5. Electrical Characteristics” added
0.03	Apr 15, 2011	2 3 6 28 38 to 40 53 54 57, 59, 61	Table 1.1 “Timers” deleted Table 1.2 Note 2, Table 1.3 Note 1 revised Table 1.6 “Current Consumption” revised 3. “The internal ROM ... with address 0FFFFh.” deleted Table 4.10 to Table 4.12 “0248h to 026Fh”, “02A8h to 02BFh”, “02C0h to 02CFh” revised Table 5.11 “V _{det2} ” revised Table 5.13 revised, Note 2 added Table 5.19, Table 5.21, Table 5.23 “High-Speed” → “High-Speed (fOCO-F)”, “Power-off mode” revised
1.00	Jun 28, 2011	10 50 54	Table 1.10, Figure 1.4 revised Table 5.7 revised Table 5.13 revised

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Laviel' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141