Renesas Electronics America Inc - R5F2L3A7MDFA#U0 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	88
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l3a7mdfa-u0

1.1.2 Differences between Groups

Table 1.1 lists the Differences between Groups, Table 1.2 lists the Programmable I/O Ports Provided for Each Group, and Table 1.3 lists the LCD Display Function Pins Provided for Each Group. Figures 1.9 to 1.13 show the Pin Assignment for Each Group, and Tables 1.7 to 1.10 list Product Information.
The explanations in the chapters which follow apply to the R8C/L3AM Group only. Note the differences shown below.

Table 1.1 Differences between Groups

Item	Function	R8C/L35M Group	R8C/L36M Group	R8C/L38M Group	R8C/L3AM Group
I/O Ports	Programmable I/O ports	41 pins	52 pins	68 pins	88 pins
	High current drive ports	5 pins	8 pins	8 pins	16 pins
Interrupts	$\overline{\text{INT}}$ interrupt pins	5 pins	8 pins	8 pins	8 pins
	Key input interrupt pins	4 pins	4 pins	8 pins	8 pins
Timer RA	Timer RA output pin	None	1 pin	1 pin	1 pin
Timer RB	Timer RB output pin	None	1 pin	1 pin	1 pin
Timer RD	Timer RD I/O pin	None	None	8 pins	8 pins
Timer RE	Timer RE output pin	None	1 pin	1 pin	1 pin
Timer RG	Timer RG I/O pin	None	None	None	2 pins
	Timer RG output pin	None	None	None	2 pins
A/D Converter	Analog input pin	12 pins	12 pins	16 pins	20 pins
LCD Drive Control Circuit	LCD power supply	3 pins (VL1, VL2, VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)	4 pins (VL1 to VL4)
	Common output pins	Max. 4 pins	Max. 8 pins	Max. 8 pins	Max. 8 pins
	Segment output pins	Max. 24 pins	Max. 32 pins	Max. 48 pins	Max. 56 pins
Packages		52-pin LQFP	64-pin LQFP	80-pin LQFP	100-pin LQFP/ 100-pin QFP

Note:
1. I/O ports are shared with I/O functions, such as interrupts or timers.
Refer to **Tables 1.11 to 1.13, Pin Name Information by Pin Number**, for details.

Table 1.5 Specifications (2)

Item	Function	Specification	
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode	
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode	
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 3 pins), PWM2 mode (PWM output: 1 pin)	
	Timer RD	16 bits × 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output: 6 pins), reset synchronous PWM mode (three-phase waveform output: 6 pins, sawtooth wave modulation), complementary PWM mode (three-phase waveform output: 6 pins, triangular wave modulation), PWM3 mode (PWM output with fixed period: 2 pins)	
	Timer RE	8 bits × 1 Real-time clock mode (counting of seconds, minutes, hours, days of week), output compare mode	
	Timer RG	16 bits × 1 Phase-counting mode, timer mode (output compare function, input capture function), PWM mode (output: 1 pin)	
Serial Interface	UART0, UART1	Clock synchronous serial I/O/UART × 2 channels	
	UART2	Clock synchronous serial I/O/UART, I^2C mode (I^2C-bus), multiprocessor communication function	
Synchronous Serial Communication Unit (SSU)		1 (shared with I^2C-bus)	
I^2C bus		1 (shared with SSU)	
LIN Module		Hardware LIN: 1 channel (timer RA, UART0 used)	
A/D Converter	R8C/L35M Group	10-bit resolution × 12 channels, including sample and hold function, with sweep mode	
	R8C/L36M Group	10-bit resolution × 12 channels, including sample and hold function, with sweep mode	
	R8C/L38M Group	10-bit resolution × 16 channels, including sample and hold function, with sweep mode	
	R8C/L3AM Group	10-bit resolution × 20 channels, including sample and hold function, with sweep mode	
D/A Converter		8-bit resolution × 2 circuits	
Comparator A		• 2 circuits (sheared with voltage monitor 1 and voltage monitor 2) • External reference voltage input available	
Comparator B		2 circuits	
LCD Drive Control Circuit	R8C/L35M Group	Common output: Max. 4 pins Segment output: Max. 24 pins	Bias: 1/2, 1/3 Duty: static, 1/2, 1/3, 1/4
	R8C/L36M Group	Common output: Max. 8 pins Segment output: Max. 32 pins (1)	Bias: 1/2, 1/3, 1/4 Duty: static, 1/2, 1/3, 1/4, 1/8
	R8C/L38M Group	Common output: Max. 8 pins Segment output: Max. 48 pins (1)	
	R8C/L3AM Group	Common output: Max. 8 pins Segment output: Max. 56 pins (1)	
		Voltage multiplier and dedicated regulator integrated	

Note:
1. This applies when four pins are selected for common output.

Table 1.10 Product List for R8C/L3AM Group **Current of Jun 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L3A7MNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7MNFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8MNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8MNFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AAMNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AAMNFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACMNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACMNFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3A7MDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7MDFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8MDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8MDFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AAMDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AAMDFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACMDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACMDFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	

(D): Under development

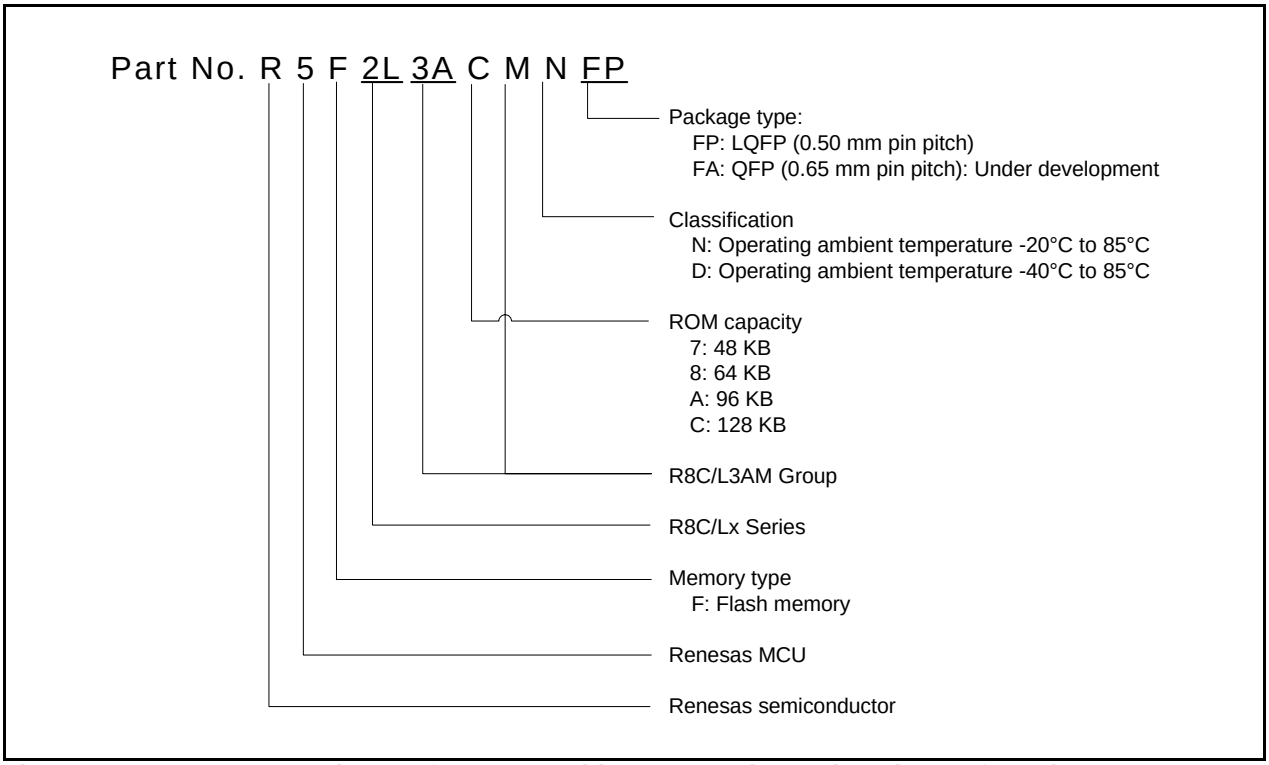
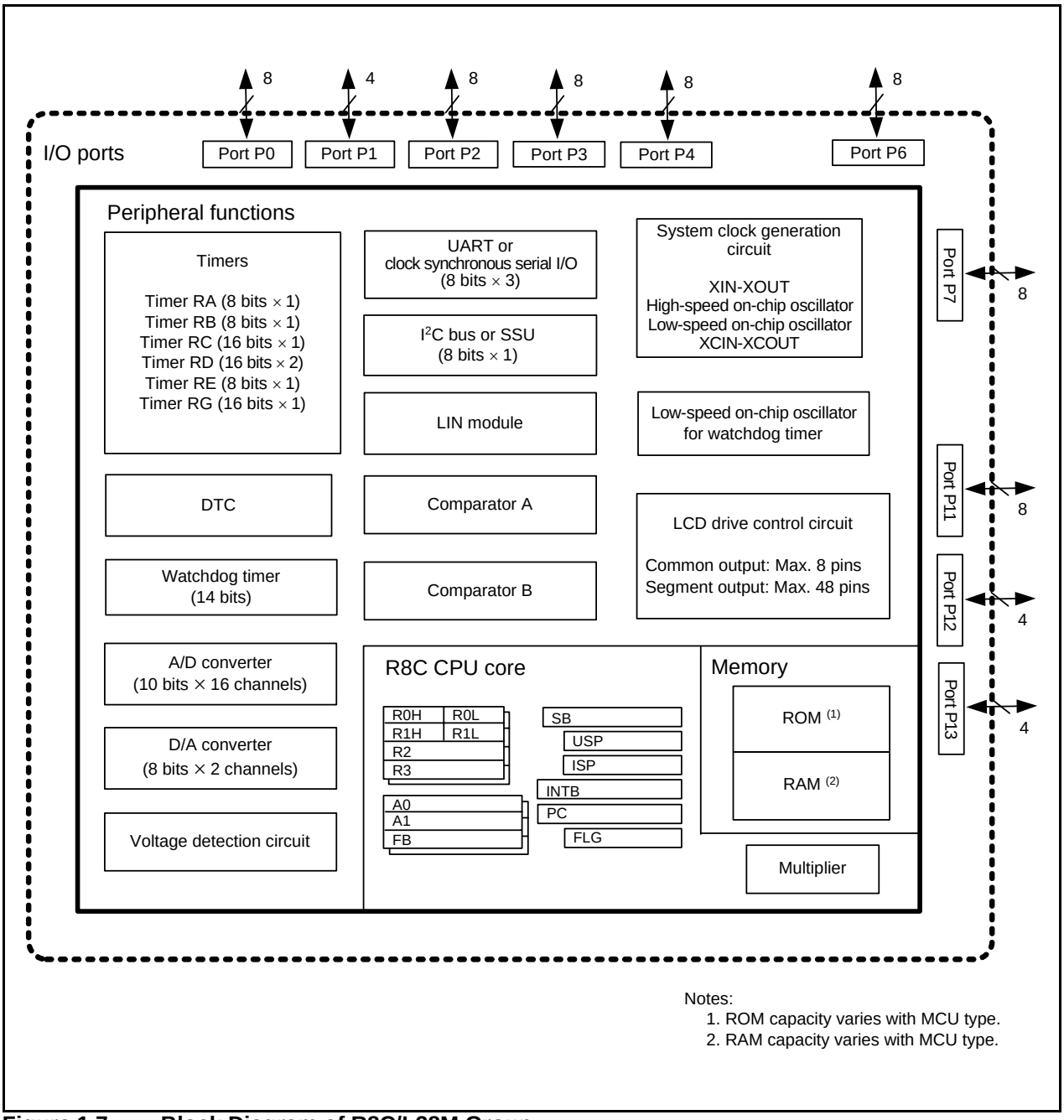


Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/L3AM Group

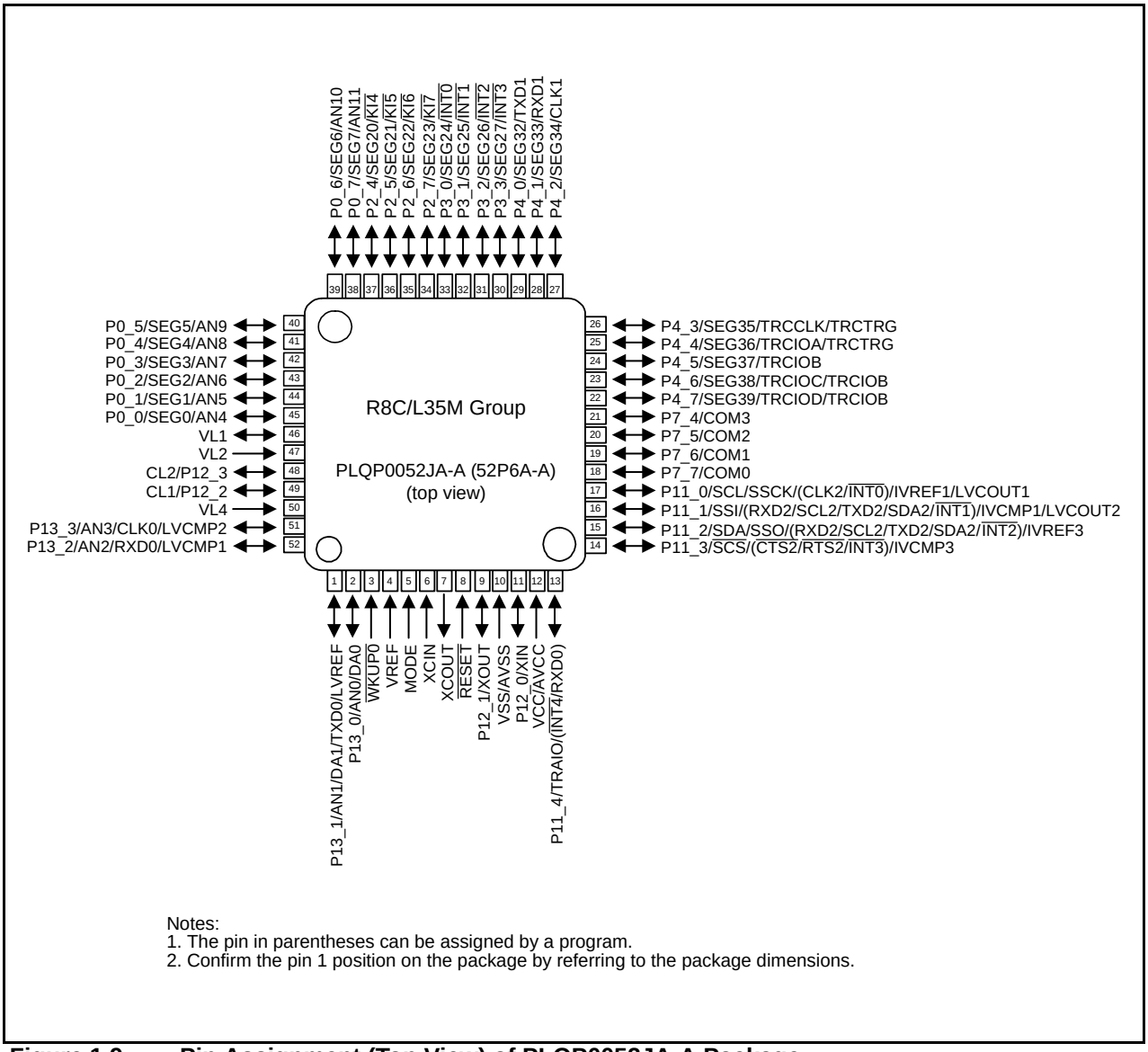


Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.7 Block Diagram of R8C/L38M Group

1.4 Pin Assignments

Figures 1.9 to 1.13 show Pin Assignments (Top View). Tables 1.11 to 1.13 list the Pin Name Information by Pin Number.



Notes:
1. The pin in parentheses can be assigned by a program.
2. Confirm the pin 1 position on the package by referring to the package dimensions.

Figure 1.9 Pin Assignment (Top View) of PLQP0052JA-A Package

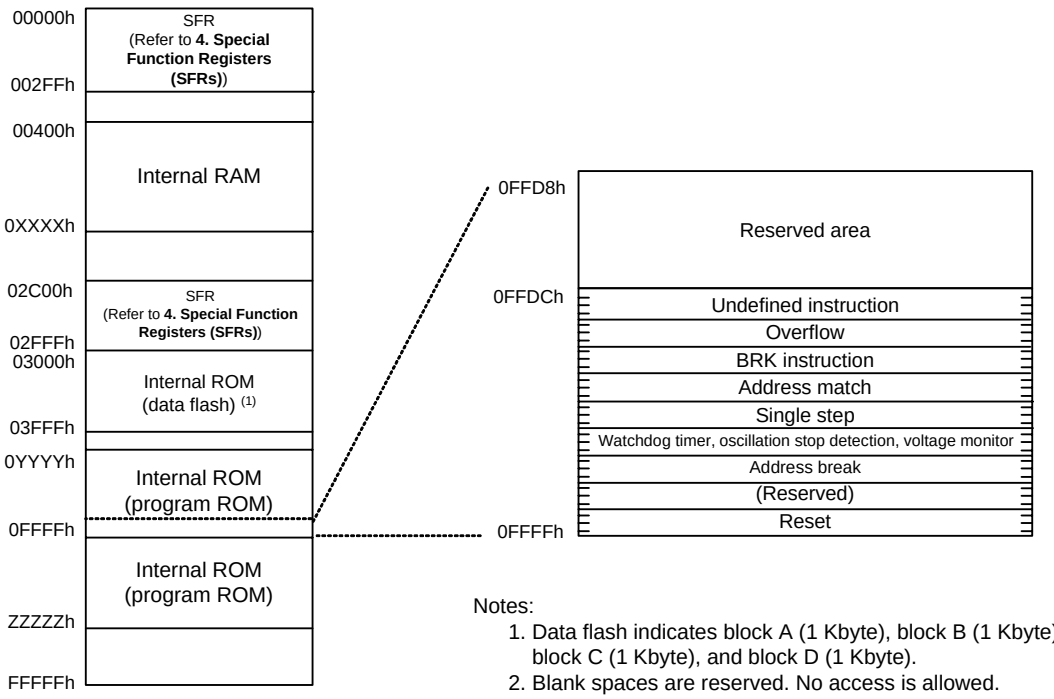
Table 1.12 Pin Name Information by Pin Number (2)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AM (Note 2)	L38M	L36M	L35M			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, D/A Converter, Comparator A, Comparator B, Voltage Detection Circuit	LCD drive control circuit
40 [42]	31				P6_6		TRDIOC1					SEG50
41 [43]	32				P6_5		TRDIOB1					SEG49
42 [44]	33				P6_4		TRDIOA1					SEG48
43 [45]	34				P6_3		TRDIOD0					SEG47
44 [46]	35				P6_2		TRDIOC0					SEG46
45 [47]	36				P6_1		TRDIOB0					SEG45
46 [48]	37				P6_0		TRDIOA0/ TRDCLK					SEG44
47 [49]					P5_3							SEG43
48 [50]					P5_2							SEG42
49 [51]					P5_1							SEG41
50 [52]					P5_0							SEG40
51 [53]	38	27	22		P4_7		TRCIOD/ TRCIOB					SEG39
52 [54]	39	28	23		P4_6		TRCIOC/ TRCIOB					SEG38
53 [55]	40	29	24		P4_5		TRCIOB					SEG37
54 [56]	41	30	25		P4_4		TRCIOA/ TRCTRG					SEG36
55 [57]	42	31	26		P4_3		TRCCLK/ TRCTRG					SEG35
56 [58]	43	32	27		P4_2			CLK1				SEG34
57 [59]	44	33	28		P4_1			RXD1				SEG33
58 [60]	45	34	29		P4_0			TXD1				SEG32
59 [61]	46	35			P3_7	$\overline{\text{INT7}}$	TRCTRG				$\overline{\text{ADTRG}}$	SEG31
60 [62]	47	36			P3_6	$\overline{\text{INT6}}$						SEG30
61 [63]	48	37			P3_5	$\overline{\text{INT5}}$						SEG29
62 [64]	49	38			P3_4	$\overline{\text{INT4}}$						SEG28
63 [65]	50	39	30		P3_3	$\overline{\text{INT3}}$						SEG27
64 [66]	51	40	31		P3_2	$\overline{\text{INT2}}$						SEG26
65 [67]	52	41	32		P3_1	$\overline{\text{INT1}}$						SEG25
66 [68]	53	42	33		P3_0	$\overline{\text{INT0}}$						SEG24
67 [69]	54	43	34		P2_7	$\overline{\text{KI7}}$						SEG23
68 [70]	55	44	35		P2_6	$\overline{\text{KI6}}$						SEG22
69 [71]	56	45	36		P2_5	$\overline{\text{KI5}}$						SEG21
70 [72]	57	46	37		P2_4	$\overline{\text{KI4}}$						SEG20
71 [73]	58				P2_3	$\overline{\text{KI3}}$						SEG19
72 [74]	59				P2_2	$\overline{\text{KI2}}$						SEG18
73 [75]	60				P2_1	$\overline{\text{KI1}}$						SEG17
74 [76]	61				P2_0	$\overline{\text{KI0}}$						SEG16
75 [77]					P1_7							SEG15
76 [78]					P1_6							SEG14
77 [79]					P1_5							SEG13
78 [80]					P1_4							SEG12
79 [81]	62				P1_3						AN15	SEG11
80 [82]	63				P1_2						AN14	SEG10
81 [83]	64				P1_1						AN13	SEG9
82 [84]	65				P1_0						AN12	SEG8
83 [85]	66	47	38		P0_7						AN11	SEG7
84 [86]	67	48	39		P0_6						AN10	SEG6

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

3. Memory

Figure 3.1 is a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F2L357M***, R5F2L367M***, R5F2L387M***, R5F2L3A7M***	48 Kbytes	04000h	–	6 Kbytes	01BFFh
R5F2L358M***, R5F2L368M***, R5F2L388M***, R5F2L3A8M***	64 Kbytes	04000h	13FFFh	8 Kbytes	023FFh
R5F2L35AM***, R5F2L36AM***, R5F2L38AM***, R5F2L3AAM***	96 Kbytes	04000h	1BFFFh	10 Kbytes	02BFFh
R5F2L35CM***, R5F2L36CM***, R5F2L38CM***, R5F2L3ACM***	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

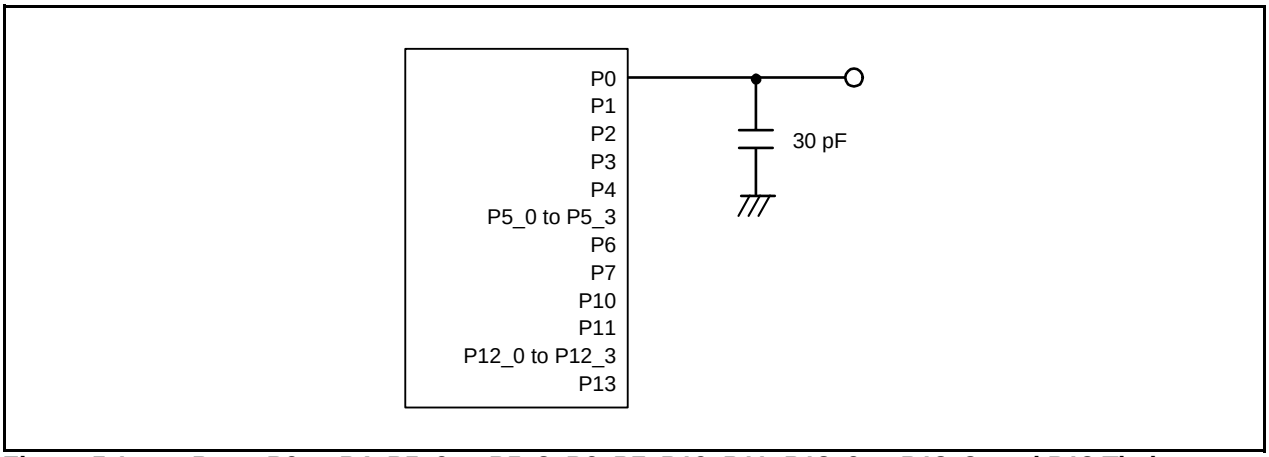


Figure 5.1 Ports P0 to P4, P5_0 to P5_3, P6, P7, P10, P11, P12_0 to P12_3, and P13 Timing Measurement Circuit

Table 5.9 Voltage Detection 0 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (1)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (3)	At the falling of Vcc from 5 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	µs

Notes:
1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.10 Voltage Detection 1 Circuit Characteristics (Vcc = 1.8 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (1)	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (1)	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (1)	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (1)	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (1)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (1)	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (1)	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (1)	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (1)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (1)	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (1)	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (1)	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (1)	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (1)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (1)	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (1)	At the falling of Vcc	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_6 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.13 High-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min. (2)	Typ.	Max. (2)	
—	High-speed on-chip oscillator frequency after reset	VCC = 1.8 V to 5.5 V –20°C ≤ Topr ≤ 85°C	39.4	40	40.6	MHz
		VCC = 1.8 V to 5.5 V –40°C ≤ Topr ≤ 85°C	39.4	40	40.6	MHz
		VCC = 1.8 V to 5.5 V Topr = 25°C	39.6	40	40.4	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (1)	VCC = 1.8 V to 5.5 V –20°C ≤ Topr ≤ 85°C	36.311	36.864	37.417	MHz
		VCC = 1.8 V to 5.5 V –40°C ≤ Topr ≤ 85°C	36.311	36.864	37.417	MHz
		VCC = 1.8 V to 5.5 V Topr = 25°C	36.495	36.864	37.233	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	VCC = 1.8 V to 5.5 V –20°C ≤ Topr ≤ 85°C	31.52	32	32.48	MHz
		VCC = 1.8 V to 5.5 V –40°C ≤ Topr ≤ 85°C	31.52	32	32.48	MHz
		VCC = 1.8 V to 5.5 V Topr = 25°C	31.68	32	32.32	MHz
—	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	—	100	450	µs
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	—	500	—	µA

Notes:
1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.
2. The minimum and maximum values are TBD for the R8C/L3AM Group (0.65-mm pin pitch) only.

Table 5.14 Low-speed On-Chip Oscillator Circuit Characteristics (VCC = 1.8 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		112.5	125	137.5	kHz
—	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	—	30	100	µs
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	—	3	—	µA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
—	Oscillation stability time	VCC = 5.0 V, Topr = 25°C	—	30	100	µs
—	Self power consumption at oscillation	VCC = 5.0 V, Topr = 25°C	—	2	—	µA

Table 5.15 Power Supply Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = 25°C, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during power-on (1)		—	—	2000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.16 LCD Drive Control Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL4	2.2	—	5.5	V
VL3	VL3 voltage		VL2	—	VL4	V
VL2	VL2 voltage	R8C/L35M	VL1	—	VL4	V
		R8C/L36M, R8C/L38M, R8C/L3AM	VL1	—	VL3	V
VL1	VL1 voltage		1	—	VL2 (3)	V
—	VL1 internally-generated voltage accuracy (1)		Setting voltage –0.2	Setting voltage	Setting voltage +0.2	V
f(FR)	Frame frequency		50	—	180	Hz
ILCD	LCD drive control circuit current		—	(Note 2)	—	µA

Notes:
1. The voltage is selected with bits LVLS0 to LVLS3 in the LCR1 register.
2. Refer to **Table 5.19 DC Characteristics (2)**, **Table 5.21 DC Characteristics (4)**, and **Table 5.23 DC Characteristics (6)**.
3. The VL1 voltage should be VCC or below.

Table 5.17 Power-Off Mode Characteristics (VCC = 2.2 to 5.5 V, VSS = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Power-off mode operating supply voltage		2.2	—	5.5	V

5.4 DC Characteristics

Table 5.18 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Port P10, P11 (1)	V_{CC} = 5V	I_{OH} = –20 mA	V_{CC} – 2.0	—	V_{CC}	V
		Other pins	V_{CC} = 5V	I_{OH} = –5 mA	V_{CC} – 2.0	—	V_{CC}	V
		XOUT	V_{CC} = 5V	I_{OH} = –200 μA	1.0	—	—	V
V_{OL}	Output “L” voltage	Port P10, P11 (1)	V_{CC} = 5V	I_{OL} = 20 mA	—	—	2.0	V
		Other pins	V_{CC} = 5V	I_{OL} = 5 mA	—	—	2.0	V
		XOUT	V_{CC} = 5V	I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{INT5}$, $\overline{INT6}$, $\overline{INT7}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, KI4, KI5, KI6, KI7, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRGCLKA, TRGCLKB, TRGIOA, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.05	0.5	—	V
		$\overline{RESET}$, $\overline{WKUP0}$			0.1	1.0	—	V
I_{IH}	Input “H” current		VI = 5.0 V, V_{CC} = 5.0 V		—	—	5.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5.0 V		—	—	–5.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	14	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.

Table 5.19 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	7.0	15	mA
			16 MHz	Off	Off	125 kHz	No division	—		—	5.6	12.5	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	3.6	—	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—		—	3.0	—	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	—		—	2.2	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		—	90	400	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		—	100	400	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	—	55	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	100	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	90	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	7	—	µA
										LCD drive control circuit (5) When the internal voltage multiplier is used	—	12	—	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2.0	5.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off		—	15	—	µA
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 Topr = 25°C		—	0.02	0.2	µA
			Off	Off	Off	Off	—	—	Power-off 0 Topr = 85°C		—	0.4	—	µA
			Off	32 kHz	Off	Off	—	—	Power-off 1 Topr = 25°C		—	1.6	3.2	µA
			Off	32 kHz	Off	Off	—	—	Power-off 1 Topr = 85°C		—	2.0	—	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V
4. VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
5. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

Table 5.22 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Port P10, P11 (1)	I_{OH} = –2 mA	V_{CC} – 0.5	—	V_{CC}	V
		Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	—	—	V
V_{OL}	Output “L” voltage	Port P10, P11 (1)	I_{OL} = 2 mA	—	—	0.5	V
		Other pins	I_{OL} = 1 mA	—	—	0.5	V
		XOUT	I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, INT7, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRGCLKA, TRGCLKB, $\overline{TRGIOA}$, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, $\overline{SSO}$		0.05	0.4	—	V
		$\overline{RESET}$, $\overline{WKUP0}$		0.1	0.8	—	V
I_{IH}	Input “H” current		VI = 1.8 V, V_{CC} = 1.8 V	—	—	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 1.8 V	—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 1.8 V	60	160	420	kΩ
R_{fXIN}	Feedback resistance	XIN		—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN		—	14	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.

5.5 AC Characteristics

Table 5.24 Timing Requirements of Synchronous Serial Communication Unit (SSU) (V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = −20 to 85°C (N version) / −40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (1)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (1)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (1)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1	t_{CYC} (1)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns

Note:
1. 1t_{CYC} = 1/f1(s)

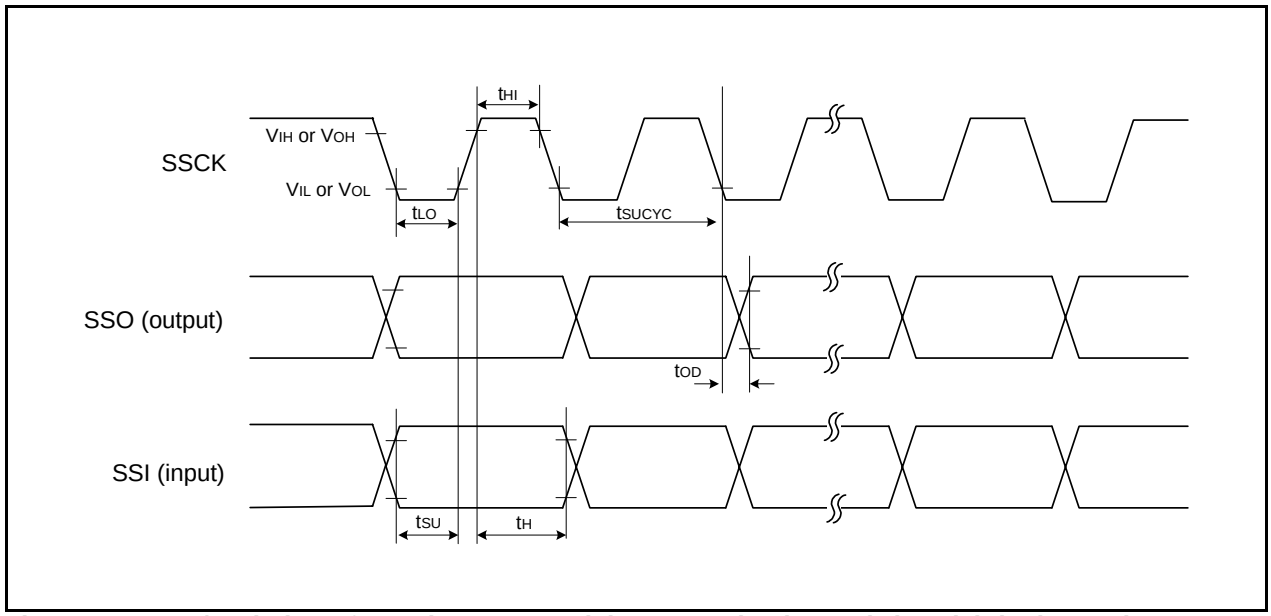
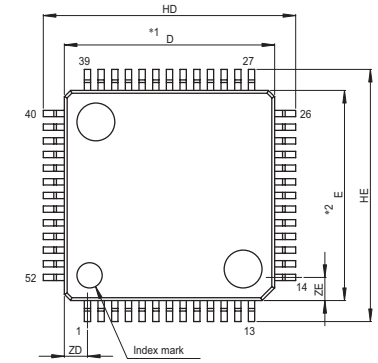


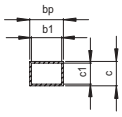
Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Package Dimensions

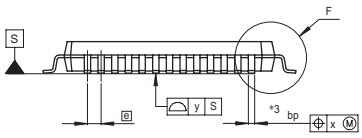
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics web site.

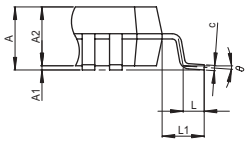
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP52-10x10-0.65	PLQP0052JA-A	52P6A-A	0.3g





Terminal cross section



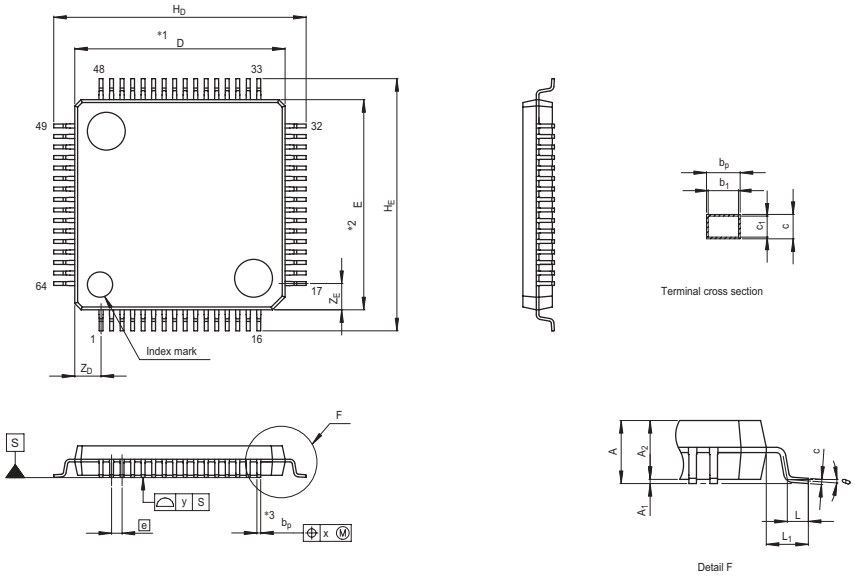


Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	1.1	—
Z_E	—	1.1	—
L	0.35	0.5	0.65
L_1	—	1.0	—

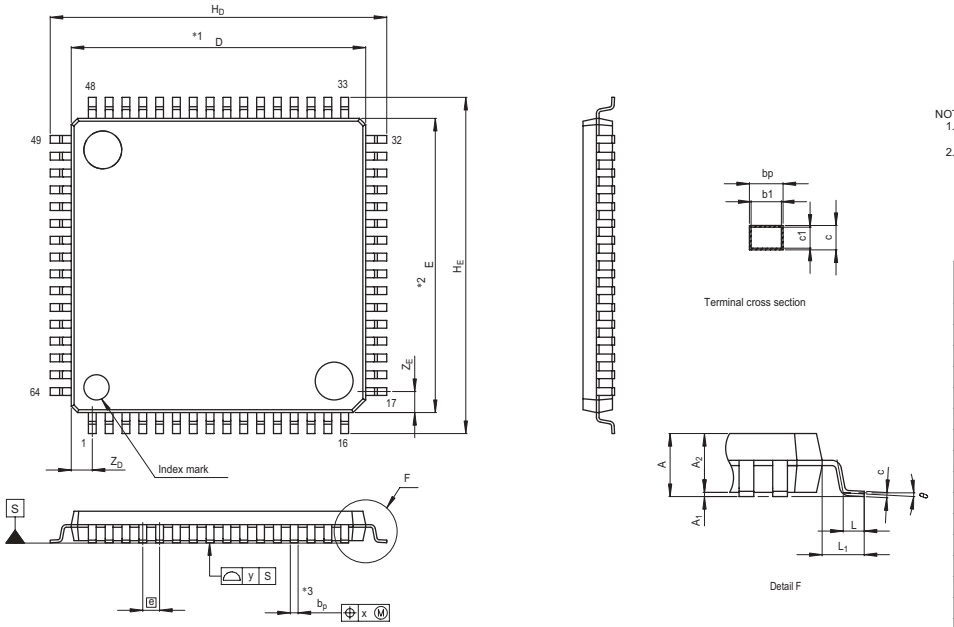
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

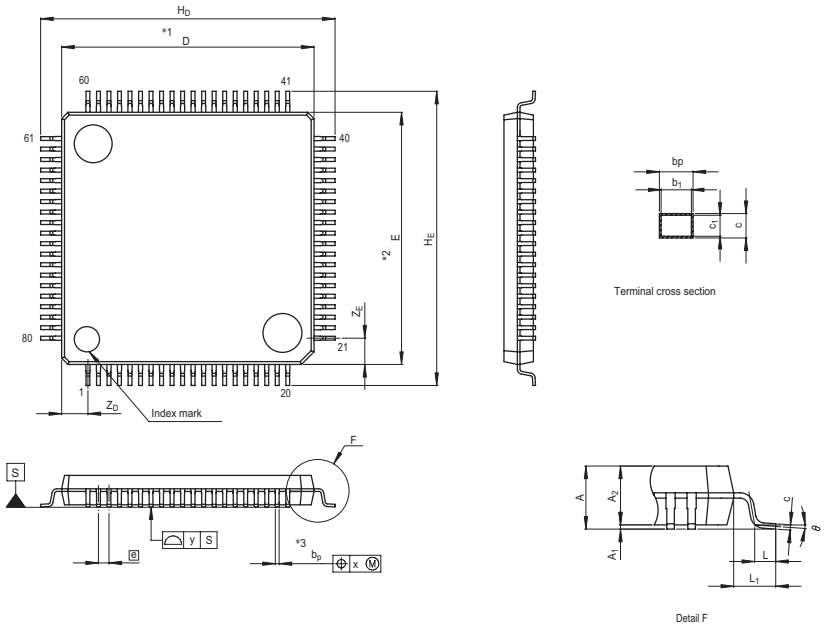
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-14x14-0.80	PLQP0064GA-A	64P6U-A/ —	0.7g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.3	0.5	0.7
L_1	—	1.0	—

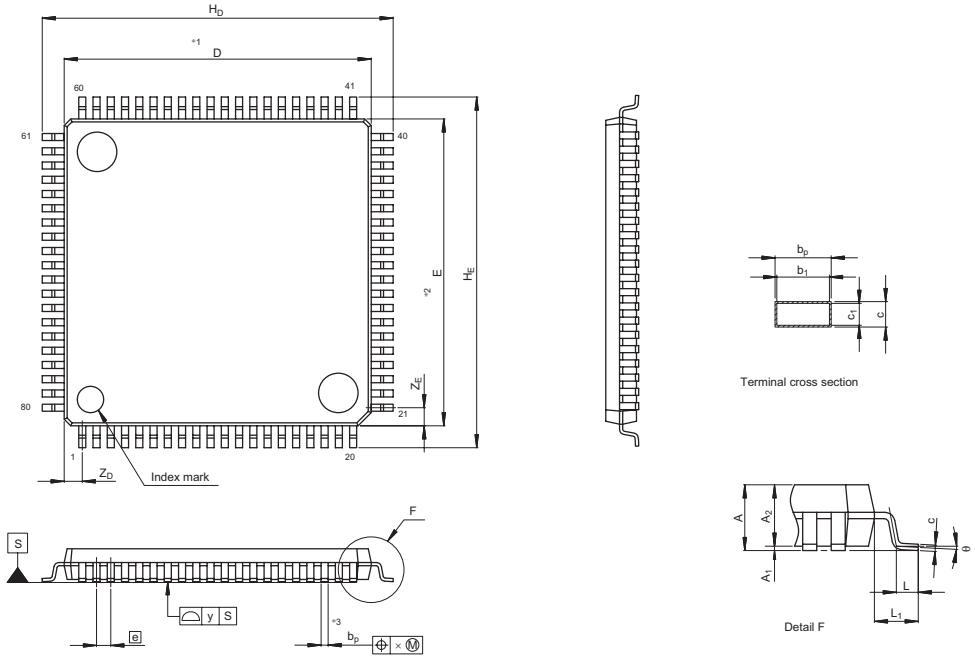
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—