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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	88
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l3a7mnfa-u0

Table 1.8 Product List for R8C/L36M Group**Current of Jun 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L367MNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	N Version
R5F2L367MNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368MNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368MNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36AMNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36AMNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CMNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CMNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L367MDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064KB-A	D Version
R5F2L367MDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0064GA-A	
R5F2L368MDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064KB-A	
R5F2L368MDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0064GA-A	
R5F2L36AMDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36AMDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	
R5F2L36CMDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064KB-A	
R5F2L36CMDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0064GA-A	

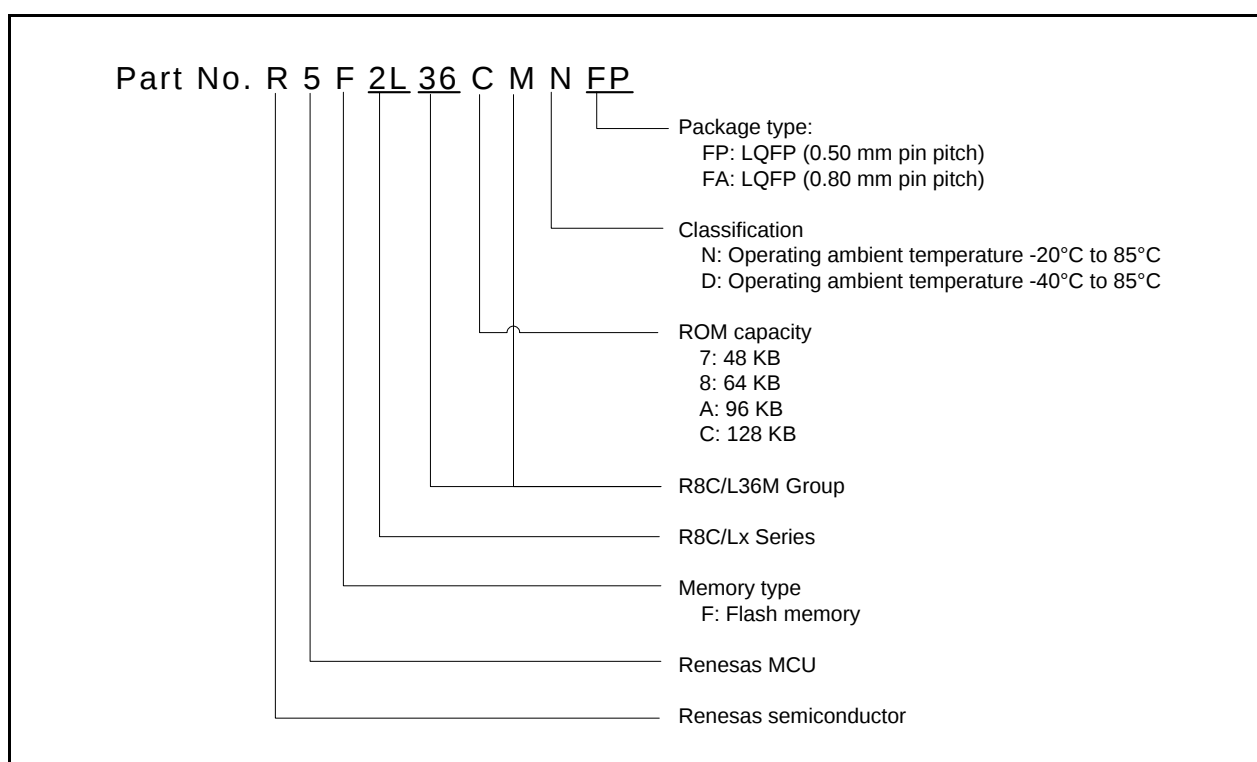
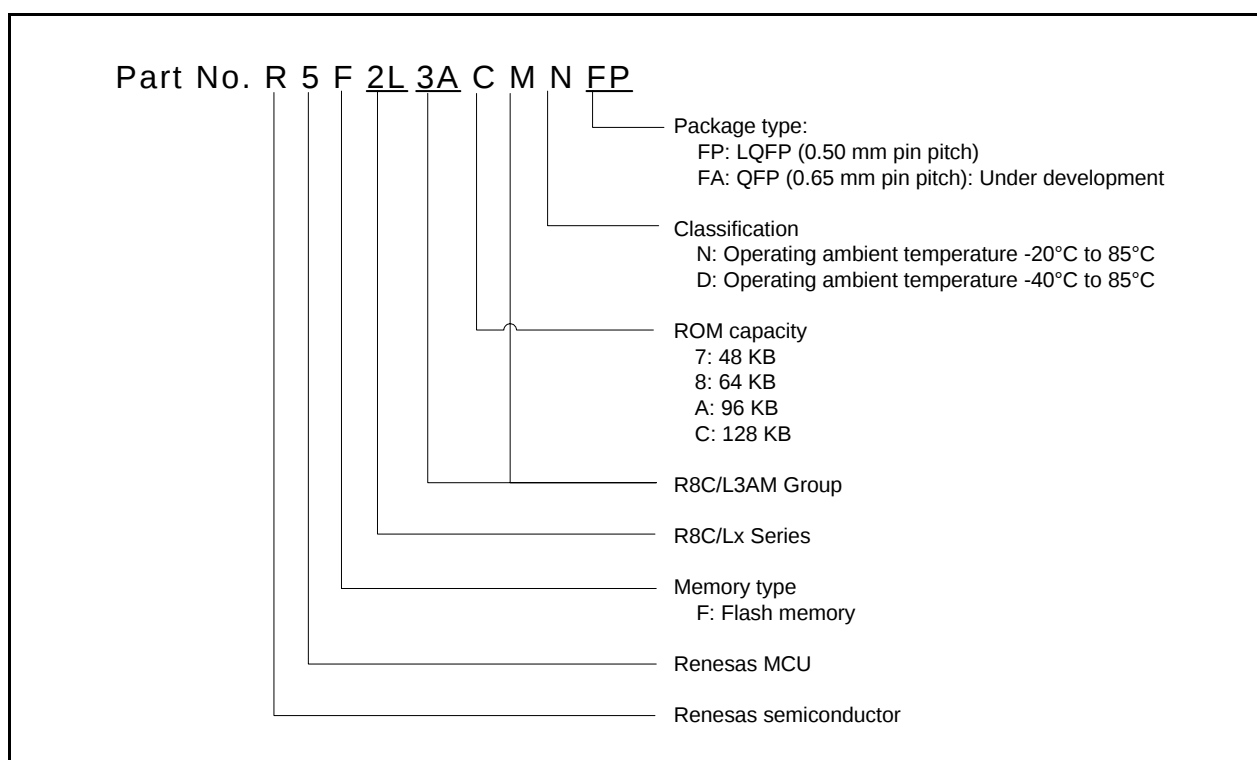
**Figure 1.2 Correspondence of Part No., with Memory Size and Package of R8C/L36M Group**

Table 1.10 Product List for R8C/L3AM Group**Current of Jun 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L3A7MNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7MNFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8MNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8MNFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AAMNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AAMNFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACMNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACMNFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3A7MDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7MDFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8MDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8MDFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AAMDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AAMDFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACMDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACMDFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	

(D): Under development

**Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/L3AM Group**

1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/L35M Group. Figure 1.6 shows a Block Diagram of R8C/L36M Group. Figure 1.7 shows a Block Diagram of R8C/L38M Group. Figure 1.8 shows a Block Diagram of R8C/L3AM Group.

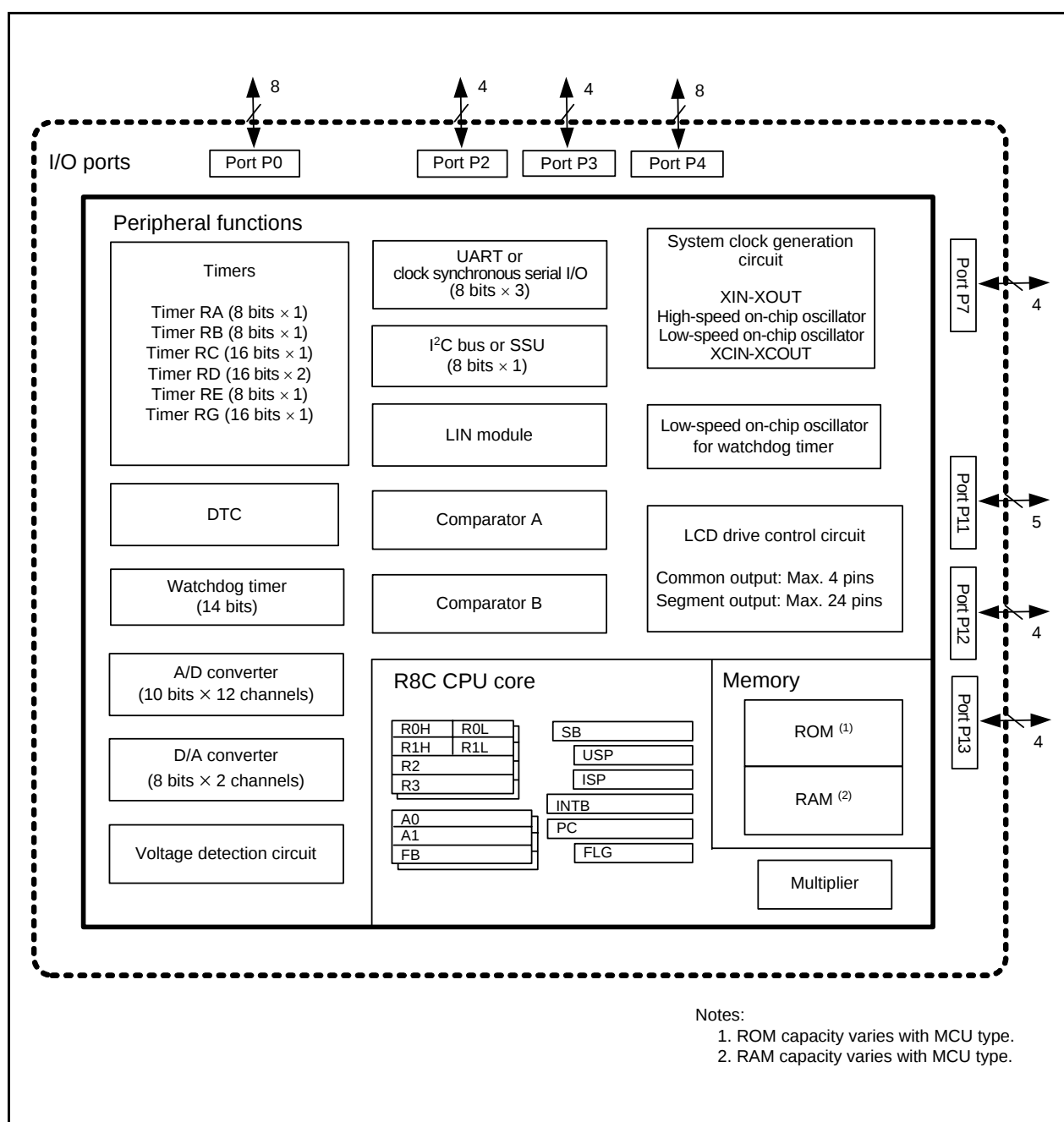


Figure 1.5 Block Diagram of R8C/L35M Group

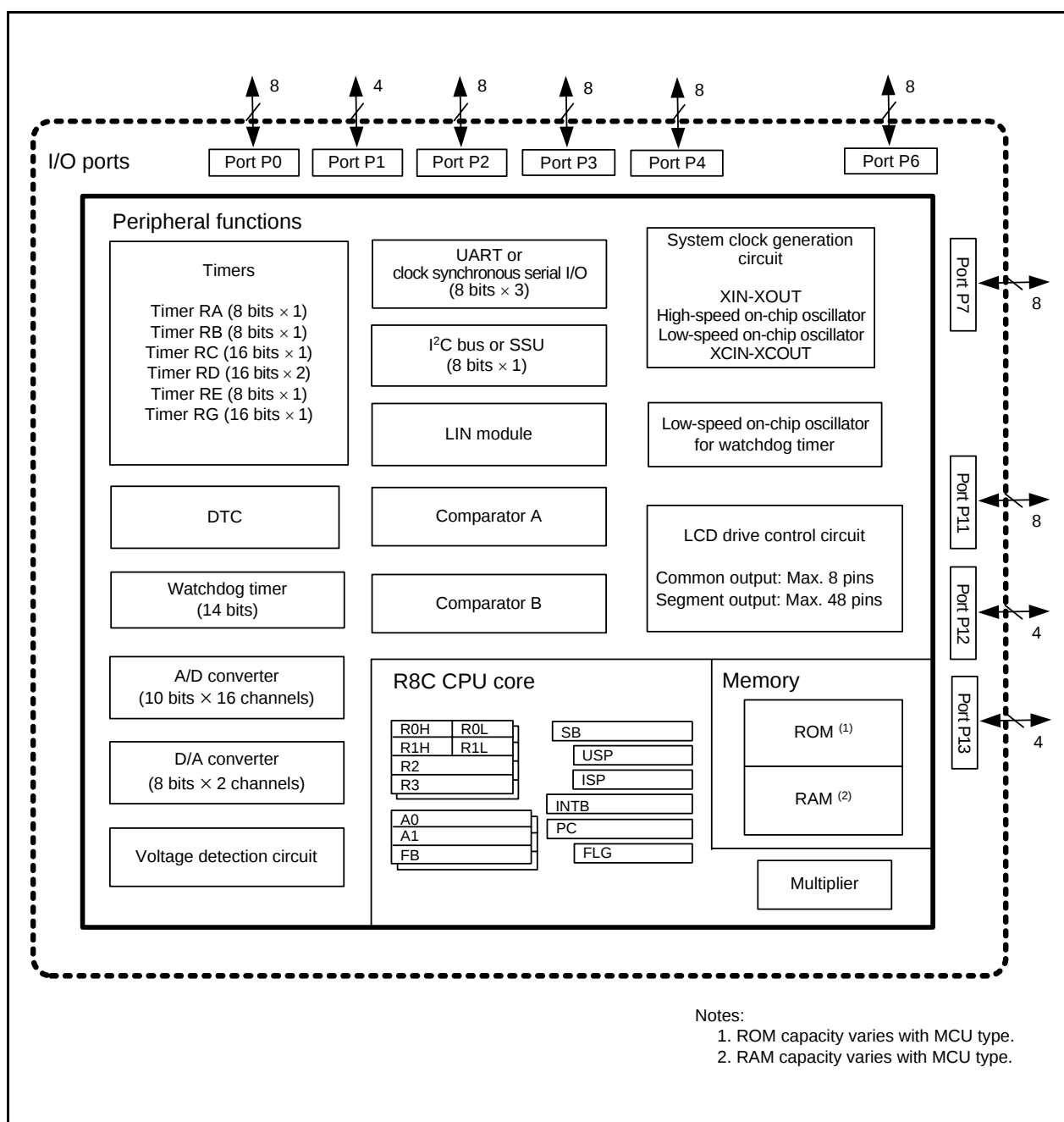


Figure 1.7 Block Diagram of R8C/L38M Group

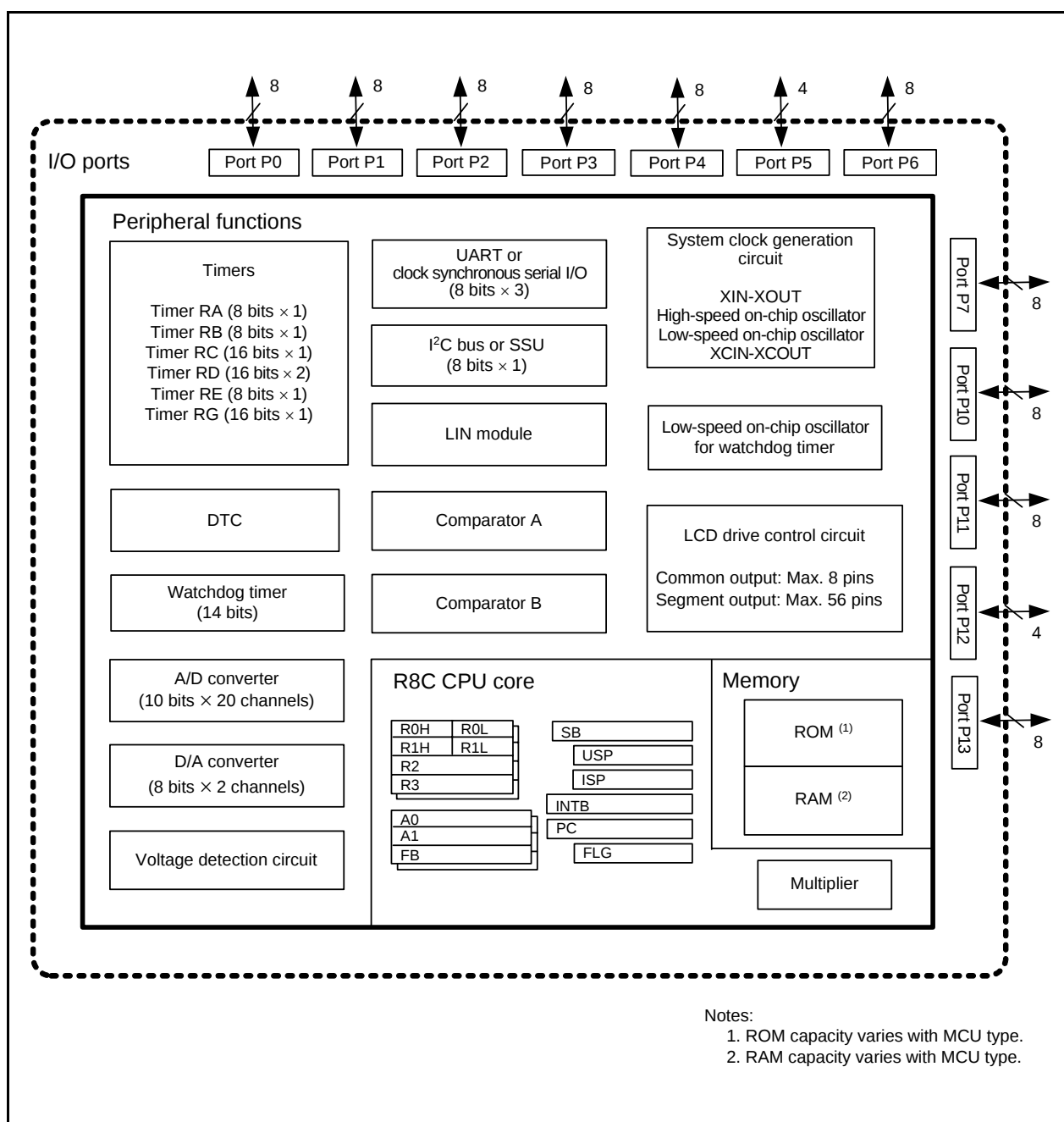


Figure 1.8 Block Diagram of R8C/L3AM Group

1.4 Pin Assignments

Figures 1.9 to 1.13 show Pin Assignments (Top View). Tables 1.11 to 1.13 list the Pin Name Information by Pin Number.

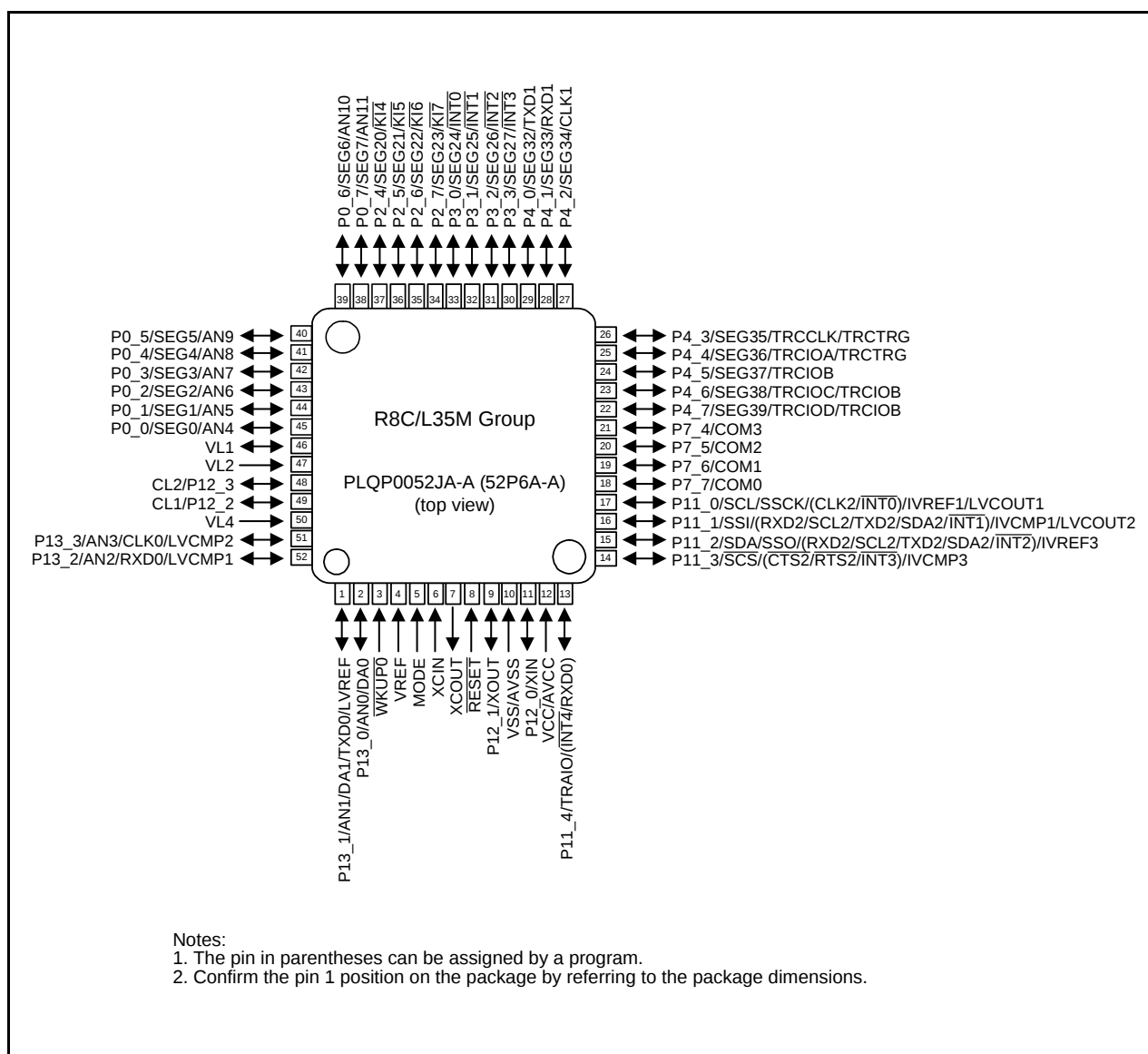


Figure 1.9 Pin Assignment (Top View) of PLQP0052JA-A Package

Table 1.11 Pin Name Information by Pin Number (1)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AM (Note 2)	L38M	L36M	L35M			Interrupt	Timer	Serial Interface	SSU	I ² C bus	A/D Converter, D/A Converter, Comparator A, Comparator B, Voltage Detection Circuit	LCD drive control circuit
1 [3]	80	61	51		P13_3			CLK0			AN3/LVCMP2	
2 [4]	1	62	52		P13_2			RXD0			AN2/LVCMP1	
3 [5]	2	63	1		P13_1			TXD0			AN1/DA1/LVREF	
4 [6]	3	64	2		P13_0						AN0/DA0	
5 [7]	4	1	3	WKUP0								
6 [8]	5	2	4	VREF								
7 [9]	6	3	5	MODE								
8 [10]	7	4	6	XCIN								
9 [11]	8	5	7	XCOU								
10 [12]	9	6	8	RESET								
11 [13]	10	7	9	XOUT	P12_1							
12 [14]	11	8	10	VSS/ AVSS								
13 [15]	12	9	11	XIN	P12_0							
14 [16]	13	10	12	VCC/ AVCC								
15 [17]	14	11			P11_7	(INT7)	TREO				(ADTRG)	
16 [18]	15	12			P11_6	(INT6)	TRBO					
17 [19]	16	13			P11_5	(INT5)	TRA0					
18 [20]	17	14	13		P11_4	(INT4)	TRAIO	(RXD0)				
19 [21]	18	15	14		P11_3	(INT3)		(CTS2/RTS2)	SCS		IVCMP3	
20 [22]	19	16	15		P11_2	(INT2)		(RXD2/SCL2/ TXD2/SDA2)	SSO	SDA	IVREF3	
21 [23]	20	17	16		P11_1	(INT1)		(RXD2/SCL2/ TXD2/SDA2)	SSI		IVCMP1/LVCOUT2	
22 [24]	21	18	17		P11_0	(INT0)		(CLK2)	SSCK	SCL	IVREF1/LVCOUT1	
23 [25]					P10_7	(KI7)	(TRDIOD1)					
24 [26]					P10_6	(KI6)	(TRDIOC1)					
25 [27]					P10_5	(KI5)	(TRDIOB1)					
26 [28]					P10_4	(KI4)	(TRDIOA1)					
27 [29]					P10_3	(KI3)	(TRDIOD0)					
28 [30]					P10_2	(KI2)	(TRDIOC0)					
29 [31]					P10_1	(KI1)	(TRDIOB0)					
30 [32]					P10_0	(KI0)	(TRDIOA0/ TRDCLK)					
31 [33]	22	19	18		P7_7							COM0
32 [34]	23	20	19		P7_6							COM1
33 [35]	24	21	20		P7_5							COM2
34 [36]	25	22	21		P7_4							COM3
35 [37]	26	23			P7_3							SEG55/ COM4
36 [38]	27	24			P7_2							SEG54/ COM5
37 [39]	28	25			P7_1							SEG53/ COM6
38 [40]	29	26			P7_0							SEG52/ COM7
39 [41]	30				P6_7		TRDIOD1					SEG51

Notes:

1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.16 list SFR Informations and Table 4.17 lists the ID Code Areas and Option Function Select Area. The description offered in this chapter is based on the R8C/L3AM Group.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00100000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	XXh (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h	Power-Off Mode Control Register 0	POMCR0	X0000000b
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit/Comparator A Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:

- Blank spaces are reserved. No access is allowed.
- The CWR bit in the RSTFR register is set to 0 after power-on, voltage monitor 0 reset, or exit from power-off mode. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
- The CSPROINI bit in the OFS register is set to 0.
- The LVDAS bit in the OFS register is set to 1.
- The LVDAS bit in the OFS register is set to 0.

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After Reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	D/A 0 Register	DA0	00h
00D9h	D/A 1 Register	DA1	00h
00DAh			
00DBh			
00DCh	D/A Control Register	DACON	00h
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h	Port P5 Register	P5	XXh
00EAh	Port P4 Direction Register	PD4	00h
00EBh	Port P5 Direction Register	PD5	00h
00ECh	Port P6 Register	P6	XXh
00EDh	Port P7 Register	P7	XXh
00EEh	Port P6 Direction Register	PD6	00h
00EFh	Port P7 Direction Register	PD7	00h
00F0h			
00F1h			
00F2h			
00F3h			
00F4h	Port P10 Register	P10	XXh
00F5h	Port P11 Register	P11	XXh
00F6h	Port P10 Direction Register	PD10	00h
00F7h	Port P11 Direction Register	PD11	00h
00F8h	Port P12 Register	P12	XXh
00F9h	Port P13 Register	P13	XXh
00FAh	Port P12 Direction Register	PD12	00h
00FBh	Port P13 Direction Register	PD13	00h
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.5 SFR Information (5) ⁽¹⁾

Address	Register	Symbol	After Reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h	LIN Control Register 2	LINCR2	00h
0106h	LIN Control Register	LINCR	00h
0107h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Timer RE Counter Data Register	TRESEC	XXh
0119h	Timer RE Minute Data Register / Timer RE Compare Data Register	TREMIN	XXh
011Ah	Timer RE Hour Data Register	TREHR	XXh
011Bh	Timer RE Day of Week Data Register	TREWK	XXh
011Ch	Timer RE Control Register 1	TRECR1	XXXXXX0XXb
011Dh	Timer RE Control Register 2	TRECR2	XXh
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h	Timer RC Trigger Control Register	TRCADCR	00h
0134h			
0135h	Timer RD Control Expansion Register	TRDECR	00h
0136h	Timer RD Trigger Control Register	TRDADCR	00h
0137h	Timer RD Start Register	TRDSTR	11111100b
0138h	Timer RD Mode Register	TRDMR	00001110b
0139h	Timer RD PWM Mode Register	TRDPMR	10001000b
013Ah	Timer RD Function Control Register	TRDFCR	10000000b
013Bh	Timer RD Output Master Enable Register 1	TRDOER1	FFh
013Ch	Timer RD Output Master Enable Register 2	TRDOER2	01111111b
013Dh	Timer RD Output Control Register	TRDOCR	00h
013Eh	Timer RD Digital Filter Function Select Register 0	TRDDF0	00h
013Fh	Timer RD Digital Filter Function Select Register 1	TRDDF1	00h

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.14 SFR Information (14) ⁽¹⁾

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACH			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

Table 4.15 SFR Information (15) ⁽¹⁾

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

- Blank spaces are reserved. No access is allowed.

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions
(VCC = 1.8 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter			Conditions	Standard			Unit	
					Min.	Typ.	Max.		
Vcc/AVcc	Supply voltage				1.8	—	5.5	V	
Vss/AVss	Supply voltage				—	0	—	V	
VIH	Input “H” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0.8 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.8 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.9 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.5 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0.85 Vcc	—	Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
VIL	Input “L” voltage	Other than CMOS input			4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.05 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.2 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.5 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection : 0.7 Vcc	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.55 Vcc	V
					2.7 V ≤ Vcc < 4.0 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
IOH(sum)	Peak sum output “H” current	Sum of all pins IOH(peak)				—	—	–160	mA
IOH(sum)	Average sum output “H” current	Sum of all pins IOH(avg)				—	—	–80	mA
IOH(peak)	Peak output “H” current	Port P10, P11 (2)				—	—	–40	mA
		Other pins				—	—	–10	mA
IOH(avg)	Average output “H” current (1)	Port P10, P11 (2)				—	—	–20	mA
		Other pins				—	—	–5	mA
IOL(sum)	Peak sum output “L” current	Sum of all pins IOL(peak)				—	—	160	mA
IOL(sum)	Average sum output “L” current	Sum of all pins IOL(avg)				—	—	80	mA
IOL(peak)	Peak output “L” current	Port P10, P11 (2)				—	—	40	mA
		Other pins				—	—	10	mA
IOL(avg)	Average output “L” current (1)	Port P10, P11 (2)				—	—	20	mA
		Other pins				—	—	5	mA
f(XIN)	XIN clock input oscillation frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
f(XCIN)	XCIN clock input oscillation frequency			1.8 V ≤ Vcc ≤ 5.5 V	—	32.768	50	kHz	
fOCO40M	When used as the count source for timer RC, timer RD, or timer RG (3)			2.7 V ≤ Vcc ≤ 5.5 V	32	—	40	MHz	
fOCO-F	fOCO-F frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
—	System clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	
f(BCLK)	CPU clock frequency			2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz	

Notes:

1. The average output current indicates the average value of current measured during 100 ms.
2. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.
3. fOCO40M can be used as the count source for timer RC, timer RD, or timer RG in the range of VCC = 2.7 V to 5.5V.

Table 5.4 D/A Converter Characteristics
($V_{CC}/AV_{CC} = V_{ref} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
t_{su}	Setup time		—	—	3	μs
R_o	Output resistor		—	6	—	$\text{k}\Omega$
I_{vref}	Reference power input current	(Note 1)	—	—	1.5	mA

Note:

1. This applies when one D/A converter is used and the value of the DAI register ($i = 0$ or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator A Characteristics
($V_{CC} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
LVREF	External reference voltage input range		1.4	—	V_{CC}	V
LVCMP1, LVCMP2	External comparison voltage input range		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	50	200	mV
—	Comparator output delay time ⁽¹⁾	At falling, $V_i = V_{ref} - 100$ mV	—	3	—	μs
		At falling, $V_i = V_{ref} - 1$ V or below	—	1.5	—	μs
		At rising, $V_i = V_{ref} + 100$ mV	—	2	—	μs
		At rising, $V_i = V_{ref} + 1$ V or above	—	0.5	—	μs
—	Comparator operating current	$V_{CC} = 5.0$ V	—	0.5	—	μA

Note:

1. When the digital filter is disabled.

Table 5.6 Comparator B Characteristics
($V_{CC} = 2.7$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	$V_{CC} - 1.4$	V
V_i	IVCMP1, IVCMP3 input voltage		-0.3	—	$V_{CC} + 0.3$	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time ⁽¹⁾	$V_i = V_{ref} \pm 100$ mV	—	0.1	—	μs
I_{CMP}	Comparator operating current	$V_{CC} = 5.0$ V	—	17.5	—	μA

Note:

1. When the digital filter is disabled.

Table 5.7 Flash Memory (Program ROM) Characteristics
(V_{CC} = 2.7 to 5.5 V and T_{opr} = 0 to 60°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽¹⁾		1,000 ⁽²⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Word program time		—	120	750	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	ms
—	Time from suspend until erase restart		—	—	30+CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly terminated until reading is enabled		—	—	30+CPU clock × 1 cycle	μs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁶⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. Definition of programming/erasure endurance
 The programming and erasure endurance is defined on a per-block basis.
 If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
 However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.9 Voltage Detection 0 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level V _{det0_0} ⁽¹⁾		1.80	1.90	2.05	V
	Voltage detection level V _{det0_1} ⁽¹⁾		2.15	2.35	2.50	V
	Voltage detection level V _{det0_2} ⁽¹⁾		2.70	2.85	3.05	V
	Voltage detection level V _{det0_3} ⁽¹⁾		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time ⁽³⁾	At the falling of V _{CC} from 5 V to (V _{det0_0} – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, V _{CC} = 5.0 V	—	1.5	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽²⁾		—	—	100	μs

Notes:

1. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.10 Voltage Detection 1 Circuit Characteristics
(V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level V _{det1_0} ⁽¹⁾	At the falling of V _{CC}	2.00	2.20	2.40	V
	Voltage detection level V _{det1_1} ⁽¹⁾	At the falling of V _{CC}	2.15	2.35	2.55	V
	Voltage detection level V _{det1_2} ⁽¹⁾	At the falling of V _{CC}	2.30	2.50	2.70	V
	Voltage detection level V _{det1_3} ⁽¹⁾	At the falling of V _{CC}	2.45	2.65	2.85	V
	Voltage detection level V _{det1_4} ⁽¹⁾	At the falling of V _{CC}	2.60	2.80	3.00	V
	Voltage detection level V _{det1_5} ⁽¹⁾	At the falling of V _{CC}	2.75	2.95	3.15	V
	Voltage detection level V _{det1_6} ⁽¹⁾	At the falling of V _{CC}	2.85	3.10	3.40	V
	Voltage detection level V _{det1_7} ⁽¹⁾	At the falling of V _{CC}	3.00	3.25	3.55	V
	Voltage detection level V _{det1_8} ⁽¹⁾	At the falling of V _{CC}	3.15	3.40	3.70	V
	Voltage detection level V _{det1_9} ⁽¹⁾	At the falling of V _{CC}	3.30	3.55	3.85	V
	Voltage detection level V _{det1_A} ⁽¹⁾	At the falling of V _{CC}	3.45	3.70	4.00	V
	Voltage detection level V _{det1_B} ⁽¹⁾	At the falling of V _{CC}	3.60	3.85	4.15	V
	Voltage detection level V _{det1_C} ⁽¹⁾	At the falling of V _{CC}	3.75	4.00	4.30	V
	Voltage detection level V _{det1_D} ⁽¹⁾	At the falling of V _{CC}	3.90	4.15	4.45	V
	Voltage detection level V _{det1_E} ⁽¹⁾	At the falling of V _{CC}	4.05	4.30	4.60	V
	Voltage detection level V _{det1_F} ⁽¹⁾	At the falling of V _{CC}	4.20	4.45	4.75	V
—	Hysteresis width at the rising of V _{CC} in voltage detection 1 circuit	V _{det1_0} to V _{det1_5} selected	—	0.07	—	V
		V _{det1_6} to V _{det1_F} selected	—	0.10	—	V
—	Voltage detection 1 circuit response time ⁽²⁾	At the falling of V _{CC} from 5 V to (V _{det1_0} – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 5.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.11 Voltage Detection 2 Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det2}	Voltage detection level V _{det2_0} ⁽¹⁾	At the falling of V _{CC}	3.70	4.00	4.30	V
	Voltage detection level V _{det2_EXT} ⁽¹⁾	At the falling of LVCMP2	1.24	1.34	1.44	V
—	Hysteresis width at the rising of V _{CC} in voltage detection 2 circuit		—	0.10	—	V
—	Voltage detection 2 circuit response time ⁽²⁾	At the falling of V _{CC} from 5 V to (V _{det2_0} – 0.1) V	—	20	150	μs
—	Voltage detection circuit self power consumption	VCA27 = 1, V _{CC} = 5.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽³⁾		—	—	100	μs

Notes:

1. The voltage detection level varies with detection targets. Select the level with the VCA24 bit in the VCA2 register.
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.12 Power-on Reset Circuit Characteristics ⁽¹⁾
($T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{trh}	External power V _{CC} rise gradient		0	—	50000	mV/msec

Note:

1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

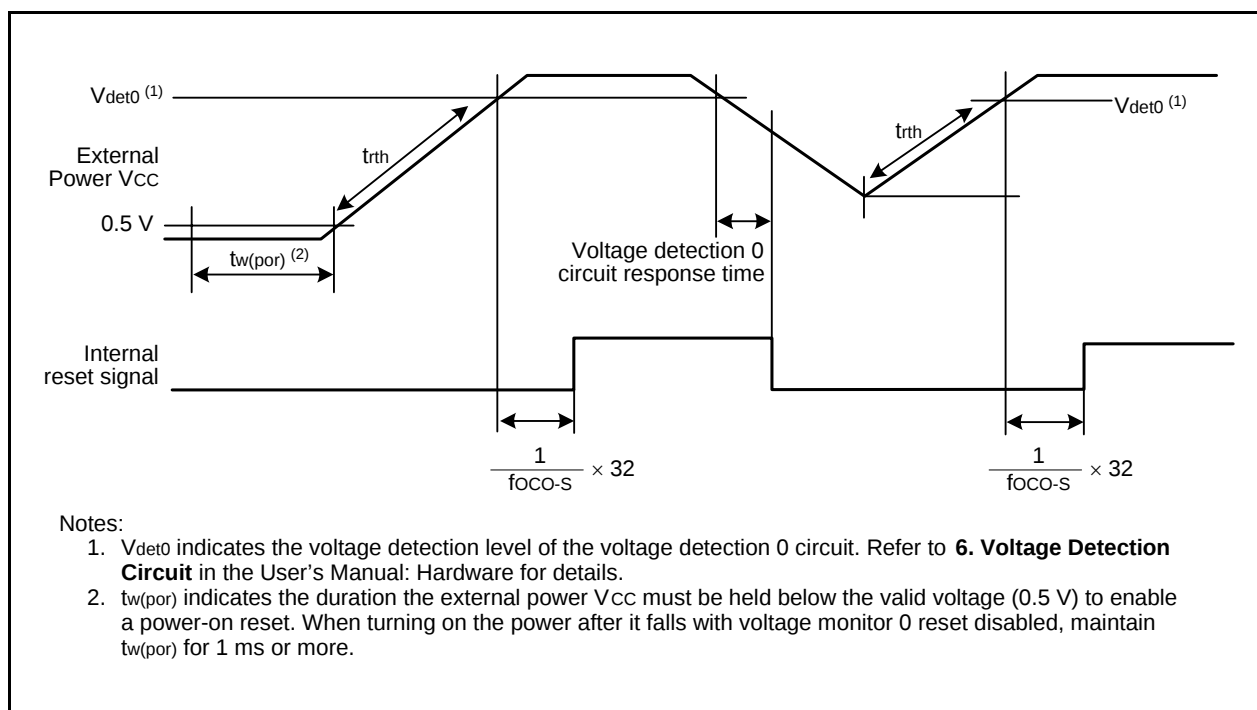


Figure 5.3 Power-on Reset Circuit Characteristics

Table 5.13 High-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min. (2)	Typ.	Max. (2)	
—	High-speed on-chip oscillator frequency after reset	$V_{CC} = 1.8$ V to 5.5 V $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	39.4	40	40.6	MHz
		$V_{CC} = 1.8$ V to 5.5 V $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	39.4	40	40.6	MHz
		$V_{CC} = 1.8$ V to 5.5 V $T_{opr} = 25^{\circ}\text{C}$	39.6	40	40.4	MHz
	High-speed on-chip oscillator frequency when the FRA4 register correction value is written into the FRA1 register and the FRA5 register correction value into the FRA3 register (1)	$V_{CC} = 1.8$ V to 5.5 V $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	36.311	36.864	37.417	MHz
		$V_{CC} = 1.8$ V to 5.5 V $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	36.311	36.864	37.417	MHz
		$V_{CC} = 1.8$ V to 5.5 V $T_{opr} = 25^{\circ}\text{C}$	36.495	36.864	37.233	MHz
	High-speed on-chip oscillator frequency when the FRA6 register correction value is written into the FRA1 register and the FRA7 register correction value into the FRA3 register	$V_{CC} = 1.8$ V to 5.5 V $-20^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	31.52	32	32.48	MHz
		$V_{CC} = 1.8$ V to 5.5 V $-40^{\circ}\text{C} \leq T_{opr} \leq 85^{\circ}\text{C}$	31.52	32	32.48	MHz
		$V_{CC} = 1.8$ V to 5.5 V $T_{opr} = 25^{\circ}\text{C}$	31.68	32	32.32	MHz
—	Oscillation stability time	$V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$	—	100	450	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$	—	500	—	μA

Notes:

1. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.
2. The minimum and maximum values are TBD for the R8C/L3AM Group (0.65-mm pin pitch) only.

Table 5.14 Low-speed On-Chip Oscillator Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V and $T_{opr} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		112.5	125	137.5	kHz
—	Oscillation stability time	$V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$	—	30	100	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$	—	3	—	μA
fOCO-WDT	Low-speed on-chip oscillator frequency for the watchdog timer		60	125	250	kHz
—	Oscillation stability time	$V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$	—	30	100	μs
—	Self power consumption at oscillation	$V_{CC} = 5.0$ V, $T_{opr} = 25^{\circ}\text{C}$	—	2	—	μA

Table 5.15 Power Supply Circuit Characteristics
($V_{CC} = 1.8$ to 5.5 V, $V_{SS} = 0$ V, and $T_{opr} = 25^{\circ}\text{C}$, unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (1)		—	—	2000	μs

Note:

1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.25 Timing Requirements of I²C bus Interface ⁽¹⁾
(V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12tcyc + 600 ⁽¹⁾	—	—	ns
t _{SCLH}	SCL input "H" width		3tcyc + 300 ⁽¹⁾	—	—	ns
t _{SCLL}	SCL input "L" width		5tcyc + 500 ⁽¹⁾	—	—	ns
t _{sf}	SCL, SDA input fall time		—	—	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		—	—	1tcyc ⁽¹⁾	ns
t _{BUF}	SDA input bus-free time		5tcyc ⁽¹⁾	—	—	ns
t _{STAH}	Start condition input hold time		3tcyc ⁽¹⁾	—	—	ns
t _{STAS}	Retransmit start condition input setup time		3tcyc ⁽¹⁾	—	—	ns
t _{STOP}	Stop condition input setup time		3tcyc ⁽¹⁾	—	—	ns
t _{SDAS}	Data input setup time		1tcyc + 40 ⁽¹⁾	—	—	ns
t _{SDAH}	Data input hold time		10	—	—	ns

Note:

1. 1tcyc = 1/f₁(s)

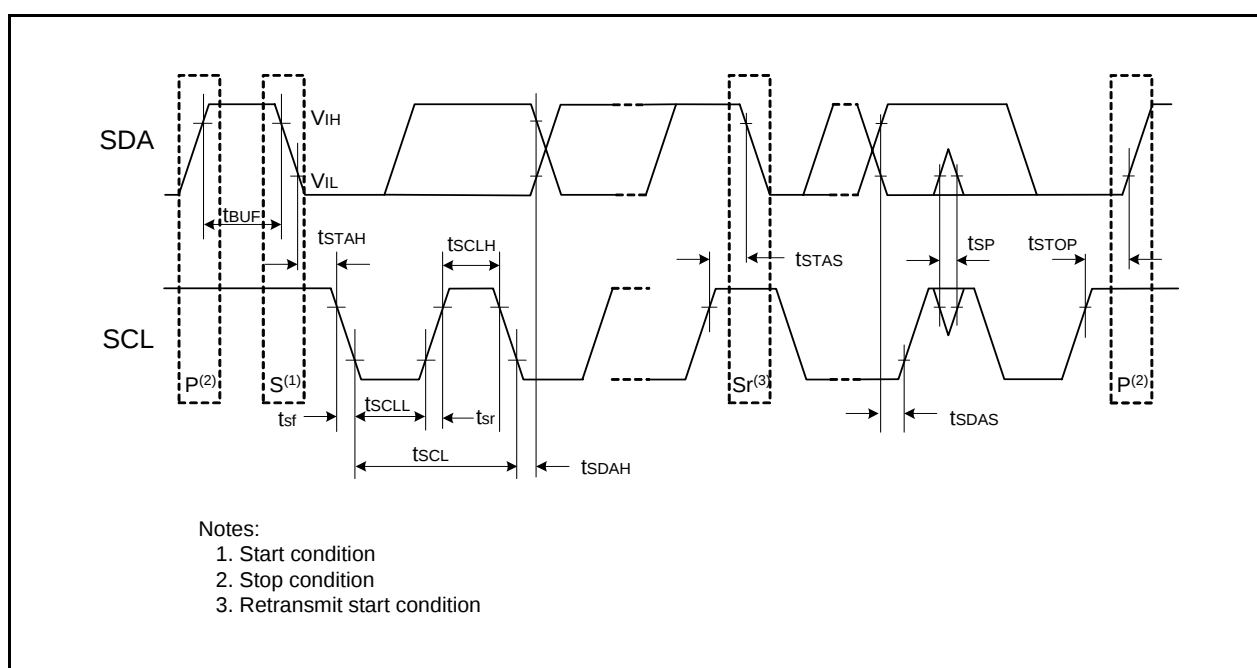


Figure 5.7 I/O Timing of I²C bus Interface

REVISION HISTORY

R8C/L35M Group, R8C/L36M Group, R8C/L38M Group, R8C/L3AM Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Sep 30, 2010	—	First Edition issued
0.02	Nov 02, 2010	All 29 45 to 68	“Preliminary” is added Table 4.1 0030h “Voltage Monitor Circuit Control Register” → “Voltage Monitor Circuit/Comparator A Control Register” “5. Electrical Characteristics” added
0.03	Apr 15, 2011	2 3 6 28 38 to 40 53 54 57, 59, 61	Table 1.1 “Timers” deleted Table 1.2 Note 2, Table 1.3 Note 1 revised Table 1.6 “Current Consumption” revised 3. “The internal ROM ... with address 0FFFFh.” deleted Table 4.10 to Table 4.12 “0248h to 026Fh”, “02A8h to 02BFh”, “02C0h to 02CFh” revised Table 5.11 “Vdet2” revised Table 5.13 revised, Note 2 added Table 5.19, Table 5.21, Table 5.23 “High-Speed” → “High-Speed (fOCO-F)”, “Power-off mode” revised
1.00	Jun 28, 2011	10 50 54	Table 1.10, Figure 1.4 revised Table 5.7 revised Table 5.13 revised

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