Renesas Electronics America Inc - R5F2L3ACMDFA#U0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	LCD, POR, PWM, Voltage Detect, WDT
Number of I/O	88
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2l3acmdfa-u0

Table 1.9 Product List for R8C/L38M Group **Current of Jun 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L387MNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	N Version
R5F2L387MNFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080JA-A	
R5F2L388MNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2L388MNFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080JA-A	
R5F2L38AMNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38AMNFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L38CMNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38CMNFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L387MDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	D Version
R5F2L387MDFA	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080JA-A	
R5F2L388MDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2L388MDFA	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080JA-A	
R5F2L38AMDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38AMDFA	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	
R5F2L38CMDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F2L38CMDFA	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080JA-A	

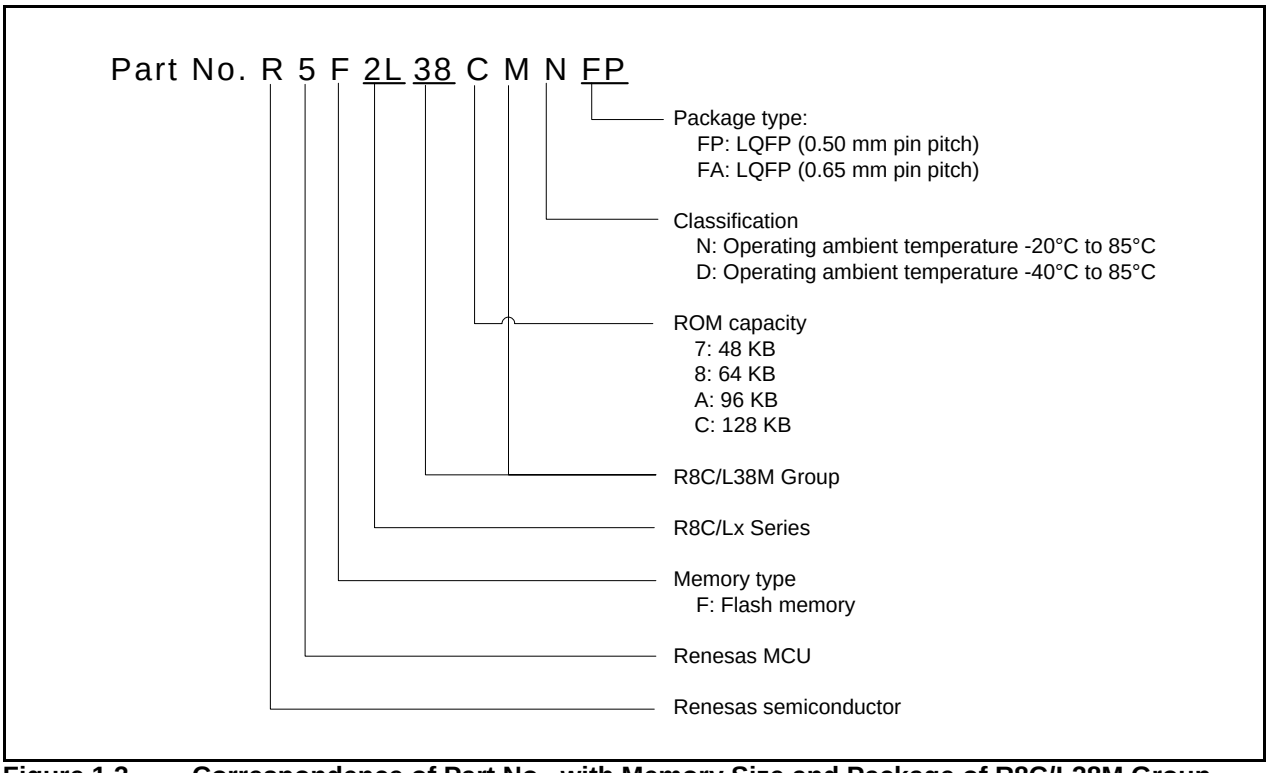


Figure 1.3 Correspondence of Part No., with Memory Size and Package of R8C/L38M Group

Table 1.10 Product List for R8C/L3AM Group **Current of Jun 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2L3A7MNFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	N Version
R5F2L3A7MNFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8MNFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8MNFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AAMNFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AAMNFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACMNFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACMNFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3A7MDFP	48 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0100KB-A	D Version
R5F2L3A7MDFA (D)	48 Kbytes	1 Kbyte × 4	6 Kbytes	PRQP0100JD-B	
R5F2L3A8MDFP	64 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0100KB-A	
R5F2L3A8MDFA (D)	64 Kbytes	1 Kbyte × 4	8 Kbytes	PRQP0100JD-B	
R5F2L3AAMDFP	96 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3AAMDFA (D)	96 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	
R5F2L3ACMDFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0100KB-A	
R5F2L3ACMDFA (D)	128 Kbytes	1 Kbyte × 4	10 Kbytes	PRQP0100JD-B	

(D): Under development

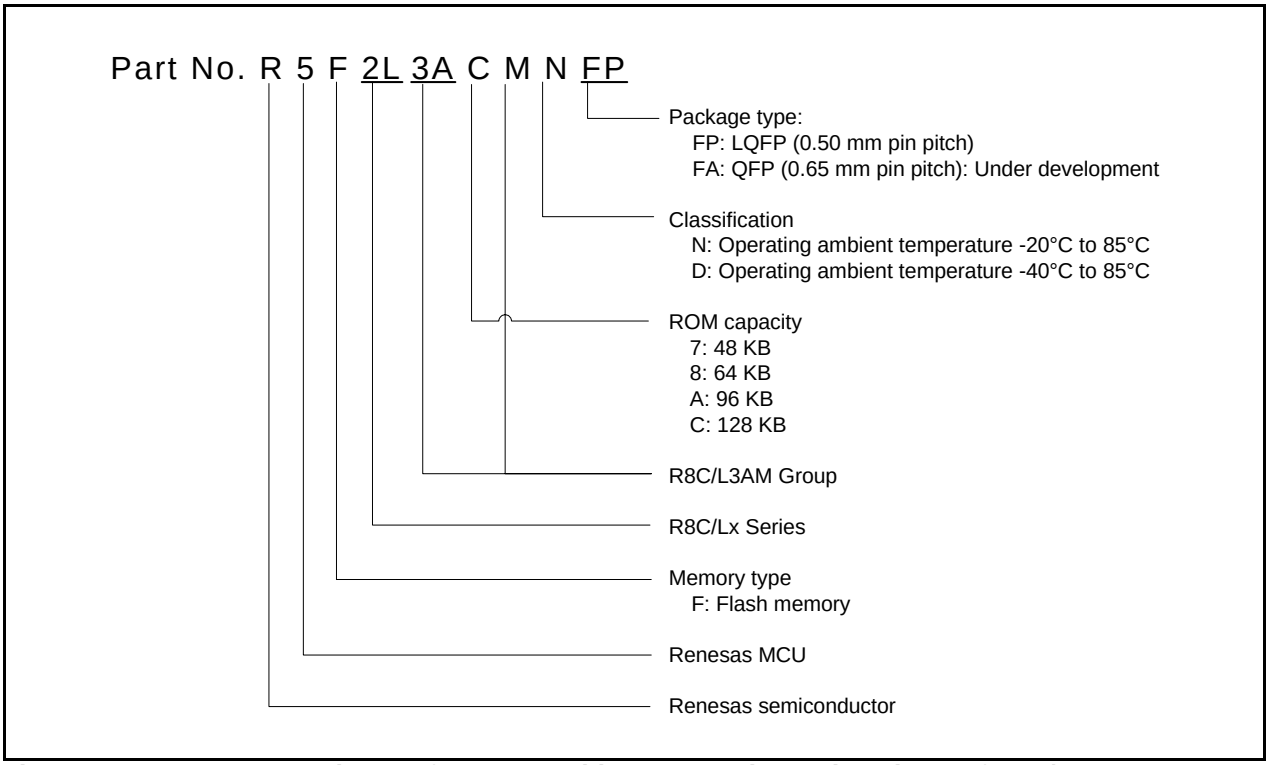
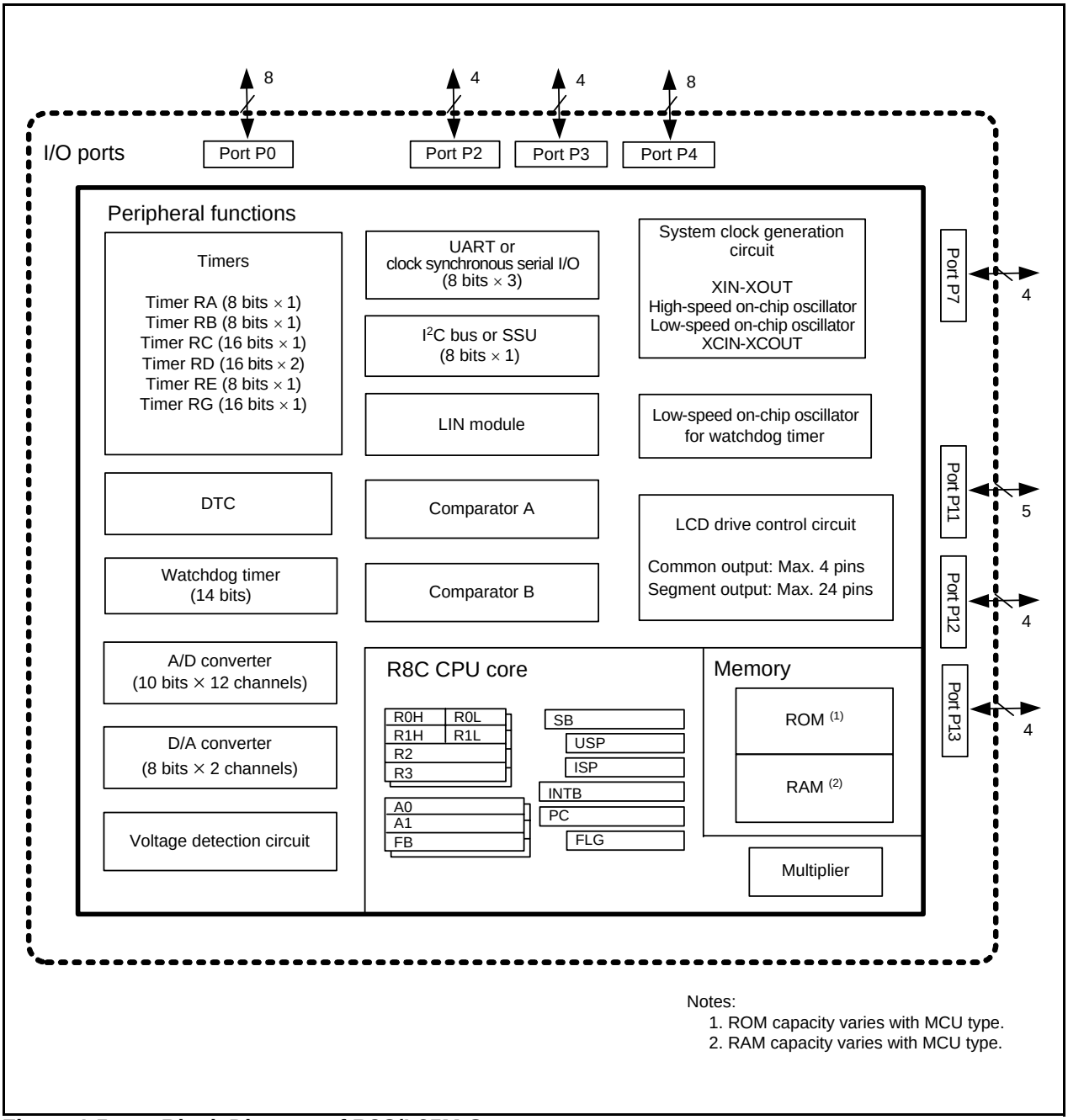


Figure 1.4 Correspondence of Part No., with Memory Size and Package of R8C/L3AM Group

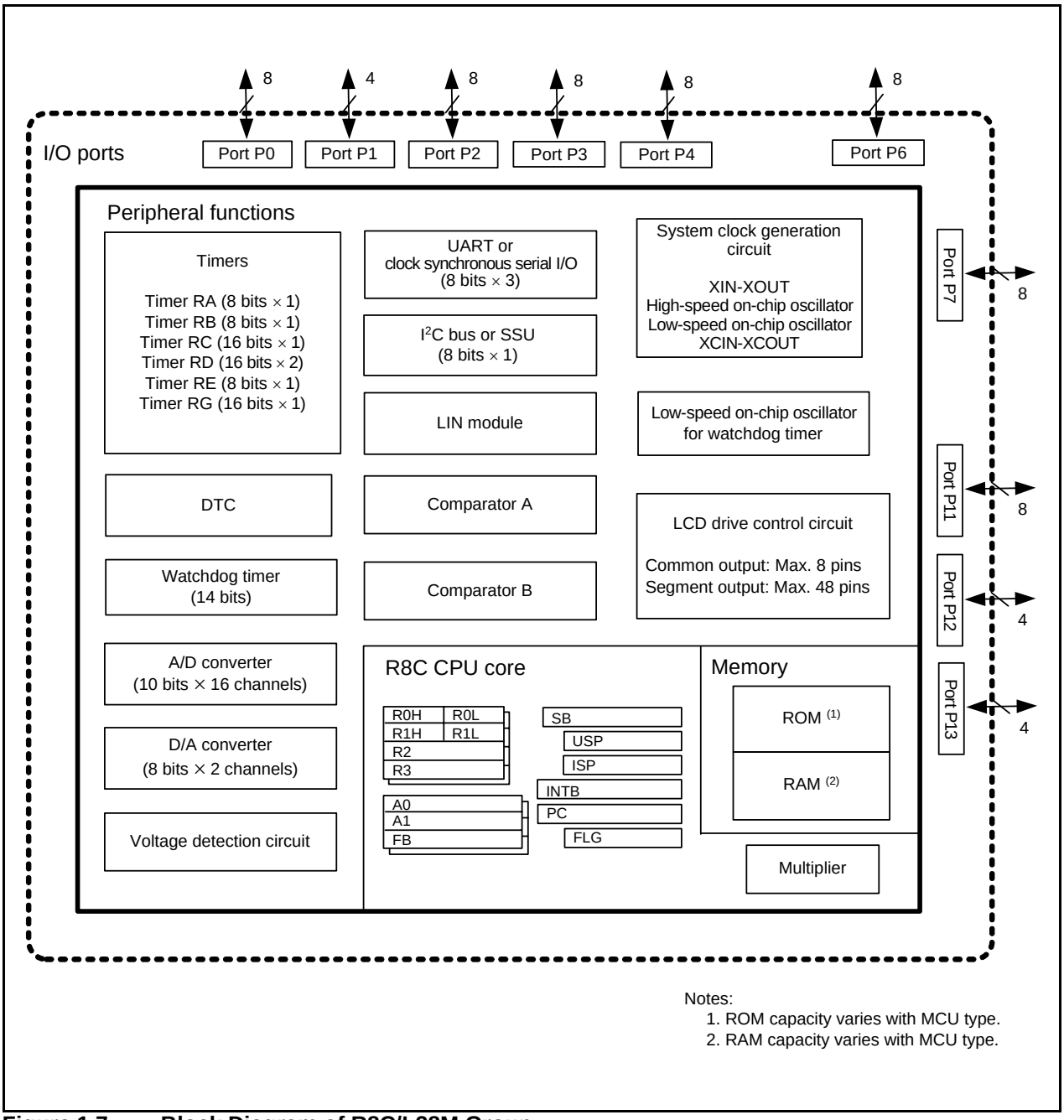
1.3 Block Diagrams

Figure 1.5 shows a Block Diagram of R8C/L35M Group. Figure 1.6 shows a Block Diagram of R8C/L36M Group. Figure 1.7 shows a Block Diagram of R8C/L38M Group. Figure 1.8 shows a Block Diagram of R8C/L3AM Group.



Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.5 Block Diagram of R8C/L35M Group



Notes:
1. ROM capacity varies with MCU type.
2. RAM capacity varies with MCU type.

Figure 1.7 Block Diagram of R8C/L38M Group

Table 1.12 Pin Name Information by Pin Number (2)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AM (Note 2)	L38M	L36M	L35M			Interrupt	Timer	Serial Interface	SSU	I²C bus	A/D Converter, D/A Converter, Comparator A, Comparator B, Voltage Detection Circuit	LCD drive control circuit
40 [42]	31				P6_6		TRDIOC1					SEG50
41 [43]	32				P6_5		TRDIOB1					SEG49
42 [44]	33				P6_4		TRDIOA1					SEG48
43 [45]	34				P6_3		TRDIOD0					SEG47
44 [46]	35				P6_2		TRDIOC0					SEG46
45 [47]	36				P6_1		TRDIOB0					SEG45
46 [48]	37				P6_0		TRDIOA0/ TRDCLK					SEG44
47 [49]					P5_3							SEG43
48 [50]					P5_2							SEG42
49 [51]					P5_1							SEG41
50 [52]					P5_0							SEG40
51 [53]	38	27	22		P4_7		TRCIOD/ TRCIOB					SEG39
52 [54]	39	28	23		P4_6		TRCIOC/ TRCIOB					SEG38
53 [55]	40	29	24		P4_5		TRCIOB					SEG37
54 [56]	41	30	25		P4_4		TRCIOA/ TRCTRG					SEG36
55 [57]	42	31	26		P4_3		TRCCLK/ TRCTRG					SEG35
56 [58]	43	32	27		P4_2			CLK1				SEG34
57 [59]	44	33	28		P4_1			RXD1				SEG33
58 [60]	45	34	29		P4_0			TXD1				SEG32
59 [61]	46	35			P3_7	$\overline{\text{INT7}}$	TRCTRG				$\overline{\text{ADTRG}}$	SEG31
60 [62]	47	36			P3_6	$\overline{\text{INT6}}$						SEG30
61 [63]	48	37			P3_5	$\overline{\text{INT5}}$						SEG29
62 [64]	49	38			P3_4	$\overline{\text{INT4}}$						SEG28
63 [65]	50	39	30		P3_3	$\overline{\text{INT3}}$						SEG27
64 [66]	51	40	31		P3_2	$\overline{\text{INT2}}$						SEG26
65 [67]	52	41	32		P3_1	$\overline{\text{INT1}}$						SEG25
66 [68]	53	42	33		P3_0	$\overline{\text{INT0}}$						SEG24
67 [69]	54	43	34		P2_7	$\overline{\text{KI7}}$						SEG23
68 [70]	55	44	35		P2_6	$\overline{\text{KI6}}$						SEG22
69 [71]	56	45	36		P2_5	$\overline{\text{KI5}}$						SEG21
70 [72]	57	46	37		P2_4	$\overline{\text{KI4}}$						SEG20
71 [73]	58				P2_3	$\overline{\text{KI3}}$						SEG19
72 [74]	59				P2_2	$\overline{\text{KI2}}$						SEG18
73 [75]	60				P2_1	$\overline{\text{KI1}}$						SEG17
74 [76]	61				P2_0	$\overline{\text{KI0}}$						SEG16
75 [77]					P1_7							SEG15
76 [78]					P1_6							SEG14
77 [79]					P1_5							SEG13
78 [80]					P1_4							SEG12
79 [81]	62				P1_3						AN15	SEG11
80 [82]	63				P1_2						AN14	SEG10
81 [83]	64				P1_1						AN13	SEG9
82 [84]	65				P1_0						AN12	SEG8
83 [85]	66	47	38		P0_7						AN11	SEG7
84 [86]	67	48	39		P0_6						AN10	SEG6

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

Table 1.13 Pin Name Information by Pin Number (3)

Pin Number				Control Pin	Port	I/O Pin Functions for Peripheral Modules						
L3AM (Note 2)	L38M	L36M	L35M			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter, Comparator A, Comparator B, Voltage Detection Circuit	LCD drive control circuit
85 [87]	68	49	40		P0_5						AN9	SEG5
86 [88]	69	50	41		P0_4						AN8	SEG4
87 [89]	70	51	42		P0_3						AN7	SEG3
88 [90]	71	52	43		P0_2						AN6	SEG2
89 [91]	72	53	44		P0_1						AN5	SEG1
90 [92]	73	54	45		P0_0						AN4	SEG0
91 [93]	74	55	46									VL1
92 [94]	75	56	47									VL2
93 [95]	76	57										VL3
94 [96]	77	58	48		P12_3							CL2
95 [97]	78	59	49		P12_2							CL1
96 [98]	79	60	50									VL4
97 [99]					P13_7		TRGCLKB				AN19	
98 [100]					P13_6		TRGIOB				AN18	
99 [1]					P13_5		TRGCLKA				AN17	
100 [2]					P13_4		TRGIOA				AN16	

Notes:
1. The pin in parentheses can be assigned by a program.
2. The number in brackets indicates the pin number for the 100P6F package.

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

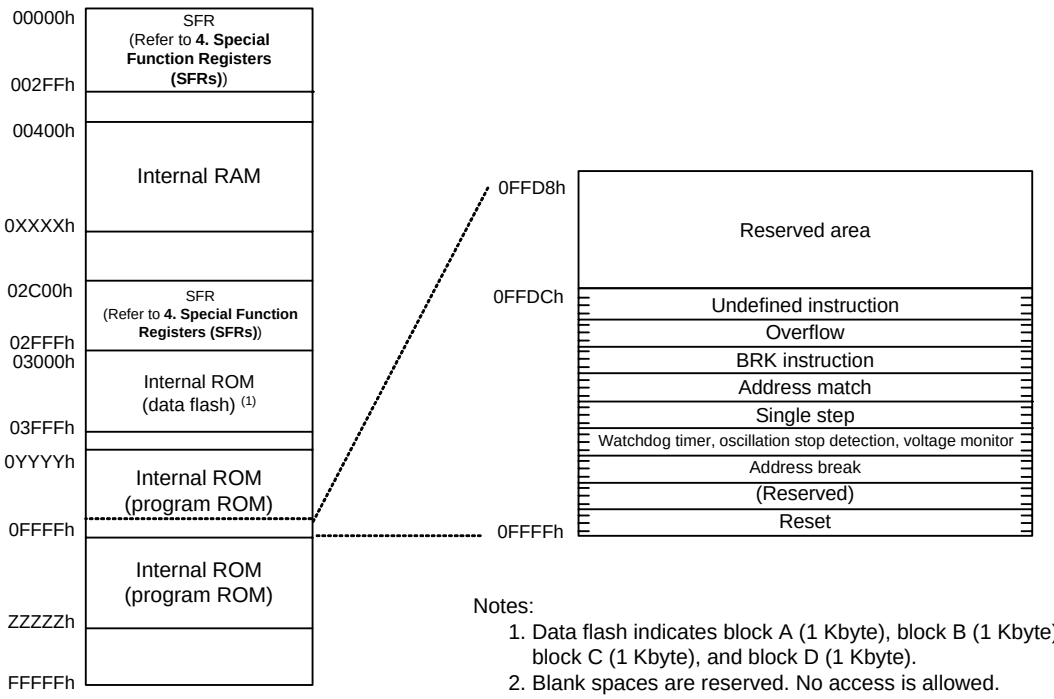
Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

3. Memory

Figure 3.1 is a Memory Map of each group. Each group has a 1-Mbyte address space from addresses 00000h to FFFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM			Internal RAM	
	Capacity	Address 0YYYYh	Address ZZZZZh	Capacity	Address 0XXXXh
R5F2L357M***, R5F2L367M***, R5F2L387M***, R5F2L3A7M***	48 Kbytes	04000h	–	6 Kbytes	01BFFh
R5F2L358M***, R5F2L368M***, R5F2L388M***, R5F2L3A8M***	64 Kbytes	04000h	13FFFh	8 Kbytes	023FFh
R5F2L35AM***, R5F2L36AM***, R5F2L38AM***, R5F2L3AAM***	96 Kbytes	04000h	1BFFFh	10 Kbytes	02BFFh
R5F2L35CM***, R5F2L36CM***, R5F2L38CM***, R5F2L3ACM***	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
0280h	LCD Display Control Data Register	LRA16H	XXh
0281h		LRA17H	XXh
0282h		LRA18H	XXh
0283h		LRA19H	XXh
0284h		LRA20H	XXh
0285h		LRA21H	XXh
0286h		LRA22H	XXh
0287h		LRA23H	XXh
0288h		LRA24H	XXh
0289h		LRA25H	XXh
028Ah		LRA26H	XXh
028Bh		LRA27H	XXh
028Ch		LRA28H	XXh
028Dh		LRA29H	XXh
028Eh		LRA30H	XXh
028Fh		LRA31H	XXh
0290h		LRA32H	XXh
0291h		LRA33H	XXh
0292h		LRA34H	XXh
0293h		LRA35H	XXh
0294h		LRA36H	XXh
0295h		LRA37H	XXh
0296h		LRA38H	XXh
0297h		LRA39H	XXh
0298h		LRA40H	XXh
0299h		LRA41H	XXh
029Ah		LRA42H	XXh
029Bh		LRA43H	XXh
029Ch		LRA44H	XXh
029Dh		LRA45H	XXh
029Eh		LRA46H	XXh
029Fh		LRA47H	XXh
02A0h		LRA48H	XXh
02A1h		LRA49H	XXh
02A2h		LRA50H	XXh
02A3h		LRA51H	XXh
02A4h		LRA52H	XXh
02A5h		LRA53H	XXh
02A6h		LRA54H	XXh
02A7h		LRA55H	XXh
02A8h			
02A9h			
02AAh			
02ABh			
02ACh			
02ADh			
02AEh			
02AFh			
02B0h			
02B1h			
02B2h			
02B3h			
02B4h			
02B5h			
02B6h			
02B7h			
02B8h			
02B9h			
02BAh			
02BBh			
02BCh			
02BDh			
02BEh			
02BFh			

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined
Note:
1. Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage			–0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.65	V
		XIN	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		VL1		–0.3 to VL2	V
		VL2	R8C/L35M	VL1 to VL4	V
			R8C/L36M, R8C/L38M, R8C/L3AM	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		VL3 to 6.5	V
		Other pins		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation buffer ON) (1)	–0.3 to 1.65	V
		XOUT	XIN-XOUT oscillation on (oscillation buffer OFF) (1)	–0.3 to V_{CC} + 0.3	V
		VL1		–0.3 to VL2 (2)	V
		VL2	R8C/L35M	VL1 to VL4	V
			R8C/L36M, R8C/L38M, R8C/L3AM	VL1 to VL3	V
		VL3		VL2 to VL4	V
		VL4		–0.3 to 6.5	V
		CL1, CL2		–0.3 to 6.5	V
		COM0 to COM7		–0.3 to VL4	V
		SEG0 to SEG55		–0.3 to VL4	V
		Other pins		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation		–40°C ≤ T_{opr} ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature			–20 to 85 (N version) / –40 to 85 (D version)	°C
T_{stg}	Storage temperature			–65 to 150	°C

Notes:
1. For the register settings for each operation, refer to **7. I/O Ports** and **9. Clock Generation Circuit** in the User's Manual: Hardware.
2. The VL1 voltage should be VCC or below.

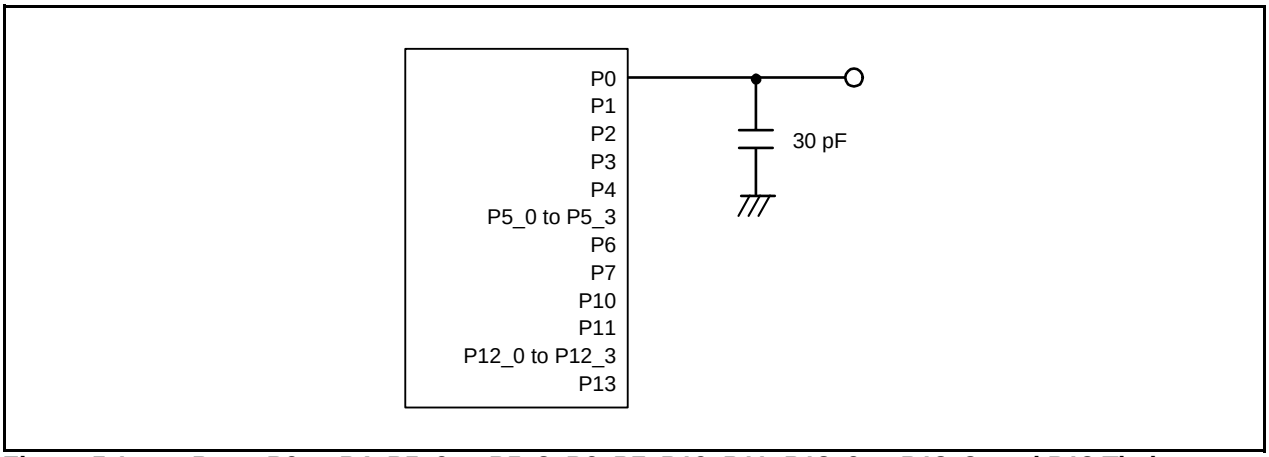


Figure 5.1 Ports P0 to P4, P5_0 to P5_3, P6, P7, P10, P11, P12_0 to P12_3, and P13 Timing Measurement Circuit

Table 5.4 D/A Converter Characteristics
(VCC/AVCC = Vref = 2.7 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bit
—	Absolute accuracy		—	—	2.5	LSB
tsu	Setup time		—	—	3	µs
RO	Output resistor		—	6	—	kΩ
IVref	Reference power input current	(Note 1)	—	—	1.5	mA

Note:
1. This applies when one D/A converter is used and the value of the DAi register (i = 0 or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included.

Table 5.5 Comparator A Characteristics
(VCC = 2.7 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
LVREF	External reference voltage input range		1.4	–	VCC	V
LVCMP1, LVCMP2	External comparison voltage input range		–0.3	–	VCC + 0.3	V
–	Offset		–	50	200	mV
–	Comparator output delay time (1)	At falling, VI = Vref – 100 mV	–	3	–	µs
		At falling, VI = Vref – 1 V or below	–	1.5	–	µs
		At rising, VI = Vref + 100 mV	–	2	–	µs
		At rising, VI = Vref + 1 V or above	–	0.5	–	µs
–	Comparator operating current	VCC = 5.0 V	–	0.5	–	µA

Note:
1. When the digital filter is disabled.

Table 5.6 Comparator B Characteristics
(VCC = 2.7 to 5.5 V and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vref	IVREF1, IVREF3 input reference voltage		0	—	VCC – 1.4	V
VI	IVCMP1, IVCMP3 input voltage		–0.3	—	VCC + 0.3	V
—	Offset		—	5	100	mV
td	Comparator output delay time (1)	VI = Vref ± 100 mV	—	0.1	—	µs
ICMP	Comparator operating current	VCC = 5.0 V	—	17.5	—	µA

Note:
1. When the digital filter is disabled.

Table 5.16 LCD Drive Control Circuit Characteristics (VCC = 1.8 to 5.5 V, VSS = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
VLCD	LCD power supply voltage	VLCD = VL4	2.2	—	5.5	V
VL3	VL3 voltage		VL2	—	VL4	V
VL2	VL2 voltage	R8C/L35M	VL1	—	VL4	V
		R8C/L36M, R8C/L38M, R8C/L3AM	VL1	—	VL3	V
VL1	VL1 voltage		1	—	VL2 (3)	V
—	VL1 internally-generated voltage accuracy (1)		Setting voltage –0.2	Setting voltage	Setting voltage +0.2	V
f(FR)	Frame frequency		50	—	180	Hz
ILCD	LCD drive control circuit current		—	(Note 2)	—	µA

Notes:
1. The voltage is selected with bits LVLS0 to LVLS3 in the LCR1 register.
2. Refer to **Table 5.19 DC Characteristics (2)**, **Table 5.21 DC Characteristics (4)**, and **Table 5.23 DC Characteristics (6)**.
3. The VL1 voltage should be VCC or below.

Table 5.17 Power-Off Mode Characteristics (VCC = 2.2 to 5.5 V, VSS = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Power-off mode operating supply voltage		2.2	—	5.5	V

Table 5.19 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ. (3)	Max.	
			XIN (2)	XCIN	High-Speed (fOCO-F)	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	7.0	15	mA
			16 MHz	Off	Off	125 kHz	No division	—		—	5.6	12.5	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	3.6	—	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—		—	3.0	—	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	—		—	2.2	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	4 MHz	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRD = 1 MSTTRC = 1 MSTTRG = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 VCA20 = 0		—	90	400	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 VCA20 = 0		—	100	400	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 VCA20 = 0	Flash memory off Program operation on RAM	—	55	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	100	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	90	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 0	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode	LCD drive control circuit (4) When external division resistors are used	—	7	—	µA
										LCD drive control circuit (5) When the internal voltage multiplier is used	—	12	—	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 VCA20 = 1 CM02 = 1 CM01 = 1	While a WAIT instruction is executed Peripheral clock off Timer RE operation in real-time clock mode		—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off		—	2.0	5.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off		—	15	—	µA
		Power-off mode	Off	Off	Off	Off	—	—	Power-off 0 Topr = 25°C		—	0.02	0.2	µA
			Off	Off	Off	Off	—	—	Power-off 0 Topr = 85°C		—	0.4	—	µA
			Off	32 kHz	Off	Off	—	—	Power-off 1 Topr = 25°C		—	1.6	3.2	µA
			Off	32 kHz	Off	Off	—	—	Power-off 1 Topr = 85°C		—	2.0	—	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. Vcc = 5.0 V
4. VLCD = Vcc, external division resistors are used for VL4 to VL1, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open. The standard value does not include the current that flows through external division resistors.
5. The internal voltage multiplier is used, bits LVLS3 to LVLS0 in the LCR1 register = 1011b, 1/3 bias, 1/4 duty, f(FR) = 64 Hz, SEG0 to SEG55 are selected, and segment and common output pins are open.

Table 5.22 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Port P10, P11 (1)	I_{OH} = –2 mA	V_{CC} – 0.5	—	V_{CC}	V
		Other pins	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	—	—	V
V_{OL}	Output “L” voltage	Port P10, P11 (1)	I_{OL} = 2 mA	—	—	0.5	V
		Other pins	I_{OL} = 1 mA	—	—	0.5	V
		XOUT	I_{OL} = 200 μA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, INT5, $\overline{INT6}$, INT7, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI5}$, $\overline{KI6}$, $\overline{KI7}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRCTRG, TRCCLK, TRGCLKA, TRGCLKB, $\overline{TRGIOA}$, TRGIOB, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, $\overline{SSO}$		0.05	0.4	—	V
		$\overline{RESET}$, $\overline{WKUP0}$		0.1	0.8	—	V
I_{IH}	Input “H” current		VI = 1.8 V, V_{CC} = 1.8 V	—	—	4.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 1.8 V	—	—	–4.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 1.8 V	60	160	420	kΩ
R_{fXIN}	Feedback resistance	XIN		—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN		—	14	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode	1.8	—	—	V

Note:
1. This applies when the drive capacity of the output transistor is set to High by registers P10DRR and P11DRR. When the drive capacity is set to Low, the value of any other pin applies.

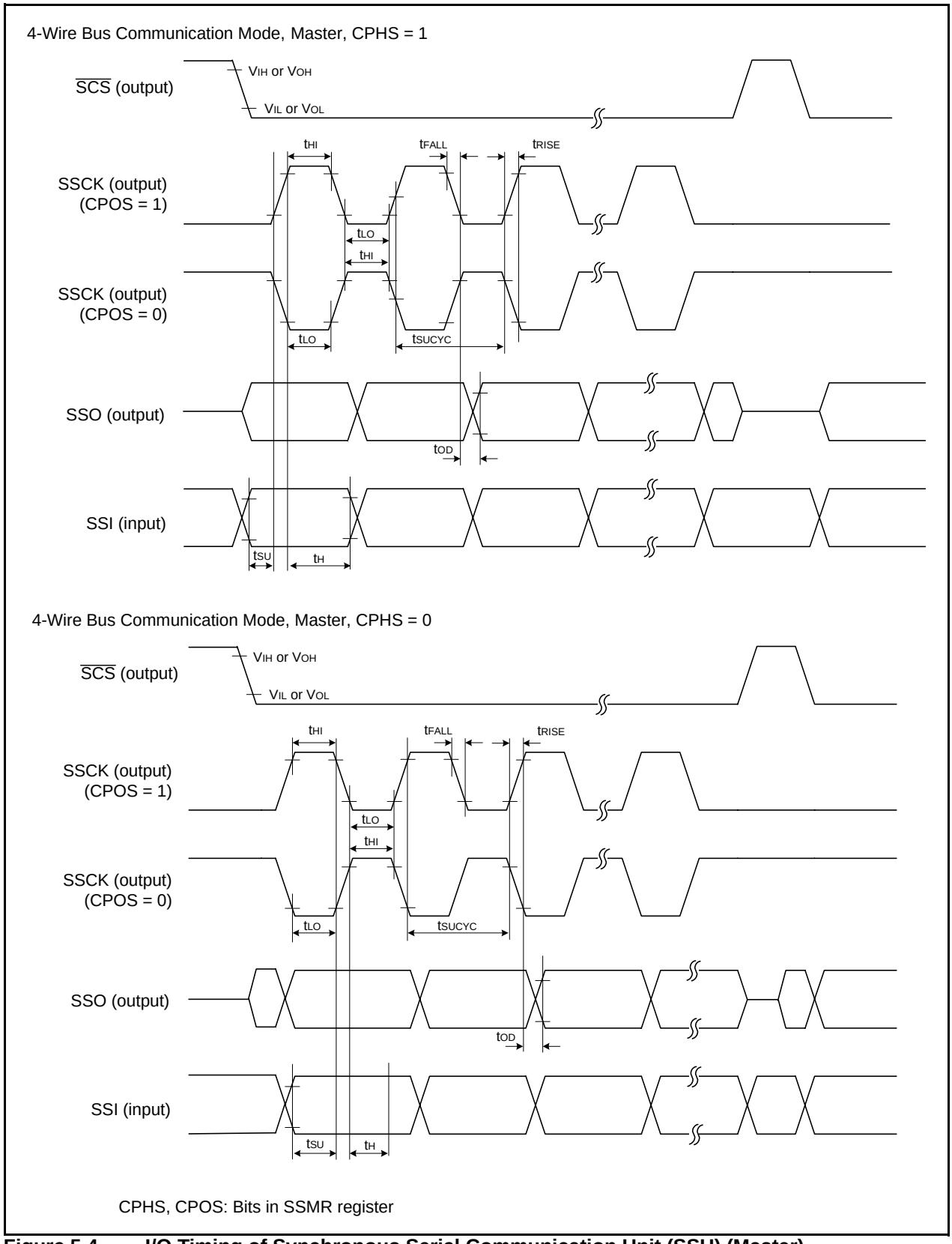


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

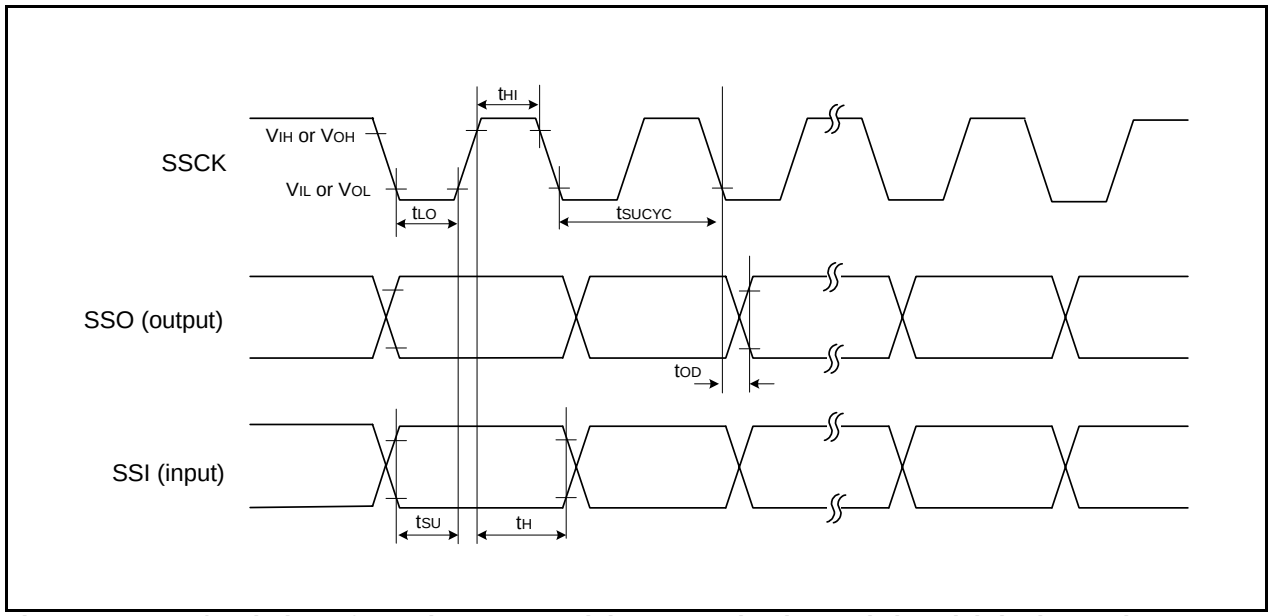
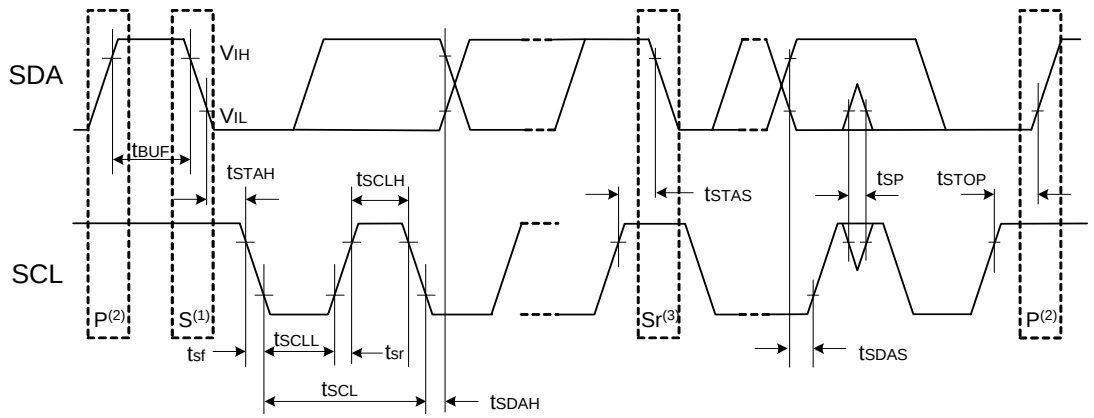


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.25 Timing Requirements of I²C bus Interface (1)
(Vcc = 1.8 to 5.5 V, Vss = 0 V, and Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
tSCL	SCL input cycle time		12tCYC + 600 (1)	—	—	ns
tSCLH	SCL input “H” width		3tCYC + 300 (1)	—	—	ns
tSCLL	SCL input “L” width		5tCYC + 500 (1)	—	—	ns
tsf	SCL, SDA input fall time		—	—	300	ns
tSP	SCL, SDA input spike pulse rejection time		—	—	1tCYC (1)	ns
tBUF	SDA input bus-free time		5tCYC (1)	—	—	ns
tSTAH	Start condition input hold time		3tCYC (1)	—	—	ns
tSTAS	Retransmit start condition input setup time		3tCYC (1)	—	—	ns
tSTOP	Stop condition input setup time		3tCYC (1)	—	—	ns
tSDAS	Data input setup time		1tCYC + 40 (1)	—	—	ns
tSDAH	Data input hold time		10	—	—	ns

Note:
1. 1tCYC = 1/f1(s)



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.7 I/O Timing of I²C bus Interface

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.