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Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-QFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08gt8acfbe

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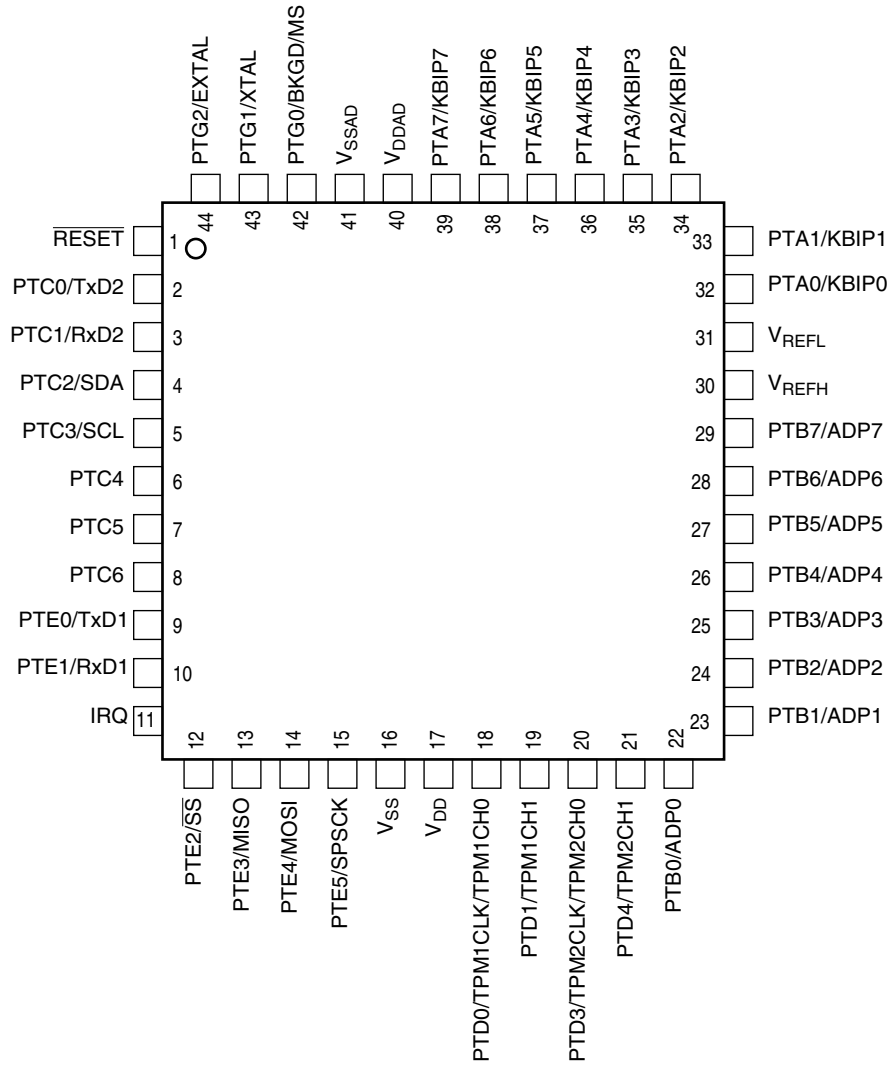


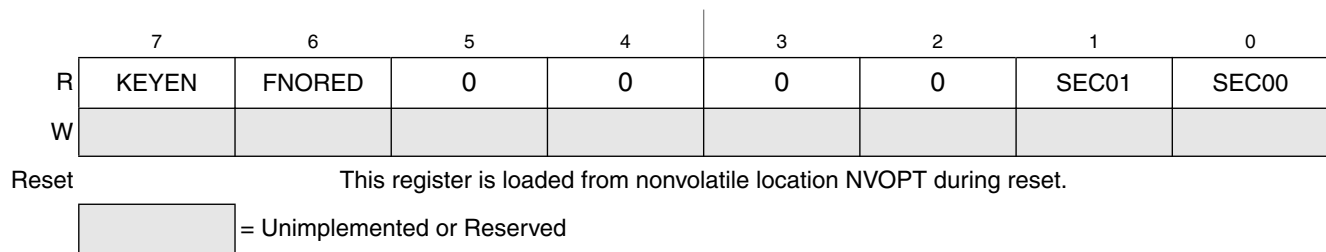
Figure 2-2. MC9S08GT16A/GT8A in 44-Pin QFP Package

Table 4-7. FLASH Clock Divider Settings

f_{Bus}	PRDIV8 (Binary)	DIV5:DIV0 (Decimal)	f_{CLK}	Program/Erase Timing Pulse (5 μ s Min, 6.7 μ s Max)
20 MHz	1	12	192.3 kHz	5.2 μ s
10 MHz	0	49	200 kHz	5 μ s
8 MHz	0	39	200 kHz	5 μ s
4 MHz	0	19	200 kHz	5 μ s
2 MHz	0	9	200 kHz	5 μ s
1 MHz	0	4	200 kHz	5 μ s
200 kHz	0	0	200 kHz	5 μ s
150 kHz	0	0	150 kHz	6.7 μ s

4.6.2 FLASH Options Register (FOPT and NVOPT)

During reset, the contents of the nonvolatile location NVOPT are copied from FLASH into FOPT. Bits 5 through 2 are not used and always read 0. This register may be read at any time, but writes have no meaning or effect. To change the value in this register, erase and reprogram the NVOPT location in FLASH memory as usual and then issue a new MCU reset.


Figure 4-6. FLASH Options Register (FOPT)
Table 4-8. FOPT Field Descriptions

Field	Description
7 KEYEN	<p>Backdoor Key Mechanism Enable — When this bit is 0, the backdoor key mechanism cannot be used to disengage security. The backdoor key mechanism is accessible only from user (secured) firmware. BDM commands cannot be used to write key comparison values that would unlock the backdoor key. For more detailed information about the backdoor key mechanism, refer to Section 4.5, “Security.”</p> <p>0 No backdoor key access allowed.</p> <p>1 If user firmware writes an 8-byte value that matches the nonvolatile backdoor key (NVBACKKEY through NVBACKKEY+7, in that order), security is temporarily disengaged until the next MCU reset.</p>

6.2.3 Port C and SCI2, IIC, and High-Current Drivers

Port C	Bit 7	6	5	3	3	2	1	Bit 0
MCU Pin:	PTC7	PTC6	PTC5	PTC4	PTC3/ SCL	PTC2/ SDA	PTC1/ RxD2	PTC0/ TxD2

Figure 6-4. Port C Pin Names

Port C is an 8-bit port which is shared among the SCI2 and IIC modules, and general-purpose I/O. When SCI2 or IIC modules are enabled, the pin direction will be controlled by the module or function. Port C has high current output drivers.

Port C pins are available as general-purpose I/O pins controlled by the port C data (PTCD), data direction (PTCDD), pullup enable (PTCPE), and slew rate control (PTCSE) registers. Refer to [Section 6.3, “Parallel I/O Controls,”](#) for more information about general-purpose I/O control.

When the SCI2 module is enabled, PTC0 serves as the SCI2 module’s transmit pin (TxD2) and PTC1 serves as the receive pin (RxD2). Refer to [Chapter 11, “Serial Communications Interface \(S08SCIV1\),”](#) for more information about using PTC0 and PTC1 as SCI pins.

When the IIC module is enabled, PTC2 serves as the IIC modules’s serial data input/output pin (SDA) and PTC3 serves as the clock pin (SCL). Refer to [Chapter 13, “Inter-Integrated Circuit \(S08IICV1\),”](#) for more information about using PTC2 and PTC3 as IIC pins.

6.2.4 Port D, TPM1 and TPM2

Port D	Bit 7	6	5	4	3	2	1	Bit 0
MCU Pin:	0	0	0	PTD4/ TPM2CH1	PTD3/ TPM2CLK/ TPM2CH0	PTD2/ TPM1CH2	PTD1/ TPM1CH1	PTD0/ TPM1CLK/ TPM1CH0

Figure 6-5. Port D Pin Names

Port D is an 5-bit port shared with the two TPM modules, TPM1 and TPM2, and general-purpose I/O. When the TPM1 or TPM2 modules are enabled in output compare or input capture modes of operation, the pin direction will be controlled by the module function.

Port D pins are available as general-purpose I/O pins controlled by the port D data (PTDD), data direction (PTDDD), pullup enable (PTDPE), and slew rate control (PTDSE) registers. Refer to [Section 6.3, “Parallel I/O Controls,”](#) for more information about general-purpose I/O control.

The TPM2 module can be configured to use PTD4–PTD3 as either input capture, output compare, PWM, or external clock input pins (PTD3 only). Refer to [Chapter 10, “Timer/PWM \(S08TPMV2\),”](#) for more information about using PTD4–PTD3 as timer pins.

The TPM1 module can be configured to use PTD2–PTD0 as either input capture, output compare, PWM, or external clock input pins (PTD0 only). Refer to [Chapter 10, “Timer/PWM \(S08TPMV2\),”](#) for more information about using PTD2–PTD0 as timer pins.

6.5.5 Port E Registers (PTED, PTEPE, PTESE, and PTEDD)

Port E includes six general-purpose I/O pins that share with the SCI1 and SPI modules. Port E pins used as general-purpose I/O pins are controlled by the port E data (PTED), data direction (PTEDD), pullup enable (PTEPE), and slew rate control (PTESE) registers.

If the SCI1 takes control of a port E pin, the corresponding PTEDD bit is ignored. PTESE can be used to provide slew rate on the SCI1 transmit pin, TxD1. PTEPE can be used, provided the corresponding PTEDD bit is 0, to provide a pullup device on the SCI1 receive pin, RxD1.

If the SPI takes control of a port E pin, the corresponding PTEDD bit is ignored. PTESE can be used to provide slew rate on the SPI serial output pin (MOSI or MISO) and serial clock pin (SPSCK) depending on the SPI operational mode. PTEPE can be used, provided the corresponding PTEDD bit is 0, to provide a pullup device on the SPI serial input pins (MOSI or MISO) and slave select pin (\overline{SS}) depending on the SPI operational mode.

Reads of PTED will return the logic value of the corresponding pin, provided PTEDD is 0.

	7	6	5	4	3	2	1	0
R	0	0	PTED5	PTED4	PTED3	PTED2	PTED1	PTED0
W								
Reset	0	0	0	0	0	0	0	0

Figure 6-24. Port E Data Register (PTED)

Table 6-17. PTED Field Descriptions

Field	Description
5:0 PTED[5:0]	<p>Port E Data Register Bits — For port E pins that are inputs, reads return the logic level on the pin. For port E pins that are configured as outputs, reads return the last value written to this register. Writes are latched into all bits in this register. For port E pins that are configured as outputs, the logic level is driven out the corresponding MCU pin.</p> <p>Reset forces PTED to all 0s, but these 0s are not driven out the corresponding pins because reset also configures all port pins as high-impedance inputs with pullups disabled.</p>

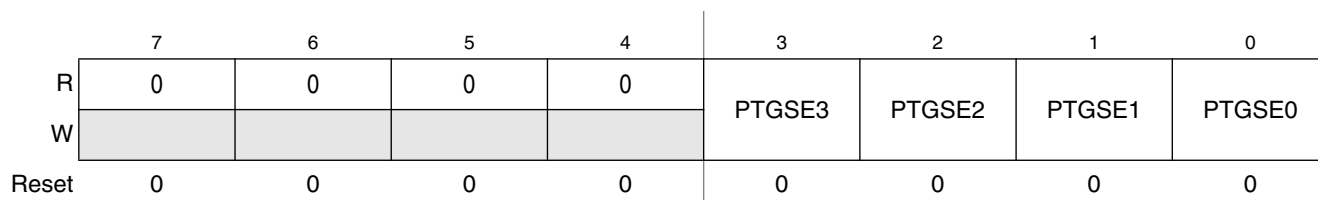


Figure 6-30. Slew Rate Control Enable for Port G (PTGSE)

Table 6-23. PTGSE Field Descriptions

Field	Description
3:0 PTGSE[3:0]	<p>Slew Rate Control Enable for Port G Bits — For port G pins that are outputs, these read/write control bits determine whether the slew rate controlled outputs are enabled. For port G pins that are configured as inputs, these bits are ignored.</p> <p>0 Slew rate control disabled. 1 Slew rate control enabled.</p>

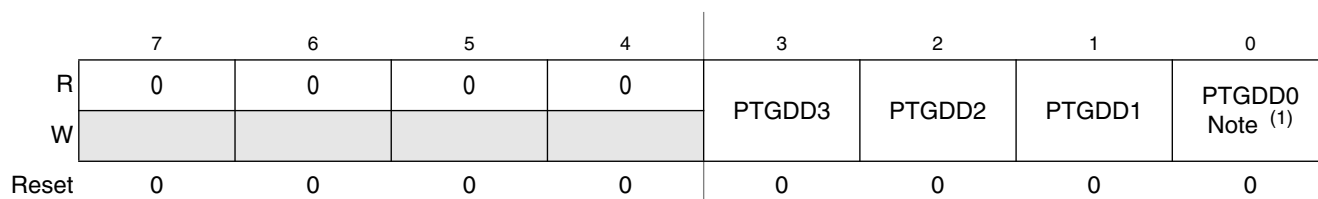


Figure 6-31. Data Direction for Port G (PTGDD)

¹ Although PTGDD0 is implemented, this bit actually has no effect on the operation of PTG0/BKGD.

Table 6-24. PTGDD Field Descriptions

Field	Description
3:0 PTGDD[3:0]	<p>Data Direction for Port G Bits — These read/write bits control the direction of port G pins and what is read for PTGD reads.</p> <p>0 Input (output driver disabled) and reads return the pin value. 1 Output driver enabled for port G bit n and PTGD reads return the contents of PTGDn.</p>

Table 8-2. HCS08 Instruction Set Summary (Sheet 2 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Bus Cycles ¹
			V	H	I	N	Z	C				
BCLR <i>n,opr8a</i>	Clear Bit n in Memory	$M_n \leftarrow 0$	-	-	-	-	-	-	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 dd 13 dd 15 dd 17 dd 19 dd 1B dd 1D dd 1F dd	5 5 5 5 5 5 5 5	
BCS <i>rel</i>	Branch if Carry Bit Set (Same as BLO)	Branch if (C) = 1	-	-	-	-	-	-	REL	25 rr	3	
BEQ <i>rel</i>	Branch if Equal	Branch if (Z) = 1	-	-	-	-	-	-	REL	27 rr	3	
BGE <i>rel</i>	Branch if Greater Than or Equal To (Signed Operands)	Branch if $(N \oplus V) = 0$	-	-	-	-	-	-	REL	90 rr	3	
BGND	Enter Active Background if ENBDM = 1	Waits For and Processes BDM Commands Until GO, TRACE1, or TAGGO	-	-	-	-	-	-	INH	82	5+	
BGT <i>rel</i>	Branch if Greater Than (Signed Operands)	Branch if $(Z) (N \oplus V) = 0$	-	-	-	-	-	-	REL	92 rr	3	
BHCC <i>rel</i>	Branch if Half Carry Bit Clear	Branch if (H) = 0	-	-	-	-	-	-	REL	28 rr	3	
BHCS <i>rel</i>	Branch if Half Carry Bit Set	Branch if (H) = 1	-	-	-	-	-	-	REL	29 rr	3	
BHI <i>rel</i>	Branch if Higher	Branch if $(C) (Z) = 0$	-	-	-	-	-	-	REL	22 rr	3	
BHS <i>rel</i>	Branch if Higher or Same (Same as BCC)	Branch if (C) = 0	-	-	-	-	-	-	REL	24 rr	3	
BIH <i>rel</i>	Branch if IRQ Pin High	Branch if IRQ pin = 1	-	-	-	-	-	-	REL	2F rr	3	
BIL <i>rel</i>	Branch if IRQ Pin Low	Branch if IRQ pin = 0	-	-	-	-	-	-	REL	2E rr	3	
BIT # <i>opr8i</i> BIT <i>opr8a</i> BIT <i>opr16a</i> BIT <i>opr16,X</i> BIT <i>opr8,X</i> BIT <i>,X</i> BIT <i>opr16,SP</i> BIT <i>opr8,SP</i>	Bit Test	(A) & (M) (CCR Updated but Operands Not Changed)	0	-	-	↕	↕	-	IMM DIR EXT IX2 IX1 IX SP2 SP1	A5 ii B5 dd C5 hh ll D5 ee ff E5 ff F5 9ED5 ee ff 9EE5 ff	2 3 4 4 3 3 5 4	
BLE <i>rel</i>	Branch if Less Than or Equal To (Signed Operands)	Branch if $(Z) (N \oplus V) = 1$	-	-	-	-	-	-	REL	93 rr	3	
BLO <i>rel</i>	Branch if Lower (Same as BCS)	Branch if (C) = 1	-	-	-	-	-	-	REL	25 rr	3	
BLS <i>rel</i>	Branch if Lower or Same	Branch if $(C) (Z) = 1$	-	-	-	-	-	-	REL	23 rr	3	
BLT <i>rel</i>	Branch if Less Than (Signed Operands)	Branch if $(N \oplus V) = 1$	-	-	-	-	-	-	REL	91 rr	3	
BMC <i>rel</i>	Branch if Interrupt Mask Clear	Branch if (I) = 0	-	-	-	-	-	-	REL	2C rr	3	
BMI <i>rel</i>	Branch if Minus	Branch if (N) = 1	-	-	-	-	-	-	REL	2B rr	3	
BMS <i>rel</i>	Branch if Interrupt Mask Set	Branch if (I) = 1	-	-	-	-	-	-	REL	2D rr	3	
BNE <i>rel</i>	Branch if Not Equal	Branch if (Z) = 0	-	-	-	-	-	-	REL	26 rr	3	
BPL <i>rel</i>	Branch if Plus	Branch if (N) = 0	-	-	-	-	-	-	REL	2A rr	3	
BRA <i>rel</i>	Branch Always	No Test	-	-	-	-	-	-	REL	20 rr	3	

Chapter 9

Internal Clock Generator (S08ICGV4)

9.1 Introduction

The MC9S08GT16A/GT8A microcontroller provides one internal clock generation (ICG) module to create the system bus frequency. All functions described in this section are available on the MC9S08GT16A/GT8A microcontroller. The EXTAL and XTAL pins share port G bits 2 and 1, respectively. Analog supply lines V_{DDA} and V_{SSA} are internally derived from the MCU's V_{DD} and V_{SS} pins. Electrical parametric data for the ICG may be found in [Appendix A, "Electrical Characteristics."](#)

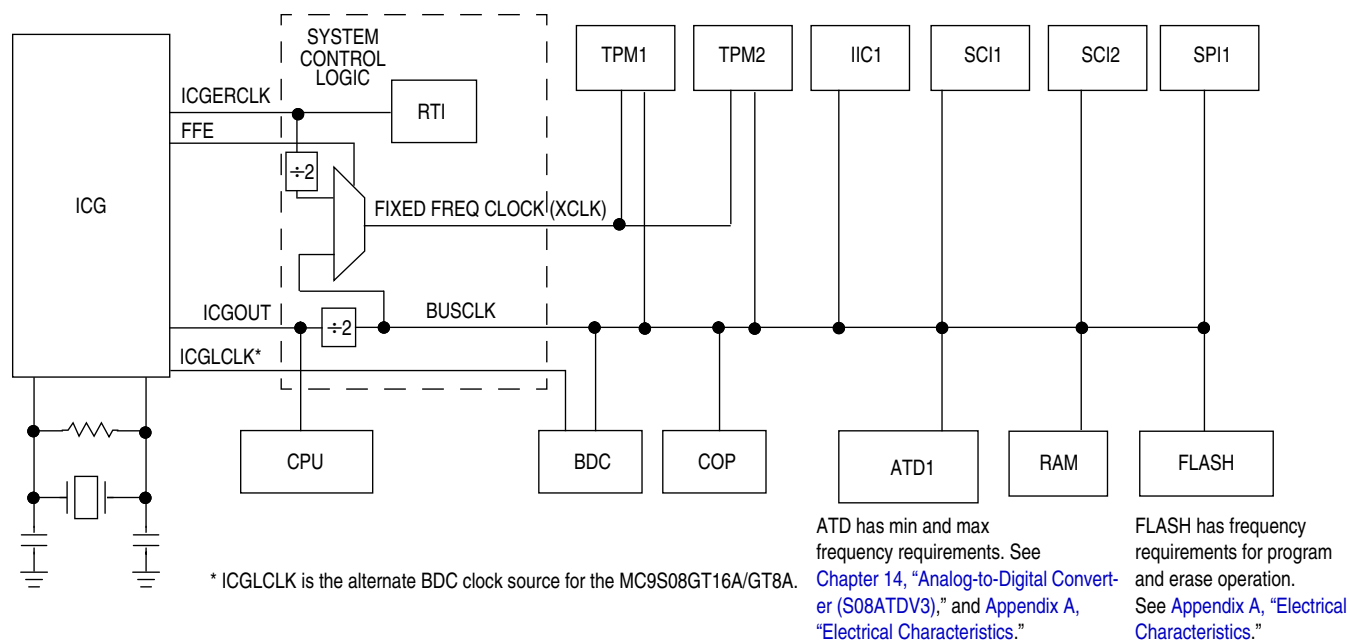


Figure 9-1. System Clock Distribution Diagram

NOTE

Freescale Semiconductor programs a factory trim value for ICGTRM into the FLASH location \$FFBE (NVICGTRM). Leaving this address for the ICGTRM value also allows debugger and programmer vendors to perform a manual trim operation and store the resultant ICGTRM value into NVICGTRM for users to access at a later time. The value in NVICGTRM is not automatically loaded and therefore must be copied into ICGTTRM by user code.

The ICG provides multiple options for clock sources. This offers a user great flexibility when making choices between cost, precision, current draw, and performance. The ICG consists of four functional blocks. Each of these is briefly described here and then in more detail in a later section.

- **Oscillator block** — The oscillator block provides means for connecting an external crystal or resonator. Two frequency ranges are software selectable to allow optimal startup and stability. Alternatively, the oscillator block can be used to route an external square wave to the system clock. External sources can provide a very precise clock source. The oscillator is capable of being configured for low power mode or high amplitude mode as selected by HGO.
- **Internal reference generator** — The internal reference generator consists of two controlled clock sources. One is designed to be approximately 8 MHz and can be selected as a local clock for the background debug controller. The other internal reference clock source is typically 243 kHz and can be trimmed for finer accuracy via software when a precise timed event is input to the MCU. This provides a highly reliable, low-cost clock source.
- **Frequency-locked loop** — A frequency-locked loop (FLL) stage takes either the internal or external clock source and multiplies it to a higher frequency. Status bits provide information when the circuit has achieved lock and when it falls out of lock. Additionally, this block can monitor the external reference clock and signals whether the clock is valid or not.
- **Clock select block** — The clock select block provides several switch options for connecting different clock sources to the system clock tree. ICGDCLK is the multiplied clock frequency out of the FLL, ICGERCLK is the reference clock frequency from the crystal or external clock source, and FFE (fixed frequency enable) is a control signal used to control the system fixed frequency clock (XCLK). ICGLCLK is the clock source for the background debug controller (BDC).

9.1.1 Features

The module is intended to be very user friendly with many of the features occurring automatically without user intervention. To quickly configure the module, go to [Section 9.5, “Initialization/Application Information”](#) and pick an example that best suits the application needs.

Features of the ICG and clock distribution system:

- Several options for the primary clock source allow a wide range of cost, frequency, and precision choices:
 - 32 kHz–100 kHz crystal or resonator
 - 1 MHz–16 MHz crystal or resonator
 - External clock
 - Internal reference generator
- Defaults to self-clocked mode to minimize startup delays
- Frequency-locked loop (FLL) generates 8 MHz to 40 MHz (for bus rates up to 20 MHz)
 - Uses external or internal clock as reference frequency
- Automatic lockout of non-running clock sources
- Reset or interrupt on loss of clock or loss of FLL lock

selected, this pin is not used by the ICG. The oscillator is capable of being configured to provide a higher amplitude output for improved noise immunity. This mode of operation is selected by $HGO = 1$.

9.2.3 External Clock Connections

If an external clock is used, then the pins are connected as shown [Figure 9-4](#).

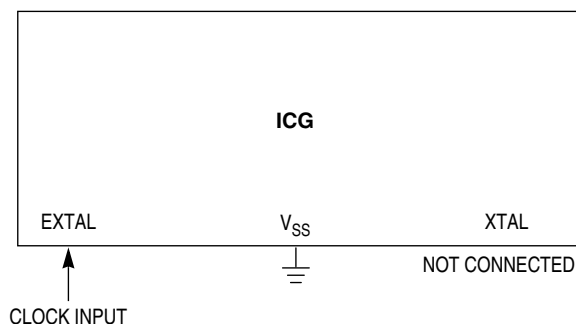


Figure 9-4. External Clock Connections

9.2.4 External Crystal/Resonator Connections

If an external crystal/resonator frequency reference is used, then the pins are connected as shown in [Figure 9-5](#). Recommended component values are listed in the [Electrical Characteristics](#) chapter.

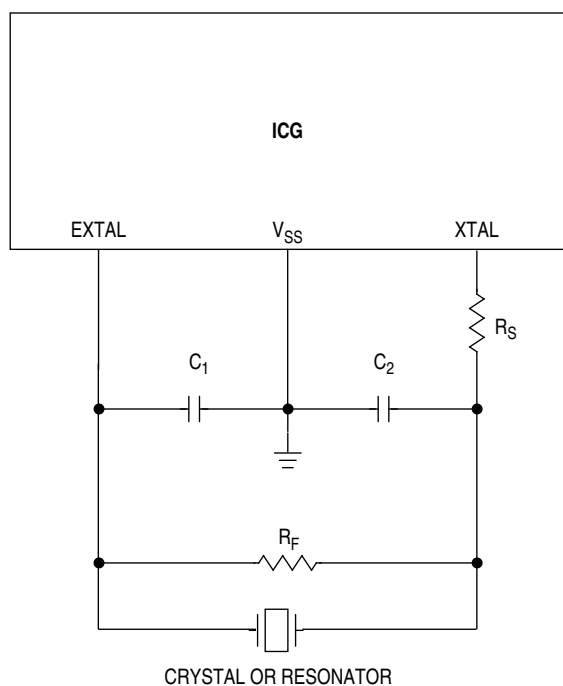


Figure 9-5. External Frequency Reference Connection

9.3.4 ICG Status Register 2 (ICGS2)

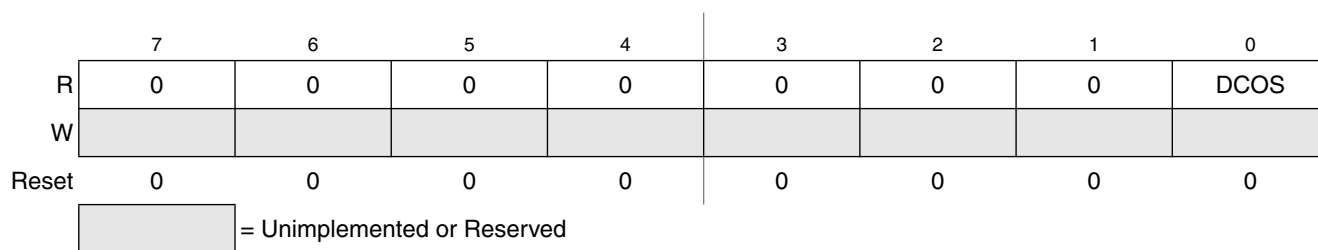


Figure 9-9. ICG Status Register 2 (ICGS2)

Table 9-4. ICGS2 Register Field Descriptions

Field	Description
0 DCOS	<p>DCO Clock Stable — The DCOS bit is set when the DCO clock (ICG2DCLK) is stable, meaning the count error has not changed by more than n_{unlock} for two consecutive samples and the DCO clock is not static. This bit is used when exiting off state if $CLKS = X1$ to determine when to switch to the requested clock mode. It is also used in self-clocked mode to determine when to start monitoring the DCO clock. This bit is cleared upon entering the off state.</p> <p>0 DCO clock is unstable. 1 DCO clock is stable.</p>

9.3.5 ICG Filter Registers (ICGFLTU, ICGFLTL)

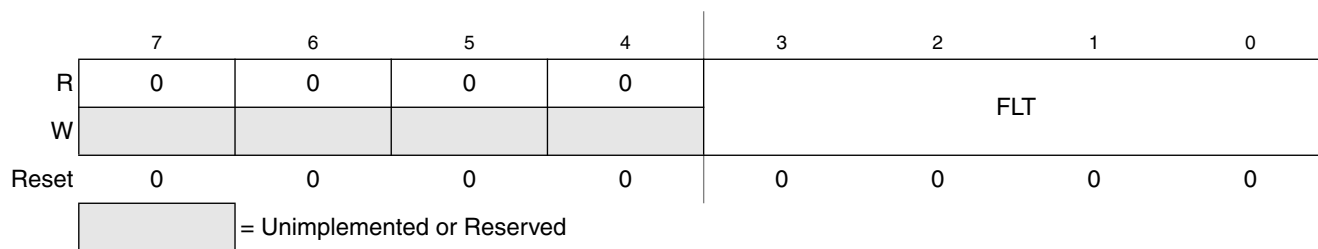


Figure 9-10. ICG Upper Filter Register (ICGFLTU)

Table 9-5. ICGFLTU Register Field Descriptions

Field	Description
3:0 FLT	<p>Filter Value — The FLT bits indicate the current filter value, which controls the DCO frequency. The FLT bits are read only except when the CLKS bits are programmed to self-clocked mode ($CLKS = 00$). In self-clocked mode, any write to ICGFLTU updates the current 12-bit filter value. Writes to the ICGFLTU register will not affect FLT if a previous latch sequence is not complete.</p>

9.4.1 Off Mode (Off)

Normally when the CPU enters stop mode, the ICG will cease all clock activity and is in the off state. However there are two cases to consider when clock activity continues while the CPU is in stop mode,

9.4.1.1 BDM Active

When the BDM is enabled, the ICG continues activity as originally programmed. This allows access to memory and control registers via the BDC controller.

9.4.1.2 OSCSTEN Bit Set

When the oscillator is enabled in stop mode ($OSCSTEN = 1$), the individual clock generators are enabled but the clock feed to the rest of the MCU is turned off. This option is provided to avoid long oscillator startup times if necessary, or to run the RTI from the oscillator during stop3.

9.4.1.3 Stop/Off Mode Recovery

Upon the CPU exiting stop mode due to an interrupt, the previously set control bits are valid and the system clock feed resumes. If FEE is selected, the ICG will source the internal reference until the external clock is stable. If FBE is selected, the ICG will wait for the external clock to stabilize before enabling ICGOUT.

Upon the CPU exiting stop mode due to a reset, the previously set ICG control bits are ignored and the default reset values applied. Therefore the ICG will exit stop in SCM mode configured for an approximately 8 MHz DCO output (4 MHz bus clock) with trim value maintained. If using a crystal, 4096 clocks are detected prior to engaging ICGERCLK. This is incorporated in crystal start-up time.

9.4.2 Self-Clocked Mode (SCM)

Self-clocked mode (SCM) is the default mode of operation and is entered when any of the following conditions occur:

- After any reset.
- Exiting from off mode when $CLKS$ does not equal 10. If $CLKS = X1$, the ICG enters this state temporarily until the DCO is stable ($DCOS = 1$).
- $CLKS$ bits are written from X1 to 00.
- $CLKS = 1X$ and ICGERCLK is not detected (both $ERCS = 0$ and $LOCS = 1$).

In this state, the FLL loop is open. The DCO is on, and the output clock signal ICGOUT frequency is given by $f_{ICGDCLK} / R$. The ICGDCLK frequency can be varied from 8 MHz to 40 MHz by writing a new value into the filter registers (ICGFLTH and ICGFLTL). This is the only mode in which the filter registers can be written.

If this mode is entered due to a reset, $f_{ICGDCLK}$ will default to f_{Self_reset} which is nominally 8 MHz. If this mode is entered from FLL engaged internal, $f_{ICGDCLK}$ will maintain the previous frequency. If this mode is entered from FLL engaged external (either by programming $CLKS$ or due to a loss of external reference clock), $f_{ICGDCLK}$ will maintain the previous frequency, but ICGOUT will double if the FLL was unlocked. If this mode is entered from off mode, $f_{ICGDCLK}$ will be equal to the frequency of ICGDCLK before

of how straight the line is (how far it deviates from a straight line). The adjusted ideal transition voltage is:

Eqn. 14-6

$$\text{Adjusted Ideal Trans. } V = \frac{(\text{Current Code} - 1/2)}{2^N} * ((V_{\text{REFH}} + E_{\text{FS}}) - (V_{\text{REFL}} + E_{\text{ZS}}))$$

- Zero scale error (E_{ZS}) — This is the difference between the transition voltage to the first valid code and the ideal transition to that code. Normally, it is defined as the difference between the actual and ideal transition to code \$001, but in some cases the first transition may be to a higher code. The ideal transition to any code is:

Eqn. 14-7

$$\text{Ideal Transition } V = \frac{(\text{Current Code} - 1/2)}{2^N} * (V_{\text{REFH}} - V_{\text{REFL}})$$

- Full scale error (E_{FS}) — This is the difference between the transition voltage to the last valid code and the ideal transition to that code. Normally, it is defined as the difference between the actual and ideal transition to code \$3FF, but in some cases the last transition may be to a lower code. The ideal transition to any code is:

Eqn. 14-8

$$\text{Ideal Transition } V = \frac{(\text{Current Code} - 1/2)}{2^N} * (V_{\text{REFH}} - V_{\text{REFL}})$$

- Total unadjusted error (E_{TU}) — This is the difference between the transition voltage to a given code and the ideal straight-line transfer function. An alternate definition (with the same result) is the difference between the actual transfer function and the ideal straight-line transfer function. This measure of error includes inherent quantization error and all forms of circuit error (INL, DNL, zero-scale, and full-scale) except input leakage error, which is not due to the ATD.
- Input leakage error (E_{IL}) — This is the error between the transition voltage to the current code and the ideal transition to that code that is the result of input leakage across the real portion of the impedance of the network that drives the analog input. This error is a system-observable error which is not inherent to the ATD, so it is not added to total error. This error is:

$$E_{\text{IL}} \text{ (in V)} = \text{input leakage} * R_{\text{AS}} \quad \text{Eqn. 14-9}$$

There are two other forms of error which are not specified which can also affect ATD accuracy. These are:

- Sampling error (E_{S}) — The error due to inadequate time to charge the ATD circuitry
- Noise error (E_{N}) — The error due to noise on V_{AIN} , V_{REFH} , or V_{REFL} due to either direct coupling (noise source capacitively coupled directly on the signal) or power supply (V_{DDAD} , V_{SSAD} , V_{DD} , and V_{SS}) noise interfering with the ATD's ability to resolve the input accurately. The error due to internal sources can be reduced (and specified operation achieved) by operating the ATD conversion in wait mode and ceasing all IO activity. Reducing the error due to external sources is dependent on system activity and board layout.

Chapter 15

Development Support

15.1 Introduction

Development support systems in the HCS08 include the background debug controller (BDC) and the on-chip debug module (DBG). The BDC provides a single-wire debug interface to the target MCU that provides a convenient interface for programming the on-chip FLASH and other nonvolatile memories. The BDC is also the primary debug interface for development and allows non-intrusive access to memory data and traditional debug features such as CPU register modify, breakpoints, and single instruction trace commands.

In the HCS08 Family, address and data bus signals are not available on external pins (not even in test modes). Debug is done through commands fed into the target MCU via the single-wire background debug interface. The debug module provides a means to selectively trigger and capture bus information so an external development system can reconstruct what happened inside the MCU on a cycle-by-cycle basis without having external access to the address and data signals.

The alternate BDC clock source for MC9S08GT16A/GT8A is the ICGCLK. See the [Chapter 9, “Internal Clock Generator \(S08ICGV4\),”](#) for more information about ICGCLK and how to select clock sources.

the host must perform $((8 - \text{CNT}) - 1)$ dummy reads of the FIFO to advance it to the first significant entry in the FIFO.

In most trigger modes, the information stored in the FIFO consists of 16-bit change-of-flow addresses. In these cases, read DBGFH then DBGFL to get one coherent word of information out of the FIFO. Reading DBGFL (the low-order byte of the FIFO data port) causes the FIFO to shift so the next word of information is available at the FIFO data port. In the event-only trigger modes (see [Section 15.3.5, “Trigger Modes”](#)), 8-bit data information is stored into the FIFO. In these cases, the high-order half of the FIFO (DBGFH) is not used and data is read out of the FIFO by simply reading DBGFL. Each time DBGFL is read, the FIFO is shifted so the next data value is available through the FIFO data port at DBGFL.

In trigger modes where the FIFO is storing change-of-flow addresses, there is a delay between CPU addresses and the input side of the FIFO. Because of this delay, if the trigger event itself is a change-of-flow address or a change-of-flow address appears during the next two bus cycles after a trigger event starts the FIFO, it will not be saved into the FIFO. In the case of an end-trace, if the trigger event is a change-of-flow, it will be saved as the last change-of-flow entry for that debug run.

The FIFO can also be used to generate a profile of executed instruction addresses when the debugger is not armed. When $\text{ARM} = 0$, reading DBGFL causes the address of the most-recently fetched opcode to be saved in the FIFO. To use the profiling feature, a host debugger would read addresses out of the FIFO by reading DBGFH then DBGFL at regular periodic intervals. The first eight values would be discarded because they correspond to the eight DBGFL reads needed to initially fill the FIFO. Additional periodic reads of DBGFH and DBGFL return delayed information about executed instructions so the host debugger can develop a profile of executed instruction addresses.

15.3.3 Change-of-Flow Information

To minimize the amount of information stored in the FIFO, only information related to instructions that cause a change to the normal sequential execution of instructions is stored. With knowledge of the source and object code program stored in the target system, an external debugger system can reconstruct the path of execution through many instructions from the change-of-flow information stored in the FIFO.

For conditional branch instructions where the branch is taken (branch condition was true), the source address is stored (the address of the conditional branch opcode). Because BRA and BRN instructions are not conditional, these events do not cause change-of-flow information to be stored in the FIFO.

Indirect JMP and JSR instructions use the current contents of the H:X index register pair to determine the destination address, so the debug system stores the run-time destination address for any indirect JMP or JSR. For interrupts, RTI, or RTS, the destination address is stored in the FIFO as change-of-flow information.

15.3.4 Tag vs. Force Breakpoints and Triggers

Tagging is a term that refers to identifying an instruction opcode as it is fetched into the instruction queue, but not taking any other action until and unless that instruction is actually executed by the CPU. This distinction is important because any change-of-flow from a jump, branch, subroutine call, or interrupt causes some instructions that have been fetched into the instruction queue to be thrown away without being executed.

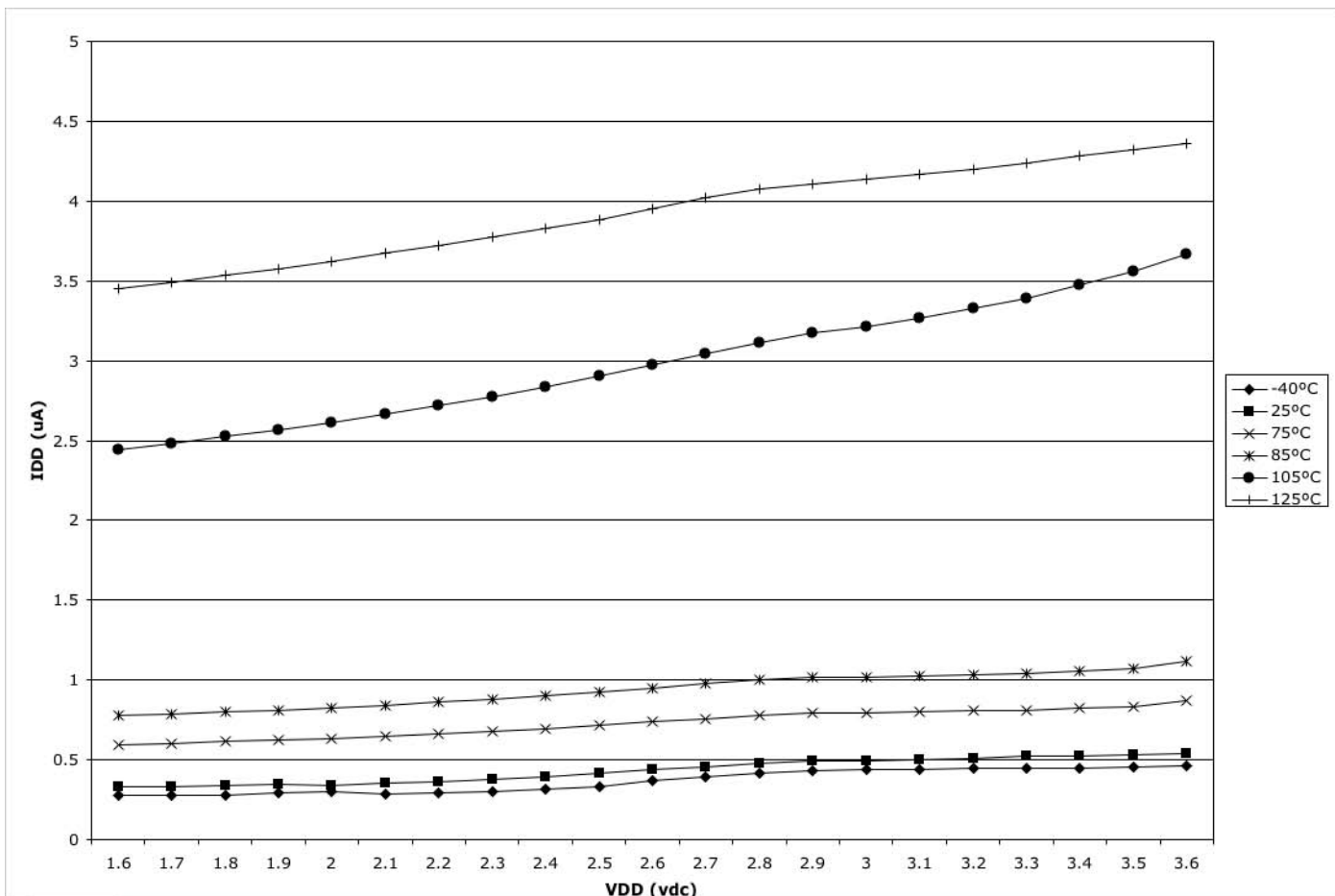
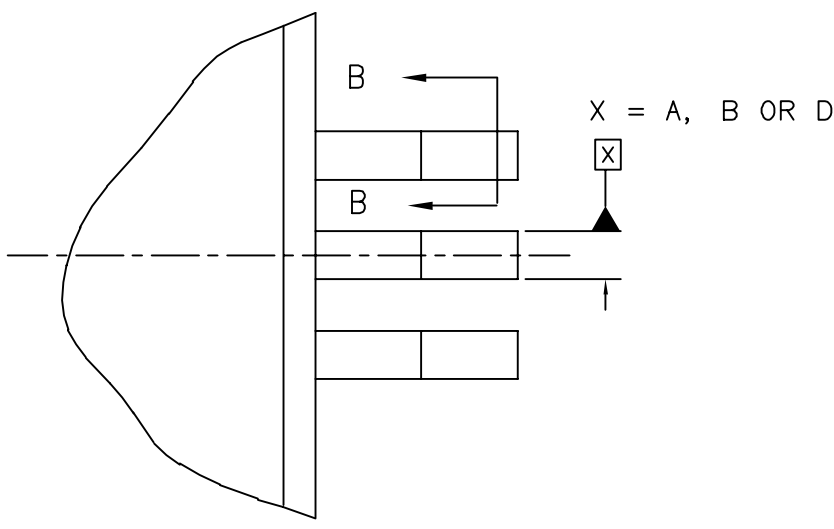
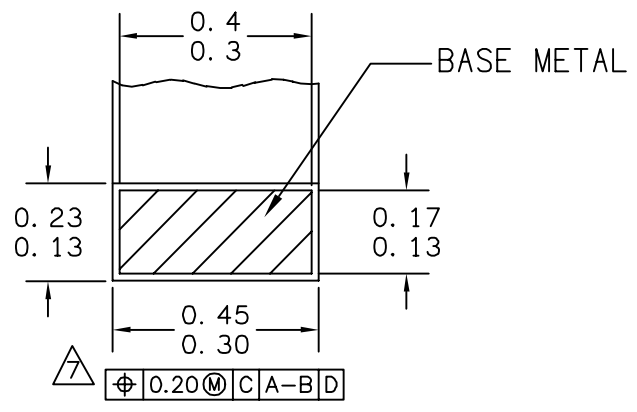


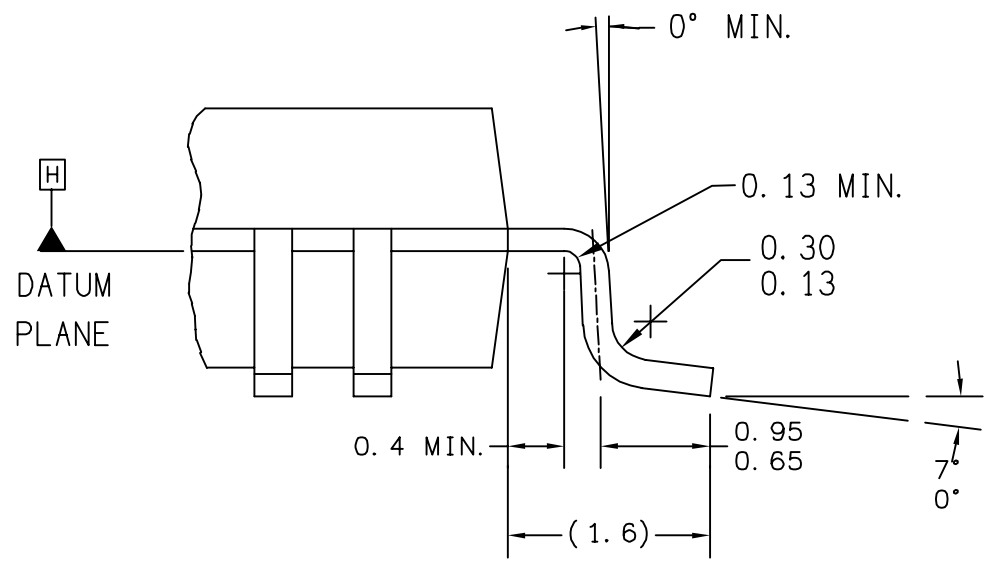
Figure A-8. Typical Stop 2 I_{DD}



DETAIL "A"

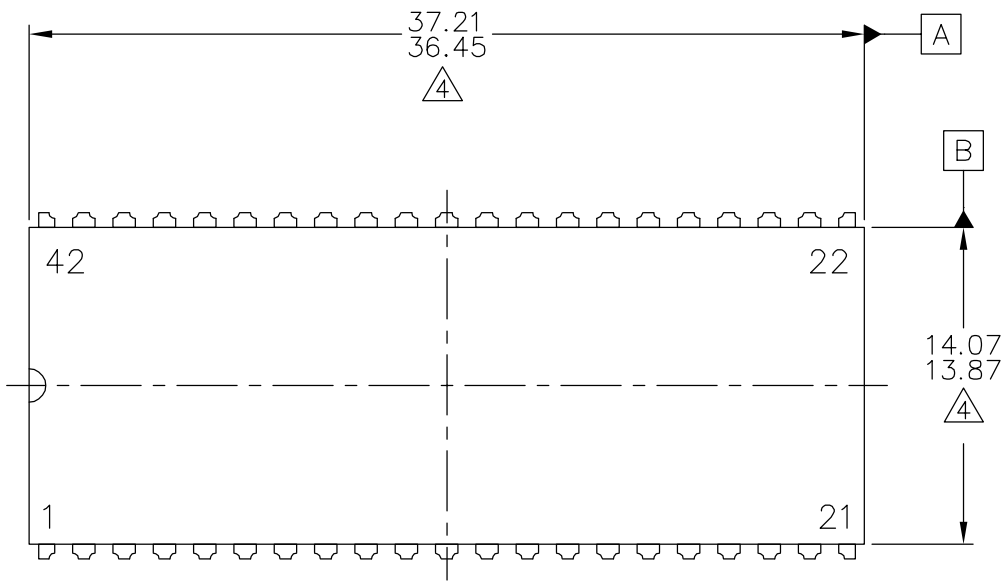


SECTION B-B
VIEW ROTATED 90°

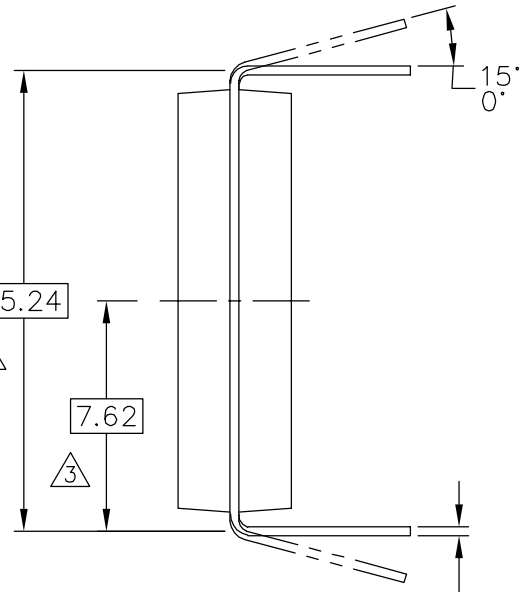


DETAIL "C"

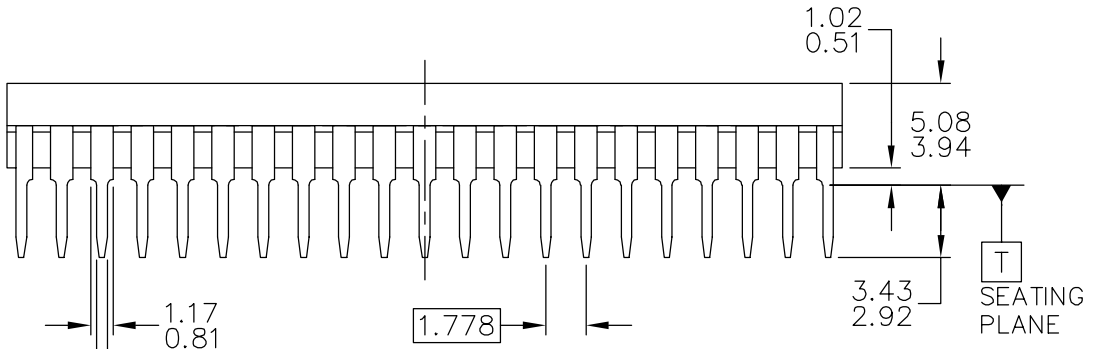
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TITLE: 44LD QFP, 10X10X2.0 PKG, 0.8 PITCH	DOCUMENT NO: 98ASB42839B	REV: B	
	CASE NUMBER: 824A-01	06 APR 2005	
	STANDARD: NON-JEDEC		



TOP VIEW



END VIEW



SIDE VIEW

42X 0.38
0.2
⊕ 0.25 (M) T B (S)

42X 0.56
0.36
⊕ 0.25 (M) T A (S)

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TITLE: 42 LD PDIP	DOCUMENT NO: 98ASB42767B	REV: A	
	CASE NUMBER: 858-01	24 OCT 2005	
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