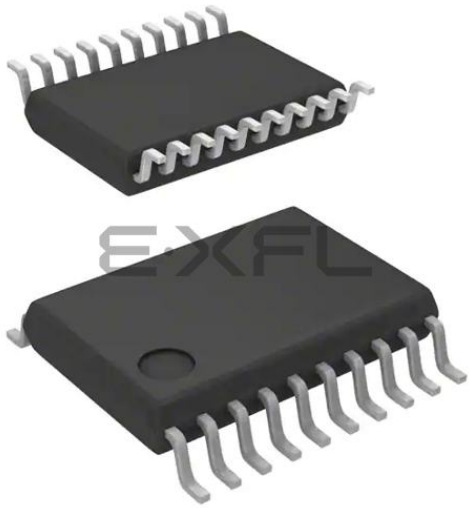

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21142sp-u0

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

Table 1.2 Performance Outline of the R8C/15 Group

Item		Performance
CPU	Number of Basic Instructions	89 instructions
	Minimum Instruction Execution Time	50ns (f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns (f(XIN)=10MHz, VCC=2.7 to 5.5V)
	Operating Mode	Single-chip
	Memory Space	1 Mbyte
	Memory Capacity	See **Table 1.4 R8C/15 Group Product Information**
Peripheral Function	Port	I/O : 13 pins (including LED drive port), Input : 2 pins
	LED drive port	I/O port: 4 pins
	Timer	Timer X: 8 bits × 1 channel, Timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Circuits of input capture and output compare)
	Serial Interface	1 channel Clock synchronous serial I/O, UART
	Chip-select clock synchronous serial I/O (SSU)	1 channel
	A/D Converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog Timer	15 bits × 1 channel (with prescaler) Reset start selectable, Count source protection mode
	Interrupt	Internal: 9 factors, External: 4 factors, Software: 4 factors Priority level: 7 levels
	Clock Generation Circuit	2 circuits • Main clock generation circuit (Equipped with a built-in feedback resistor) • On-chip oscillator (high speed, low speed) Equipped with frequency adjustment function on high-speed on-chip oscillator
	Oscillation Stop Detection Function	Main clock oscillation stop detection function
	Voltage Detection Circuit	Included
	Power on Reset Circuit	Included
Electric Characteristics	Supply Voltage	VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz)
	Power Consumption	Typ. 9mA (VCC=5.0V, f(XIN)=20MHz) Typ. 5mA (VCC=3.0V, f(XIN)=10MHz) Typ. 35μA (VCC=3.0V, wait mode, peripheral clock off) Typ. 0.7μA (VCC=3.0V, stop mode)
Flash Memory	Program/Erase Supply Voltage	VCC=2.7 to 5.5V
	Program/Erase Endurance	10,000 times (Data flash)
		1,000 times (Program ROM)
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D Version)
Package		20-pin plastic mold LSSOP

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

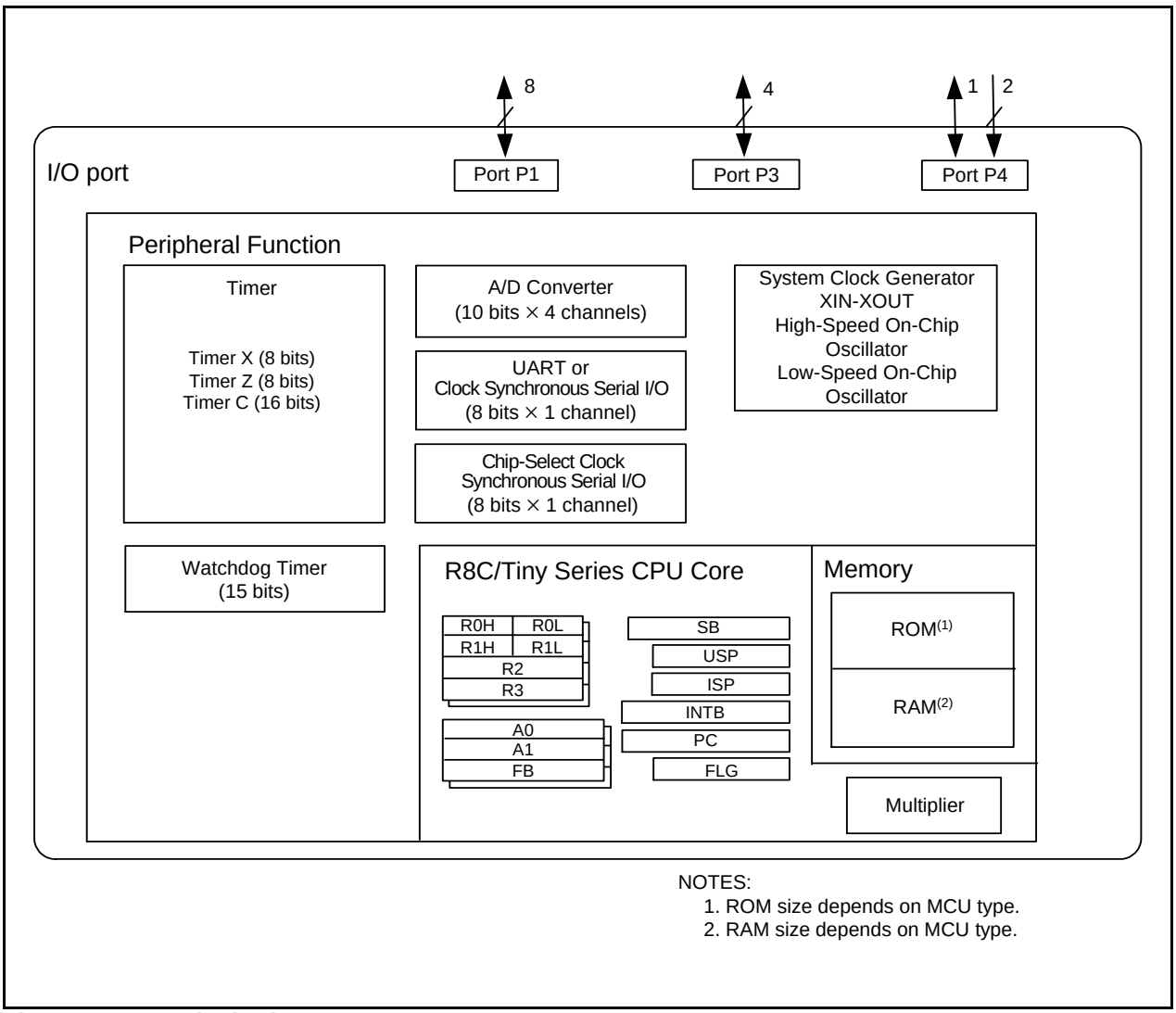

Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists the Product Information of R8C/14 Group and Table 1.4 lists the Product Information of R8C/15 Group.

Table 1.3 Product Information of R8C/14 Group **As of Jan 2006**

Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21142SP	8 Kbytes	512 bytes	PLSP0020JB-A	Flash memory version
R5F21143SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21144SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21142DSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version
R5F21143DSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21144DSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	

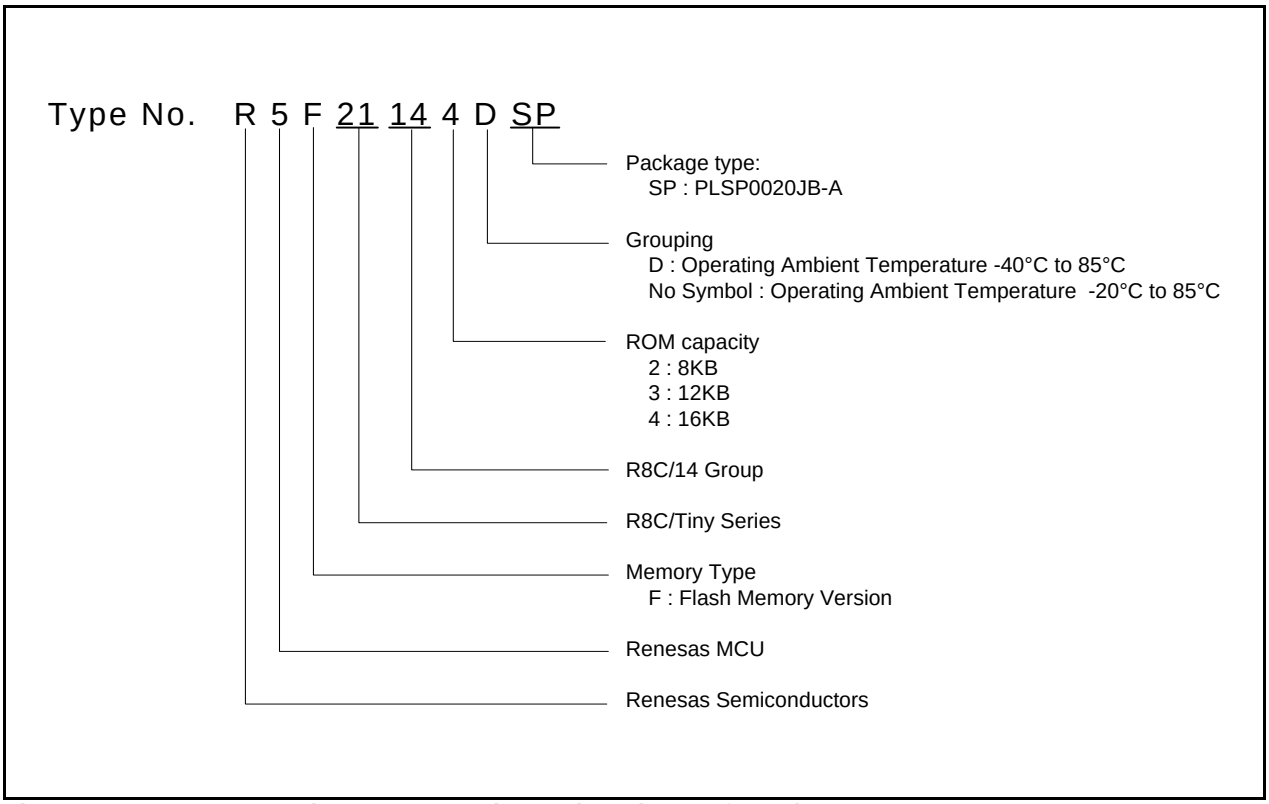

Figure 1.2 Part Number, Memory Size and Package of R8C/14 Group

Table 1.4 Product Information of R8C/15 Group **As of Jan 2006**

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program ROM	Data flash			
R5F21152SP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	Flash memory version
R5F21153SP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21154SP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F21152DSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	D version
R5F21153DSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21154DSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	

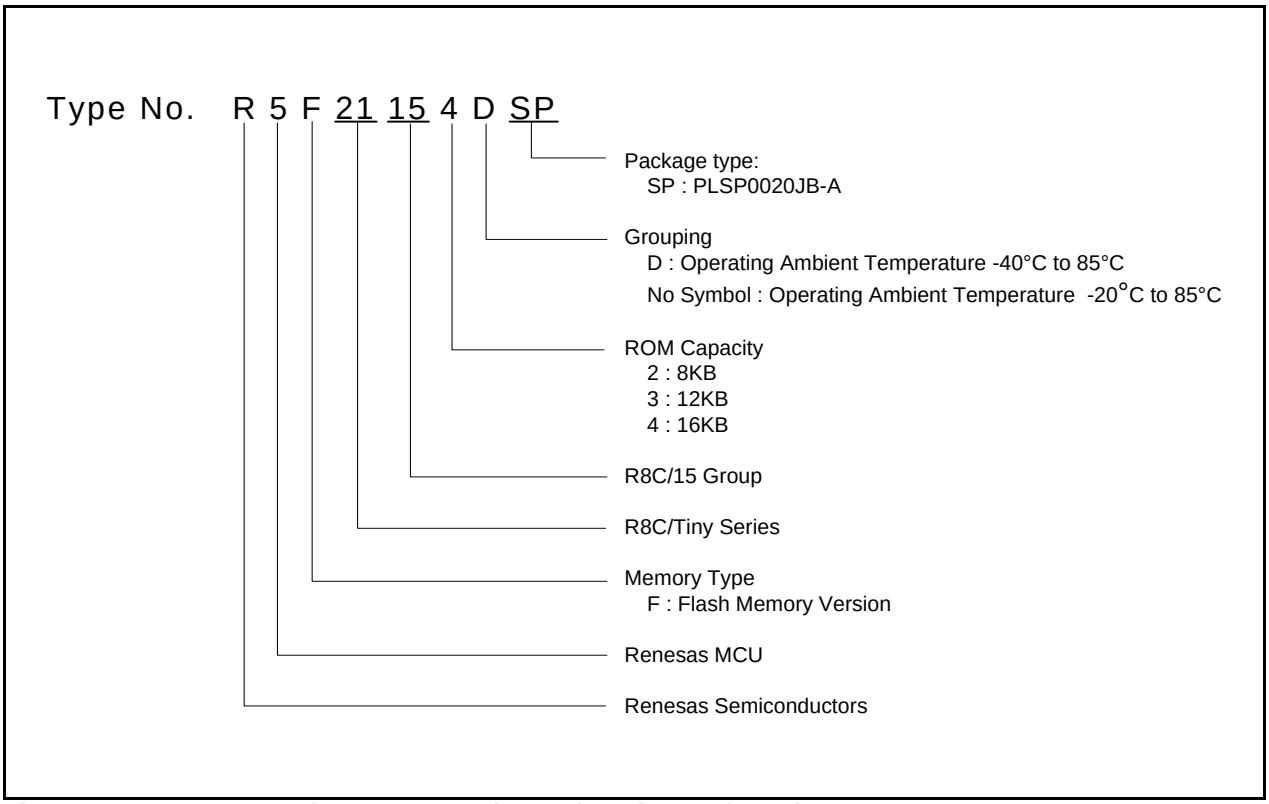

Figure 1.3 Part Number, Memory Size and Package of R8C/15 Group

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin of Peripheral Function				
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	A/D Converter
1		P3_5		CMP1_2		SSCK	
2		P3_7		$\overline{\text{CNTR0}}$		SSO	
3	$\overline{\text{RESET}}$						
4	XOUT	P4_7					
5	VSS/AVSS						
6	XIN	P4_6					
7	VCC						
8	MODE						
9		P4_5	$\overline{\text{INT0}}$				
10		P1_7	$\overline{\text{INT10}}$	CNTR00			
11		P1_6			CLK0		
12		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0		
13		P1_4			TXD0		
14		P1_3	$\overline{\text{KI3}}$	TZOUT			AN11
15		P1_2	$\overline{\text{KI2}}$	CMP0_2			AN10
16	AVCC/VREF						
17		P1_1	$\overline{\text{KI1}}$	CMP0_1			AN9
18		P1_0	$\overline{\text{KI0}}$	CMP0_0			AN8
19		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0		SSI	
20		P3_4		CMP1_1		$\overline{\text{SCS}}$	

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to “0”.

2.8.3 Zero Flag (Z)

The Z flag is set to “1” when an arithmetic operation resulted in 0; otherwise, “0”.

2.8.4 Sign Flag (S)

The S flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, “0”.

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is “0”. The register bank 1 is selected when this flag is set to “1”.

2.8.6 Overflow Flag (O)

The O flag is set to “1” when the operation resulted in an overflow; otherwise, “0”.

2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to “0”, and are enabled when the I flag is set to “1”. The I flag is set to “0” when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is set to “0”, USP is selected when the U flag is set to “1”.
The U flag is set to “0” when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to “0”. When read, its content is indeterminate.

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00000XXXb
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h			
00E1h	Port P1 Register	P1	XXh
00E2h			
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh	Pull-Up Control Register 0	PUR0	00XX0000b
00FDh	Pull-Up Control Register 1	PUR1	XXXXXX0Xb
00FEh	Port P1 Drive Capacity Control Register	DRR	00h
00FFh	Timer C Output Control Register	TCOUT	00h
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
0FFFFh	Optional Function Select Register	OFS	(2)

X: Undefined

NOTES:

1. Blank columns, 0100h to 01B2h and 01B8h to 02FFh are all reserved. No access is allowed.
2. The OFS register cannot be changed by program. Use a flash programmer to write to it.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply Voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog Supply Voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
V_I	Input Voltage		-0.3 to V_{CC}+0.3	V
V_O	Output Voltage		-0.3 to V_{CC}+0.3	V
P_d	Power Dissipation	T_{opr} = 25°C	300	mW
T_{opr}	Operating Ambient Temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage Temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply Voltage			2.7	–	5.5	V
AV_{CC}	Analog Supply Voltage			–	V_{CC}(3)	–	V
V_{SS}	Supply Voltage			–	0	–	V
AV_{SS}	Analog Supply Voltage			–	0	–	V
V_{IH}	Input “H” Voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” Voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak Sum Output “H” Current	Sum of All Pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak Output “H” Current			–	–	-10	mA
$I_{OH(avg)}$	Average Output “H” Current			–	–	-5	mA
$I_{OL(sum)}$	Peak Sum Output “L” Currents	Sum of All Pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak Output “L” Currents	Except P1_0 to P1_3		–	–	10	mA
		P1_0 to P1_3	Drive Capacity HIGH	–	–	30	mA
			Drive Capacity LOW	–	–	10	mA
$I_{OL(avg)}$	Average Output “L” Current	Except P1_0 to P1_3		–	–	5	mA
		P1_0 to P1_3	Drive Capacity HIGH	–	–	15	mA
			Drive Capacity LOW	–	–	5	mA
$f_{(XIN)}$	Main Clock Input Oscillation Frequency		3.0V ≤ V_{CC} ≤ 5.5V	0	–	20	MHz
			2.7V ≤ V_{CC} < 3.0V	0	–	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V_{CC} = AV_{CC}.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/Erase Endurance(2)	R8C/14 Group	100(3)	–	–	times
		R8C/15 Group	1,000(3)	–	–	times
–	Byte Program Time	V_{CC} = 5.0 V at T_{opr} = 25 °C	–	50	400	µs
–	Block Erase Time	V_{CC} = 5.0 V at T_{opr} = 25 °C	–	0.4	9	s
$t_{d(SR-ES)}$	Time Delay from Suspend Request until Erase Suspend		–	–	8	ms
–	Erase Suspend Request Interval		10	–	–	ms
–	Program, Erase Voltage		2.7	–	5.5	V
–	Read Voltage		2.7	–	5.5	V
–	Program, Erase Temperature		0	–	60	°C
–	Data Hold Time(7)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = AVcc = 2.7 to 5.5V at Topr = 0 to 60 °C, unless otherwise specified.
2. Definition of program and erase
   The program and erase endurance shows an erase endurance for every block.
   If the program and erase endurance is “n” times (n = 100, 10000), “n” times erase can be performed for every block.
   For example, if performing 1-byte write to the distinct addresses on Block A of 1Kbyte block 1,024 times and then erasing that block, program and erase endurance is counted as one time.
   However, do not perform multiple programs to the same address for one time ease.(disable overwriting).
3. Endurace to guarantee all electrical characteristics after program and erase.(1 to “Min.” value can be guaranateed).
4. In the case of a system to execute multiple programs, perform one erase after programming as reducing effective reprogram endurance not to leave blank area as possible such as programming write addresses in turn . If programming a set of 16 bytes, programming up to 128 sets and then erasing them one time can reduce effective reprogram endurance. Additionally, averaging erase endurance for Block A and B can reduce effective reprogram endurance more. To leave erase endurance for every block as information and determine the restricted endurance are recommended.
5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
6. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
7. The data hold time incudes time that the power supply is off or the clock is not supplied.

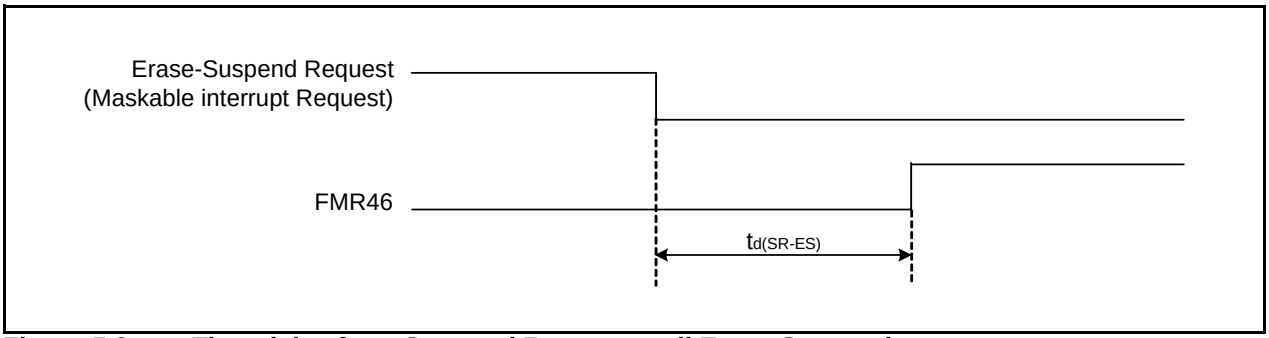

Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage Detection Level(3)		2.70	2.85	3.00	V
–	Voltage Detection Circuit Self Power Consumption	VCA26 = 1, V_{CC} = 5.0V	–	600	–	nA
$t_{d(E-A)}$	Waiting Time until Voltage Detection Circuit Operation Starts(2)		–	–	100	µs
Vccmin	Microcomputer Operating Voltage Minimum Value		2.7	–	–	V

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 2.7V to 5.5V and T_{opr} = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to “1” again after setting the VCA26 bit in the VCA2 register to “0”.
3. Hold $V_{det2} > V_{det1}$.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage Detection Level(4)		3.00	3.30	3.60	V
–	Voltage Monitor 2 Interrupt Request Generation Time(2)		–	40	–	µs
–	Voltage Detection Circuit Self Power Consumption	VCA27 = 1, V_{CC} = 5.0V	–	600	–	nA
$t_{d(E-A)}$	Waiting Time until Voltage Detection Circuit Operation Starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 2.7V to 5.5V and T_{opr} = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated since the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to “1” again after setting the VCA27 bit in the VCA2 register to “0”.
4. Hold $V_{det2} > V_{det1}$.

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-Speed On-Chip Oscillator Frequency When the Reset is Deasserted	V_{CC} = 5.0V, T_{opr} = 25 °C	–	8	–	MHz
–	High-Speed On-Chip Oscillator Frequency Temperature • Supplay Voltage Dependence	0 to +60 °C / 5 V ± 5 %(2)	7.44	–	8.56	MHz
		–20 to +85 °C / 2.7 to 5.5 V(2)	7.04	–	8.96	MHz
		–40 to +85 °C / 2.7 to 5.5 V(2)	6.80	–	9.20	MHz

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 5.0V and T_{opr} = 25 °C.
2. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization during Power-On(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP Exit Time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 2.7 to 5.5V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK Clock Cycle Time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK Clock “H” Width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK Clock “L” Width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK Clock Rising Time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK Clock Falling Time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI Data Input Setup Time			100	–	–	ns
t_{H}	SSO, SSI Data Input Hold Time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ Setup Time	Slave		1t_{CYC}+50	–	–	ns
t_{LAG}	$\overline{SCS}$ Hold Time	Slave		1t_{CYC}+50	–	–	ns
t_{OD}	SSO, SSI Data Output Delay Time			–	–	1	t_{CYC}(2)
t_{SA}	SSI Slave Access Time			–	–	1.5t_{CYC}+100	ns
t_{OR}	SSI Slave Out Open Time			–	–	1.5t_{CYC}+100	ns

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V, V_{SS} = 0V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

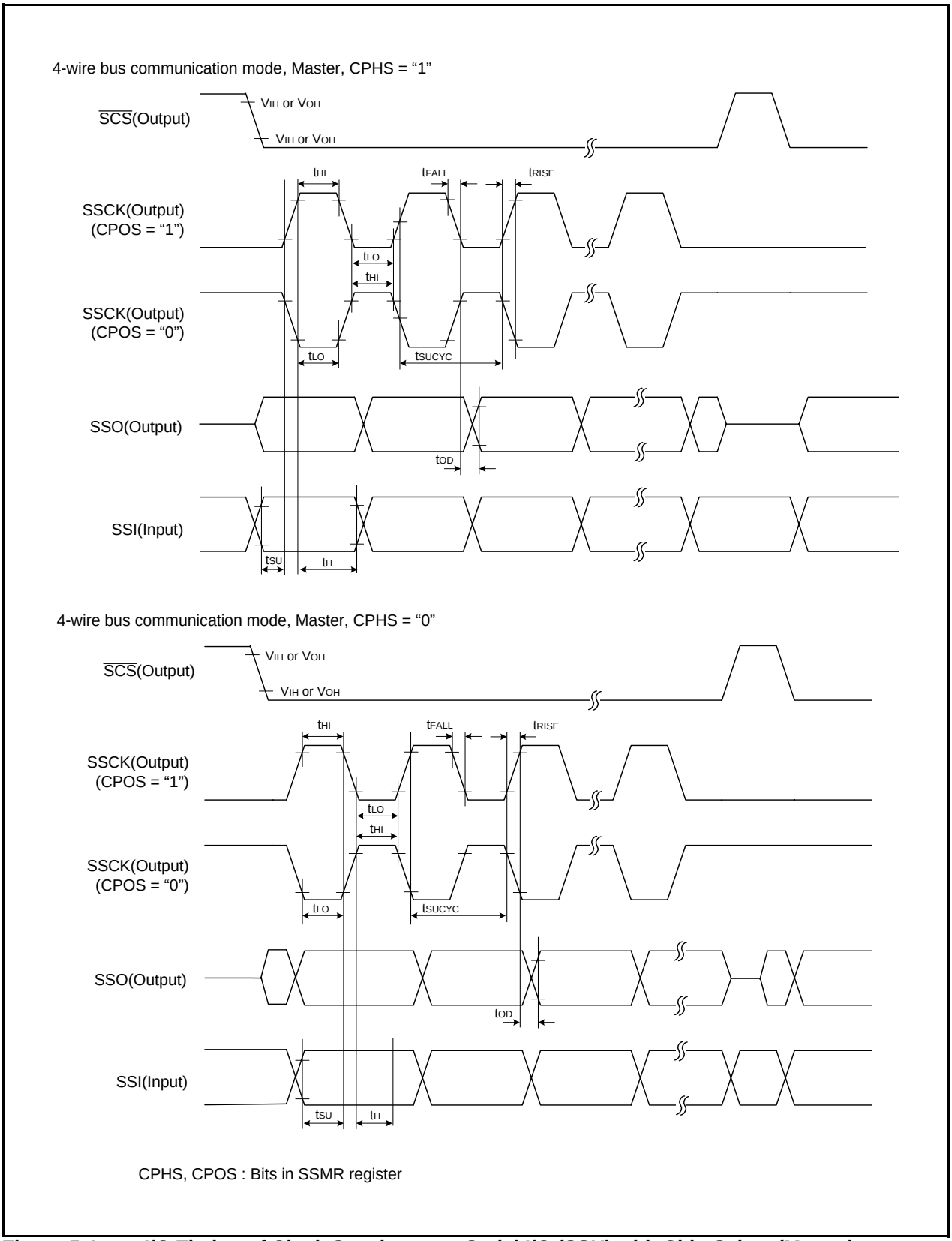

Figure 5.4 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Master)

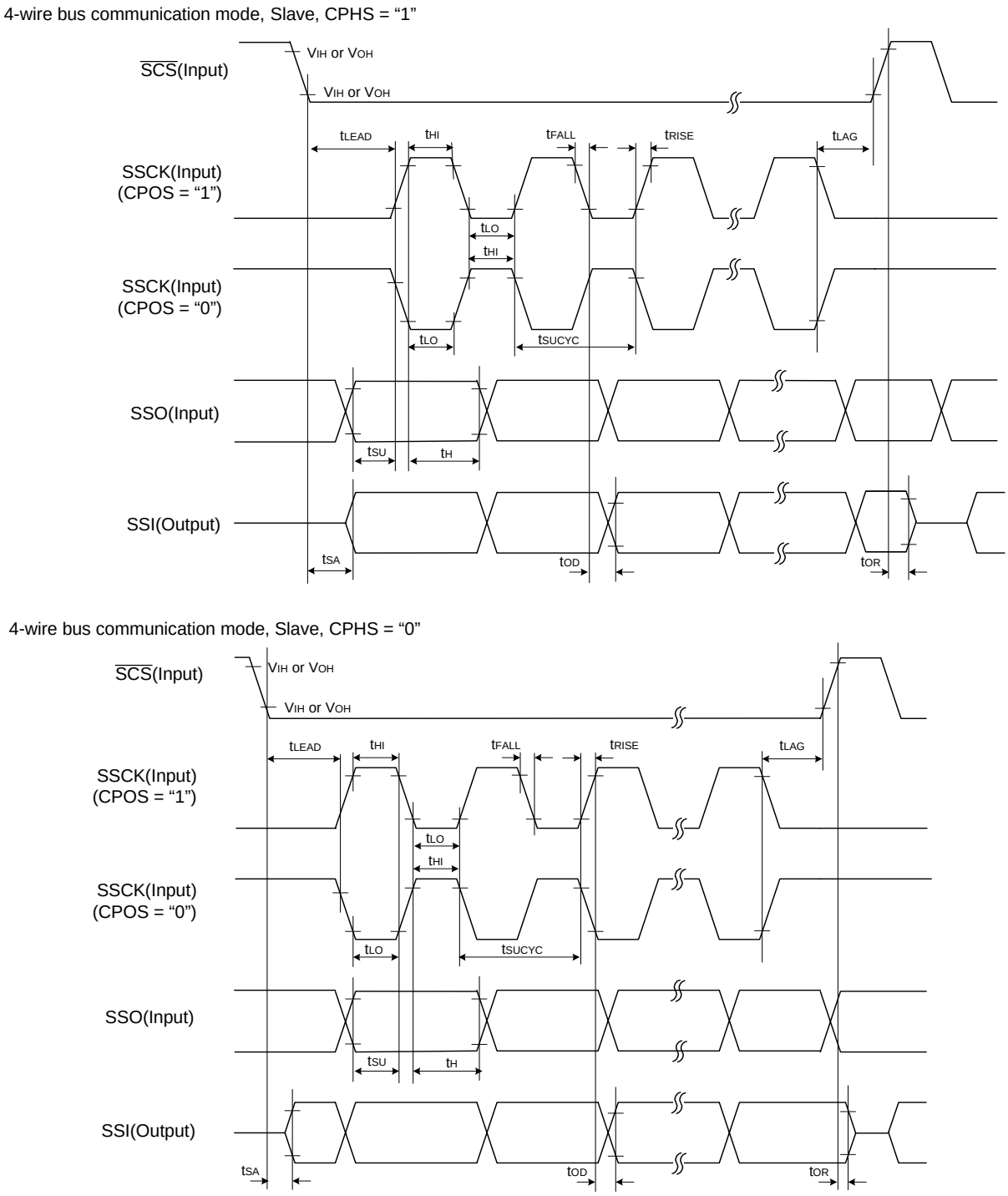

Figure 5.5 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Slave)

Table 5.13 Electrical Characteristics (1) [Vcc = 5V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” Voltage	Except X_{OUT}	I_{OH} = -5mA		V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = -200µA		V_{CC} – 0.3	–	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH} = -1mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -500µA	V_{CC} – 2.0	–	V_{CC}	V
V_{OL}	Output “L” Voltage	Except P1_0 to P1_3, X_{OUT}	I_{OL} = 5mA		–	–	2.0	V
			I_{OL} = 200µA		–	–	0.45	V
		P1_0 to P1_3	Drive capacity HIGH	I_{OL} = 15mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 5mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 200µA	–	–	0.45	V
		X_{OUT}	Drive capacity HIGH	I_{OL} = 1mA	–	–	2.0	V
			Drive capacity LOW	I_{OL} = 500µA	–	–	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RXD0, SSO			0.2	–	1.0	V
		$\overline{RESET}$			0.2	–	2.2	V
I_{IH}	Input “H” current		VI = 5V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0V		–	–	-5.0	µA
R_{PULLUP}	Pull-Up Resistance		VI = 0V		30	50	167	kΩ
R_{fXIN}	Feedback Resistance	XIN			–	1.0	–	MΩ
f_{RING-S}	Low-Speed On-Chip Oscillator Frequency				40	125	250	kHz
V_{RAM}	RAM Hold Voltage		During stop mode		2.0	–	–	V

NOTES:
1. V_{CC} = AV_{CC} = 4.2 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(XIN)=20MHz, unless otherwise specified.

Table 5.14 Electrical Characteristics (2) [Vcc = 5V] (Topr = -40 to 85 °C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power Supply Current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	9	15	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	8	14	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	5	–	mA
		Medium-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	4	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	3	–	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	2	–	mA
		High-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division	–	4	8	mA
			Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8	–	1.5	–	mA
		Low-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	470	900	µA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0	–	40	80	µA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0	–	38	76	µA
		Stop Mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	µA

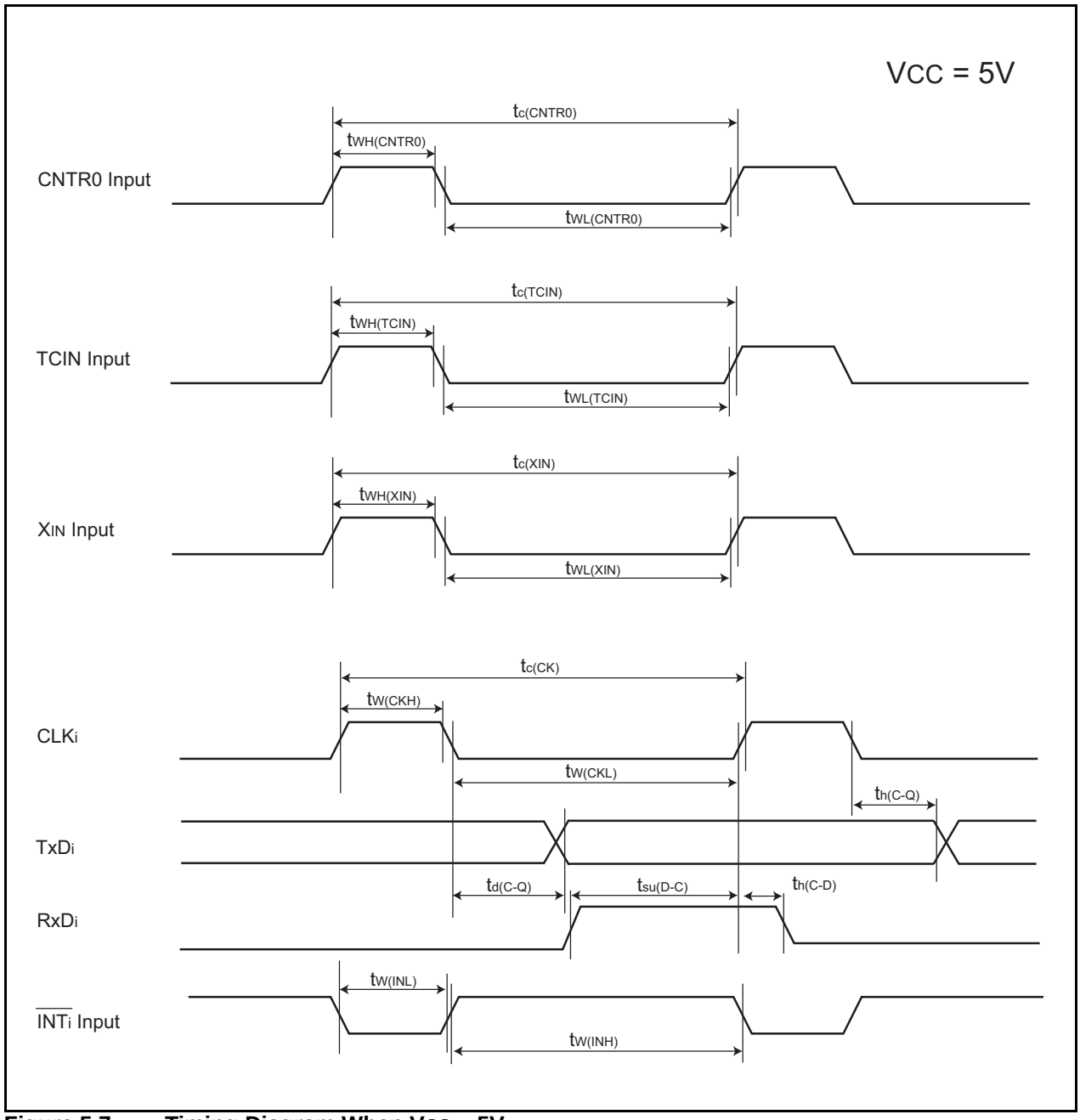

Figure 5.7 Timing Diagram When Vcc = 5V

Table 5.20 Electrical Characteristics (3) [Vcc = 3V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” Voltage	Except X_{OUT}	I_{OH} = -1mA		V_{CC} – 0.5	–	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH} = -0.1mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -50µA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” Voltage	Except P1_0 to P1_3, X_{OUT}	I_{OL} = 1mA		–	–	0.5	V
		P1_0 to P1_3	Drive capacity HIGH	I_{OL} = 2mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1mA	–	–	0.5	V
		X_{OUT}	Drive capacity HIGH	I_{OL} = 0.1mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RXD0, SSO			0.2	–	0.8	V
		$\overline{RESET}$			0.2	–	1.8	V
I_{IH}	Input “H” Current		VI = 3V		–	–	4.0	µA
I_{IL}	Input “L” Current		VI = 0V		–	–	-4.0	µA
R_{PULLUP}	Pull-Up Resistance		VI = 0V		66	160	500	kΩ
R_{fXIN}	Feedback Resistance	XIN			–	3.0	–	MΩ
f_{RING-S}	Low-Speed On-Chip Oscillator Frequency				40	125	250	kHz
V_{RAM}	RAM Hold Voltage		During stop mode		2.0	–	–	V

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 3.3V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(XIN)=10MHz, unless otherwise specified.

REVISION HISTORY	R8C/14 Group, R8C/15 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Jan 30, 2006	8	Figure 1.5 PRDP0020BA-A Package Pin Assignment (top view) deleted Table 1.5 Pin Description; Timer C: "CMP0_0 to CMP0_3, CMP1_0 to CMP1_3" → "CMP0_0 to CMP0_2, CMP1_0 to CMP1_2" revised
		10	Figure 2.1 CPU Register; "Reserved Area" → "Reserved Bit" revised
		12	2.8.10 Reserved Area; "Reserved Area" → "Reserved Bit" revised
		13	Figure 3.1 Memory Map of R8C/14 Group revised
		14	3.2 R8C/15 Group; "(data area)" → "(data flash)", "(program area)" → "(program ROM)" revised Figure 3.2 Memory Map of R8C/15 Group revised
		15	Table 4.1 SFR Information(1); 0009h: "XXXXXX00b" → "00h" 000Ah: "00XXX000b" → "00h" 001Eh: "XXXXX000b" → "00h"
		17	Table 4.3 SFR Information(3); 0085h: "Prescaler Z" → "Prescaler Z Register" 0086h: "Timer Z Secondary" → "Timer Z Secondary Register" 0087h: "Timer Z Primary" → "Timer Z Primary Register" 008Ch: "Prescaler X" → "Prescaler X Register" 008Dh: "Timer X" → "Timer X Register" 0090h, 0091h: "Timer C" → "Timer C Register" revised
		21	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; • NOTES 1 to 7 added • "Topr" → "Ambient temperature", "Program area" → "Program ROM" revised
		22	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; • NOTE1 revised, NOTE9 added • "Topr" → "Ambient temperature", "Data area" → "Data flash" revised
		23	Figure 5.2 Time delay from Suspend Request until Erase Suspend revised
		24	Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset); NOTE2 revised Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset); NOTE1 revised
		25	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; revised Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select; revised
		30	Table 5.14 Electrical Characteristics (2) [Vcc = 5V]; revised
		31	"Timing Requirements (Unless ... at Ta = 25°C) [VCC = 5V]" → "Timing Requirements (Unless ... at Topr = 25°C) [VCC = 5V]" revised Table 5.18 Serial Interface; "35" → "50", "80" → "50"
		34	Table 5.21 Electrical Characteristics (4) [Vcc = 3V]; revised
		35	"Timing requirements (Unless ... at Ta = 25°C) [VCC = 3V]" → "Timing requirements (Unless ... at Topr = 25°C) [VCC = 3V]" revised Table 5.25 Serial Interface; "55" → "70", "160" → "80"
		37	Package Dimensions; Package "PRDP0020BA-A" deleted