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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21142sp-w4

1.2 Performance Overview

Table 1.1 lists the Performance Outline of the R8C/14 Group and Table 1.2 lists the Performance Outline of the R8C/15 Group.

Table 1.1 Performance Outline of the R8C/14 Group

Item		Performance
CPU	Number of Basic Instructions	89 instructions
	Minimum Instruction Execution Time	50ns(f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns(f(XIN)=10MHz, VCC=2.7 to 5.5V)
	Operating Mode	Single-chip
	Memory Space	1 Mbyte
	Memory Capacity	See Table 1.3 R8C/14 Group Product Information
Peripheral Function	Port	I/O port : 13 pins (including LED drive port), Input : 2 pins
	LED Drive Port	I/O port: 4 pins
	Timer	Timer X: 8 bits × 1 channel, Timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Circuits of input capture and output compare)
	Serial Interface	1 channel Clock synchronous serial I/O, UART
	Chip-Select Clock Synchronous Serial I/O (SSU)	1 channel
	A/D Converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog Timer	15 bits × 1 channel (with prescaler) Reset start selectable, Count source protection mode
	Interrupt	Internal: 9 factors, External: 4 factors, Software: 4 factors, Priority level: 7 levels
	Clock Generation Circuit	2 circuits • Main clock oscillation circuit (Equipped with a built-in feedback resistor) • On-chip oscillator (high speed, low speed) Equipped with frequency adjustment function on high-speed on-chip oscillator
	Oscillation Stop Detection Function	Main clock oscillation stop detection function
	Voltage Detection Circuit	Included
	Power-On Reset Circuit	Included
Electric Characteristics	Supply Voltage	VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz)
	Power Consumption	Typ. 9mA (VCC=5.0V, f(XIN)=20MHz) Typ. 5mA (VCC=3.0V, f(XIN)=10MHz) Typ. 35μA (VCC=3.0V, wait mode, peripheral clock off) Typ. 0.7μA (VCC=3.0V, stop mode)
Flash Memory	Program/Erase Supply Voltage	VCC=2.7 to 5.5V
	Program/Erase Endurance	100 times
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D Version)
Package		20-pin plastic mold LSSOP

1.4 Product Information

Table 1.3 lists the Product Information of R8C/14 Group and Table 1.4 lists the Product Information of R8C/15 Group.

Table 1.3 Product Information of R8C/14 Group

As of Jan 2006

Type No.	ROM capacity	RAM capacity	Package type	Remarks
R5F21142SP	8 Kbytes	512 bytes	PLSP0020JB-A	Flash memory version
R5F21143SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21144SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21142DSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version
R5F21143DSP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21144DSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	

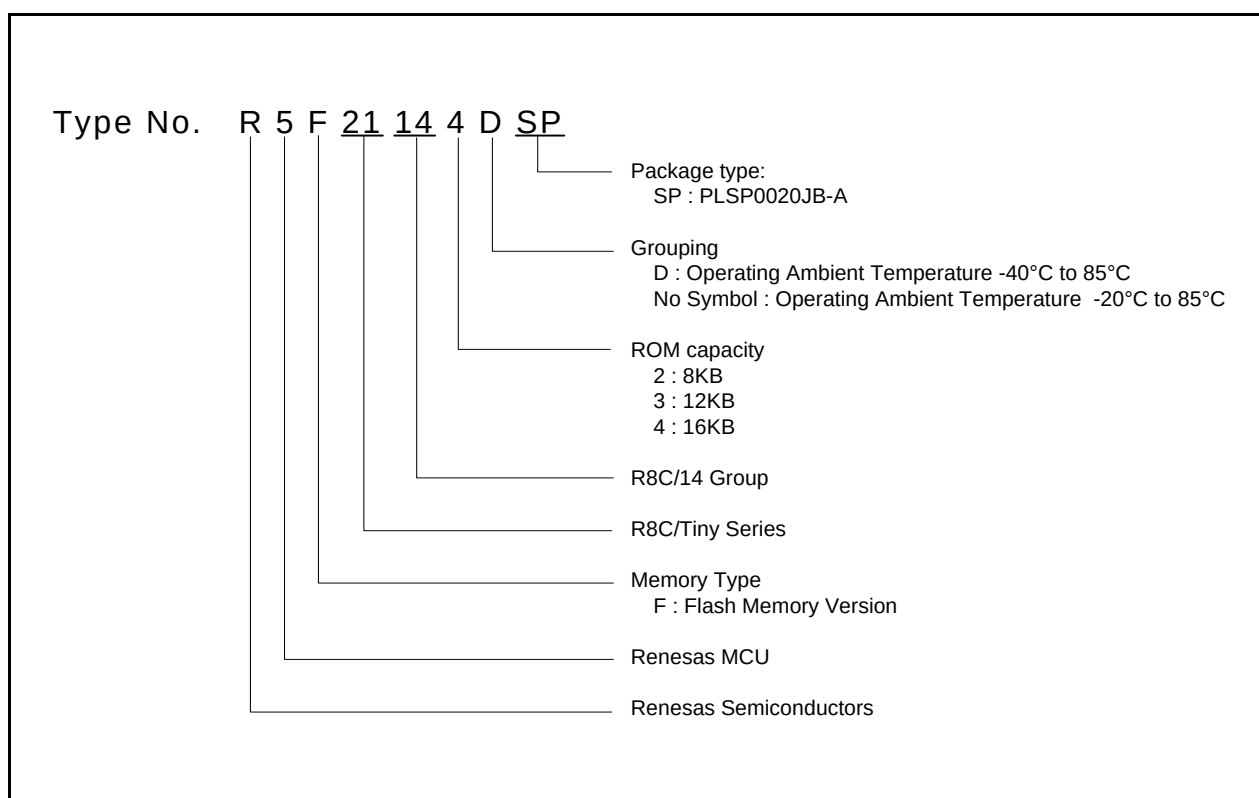


Figure 1.2 Part Number, Memory Size and Package of R8C/14 Group

1.5 Pin Assignments

Figure 1.4 shows the PLSP0020JB-A Package Pin Assignment (top view).

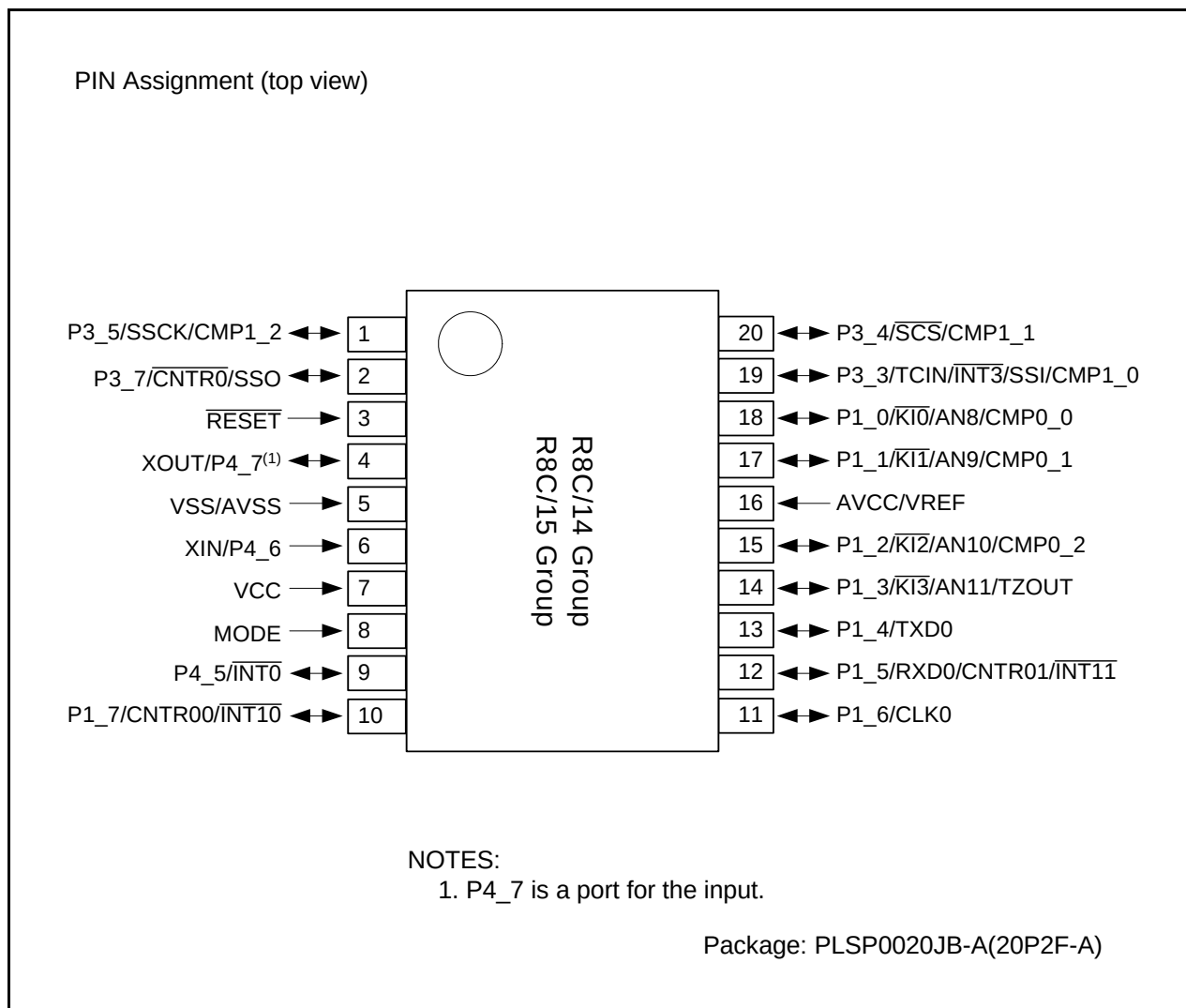


Figure 1.4 PLSP0020JB-A Package Pin Assignment (top view)

1.6 Pin Description

Table 1.5 lists the Pin Description and Table 1.6 lists the Pin Name Information by Pin Number.

Table 1.5 Pin Description

Function	Pin name	I/O type	Description
Power Supply Input	VCC VSS	I	Apply 2.7V to 5.5V to the VCC pin. Apply 0V to the VSS pin
Analog Power Supply Input	AVCC AVSS	I	Power supply input pins to A/D converter. Connect AVCC to VCC. Apply 0V to AVSS. Connect a capacitor between AVCC and AVSS.
Reset Input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU
MODE	MODE	I	Connect this pin to VCC via a resistor
Main Clock Input	XIN	I	These pins are provided for the main clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open.
Main Clock Output	XOUT	O	
$\overline{\text{INT}}$ Interrupt	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	INT interrupt input pins
Key Input Interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer X	CNTR0	I/O	Timer X I/O pin
	$\overline{\text{CNTR0}}$	O	Timer X output pin.
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
	CMP0_0 to CMP0_2, CMP1_0 to CMP1_2	O	Timer C output pins.
Serial Interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0	I	Serial data input pin.
	TXD0	O	Serial data output pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
Reference Voltage Input	VREF	I	Reference voltage input pin to A/D converter Connect VREF to VCC
A/D Converter	AN8 to AN11	I	Analog input pins to A/D converter
I/O Port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	These are CMOS I/O ports. Each port contains an I/O select direction register, allowing each pin in that port to be directed for input or output individually. Any port set to input can select whether to use a pull-up resistor or not by program. P1_0 to P1_3 also function as LED drive ports.
Input Port	P4_6, P4_7	I	Port for input-only

I: Input O: Output I/O: Input and output

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin of Peripheral Function				
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	A/D Converter
1		P3_5		CMP1_2		SSCK	
2		P3_7		CNTR0		SSO	
3	RESET						
4	XOUT	P4_7					
5	VSS/AVSS						
6	XIN	P4_6					
7	VCC						
8	MODE						
9		P4_5	INT0				
10		P1_7	INT10	CNTR00			
11		P1_6			CLK0		
12		P1_5	INT11	CNTR01	RXD0		
13		P1_4			TXD0		
14		P1_3	KI3	TZOUT			AN11
15		P1_2	KI2	CMP0_2			AN10
16	AVCC/VREF						
17		P1_1	KI1	CMP0_1			AN9
18		P1_0	KI0	CMP0_0			AN8
19		P3_3	INT3	TCIN/CMP1_0		SSI	
20		P3_4		CMP1_1		SCS	

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

3.2 R8C/15 Group

Figure 3.2 is a Memory Map of R8C/15 Group. The R8C/15 group provides 1-Mbyte address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.

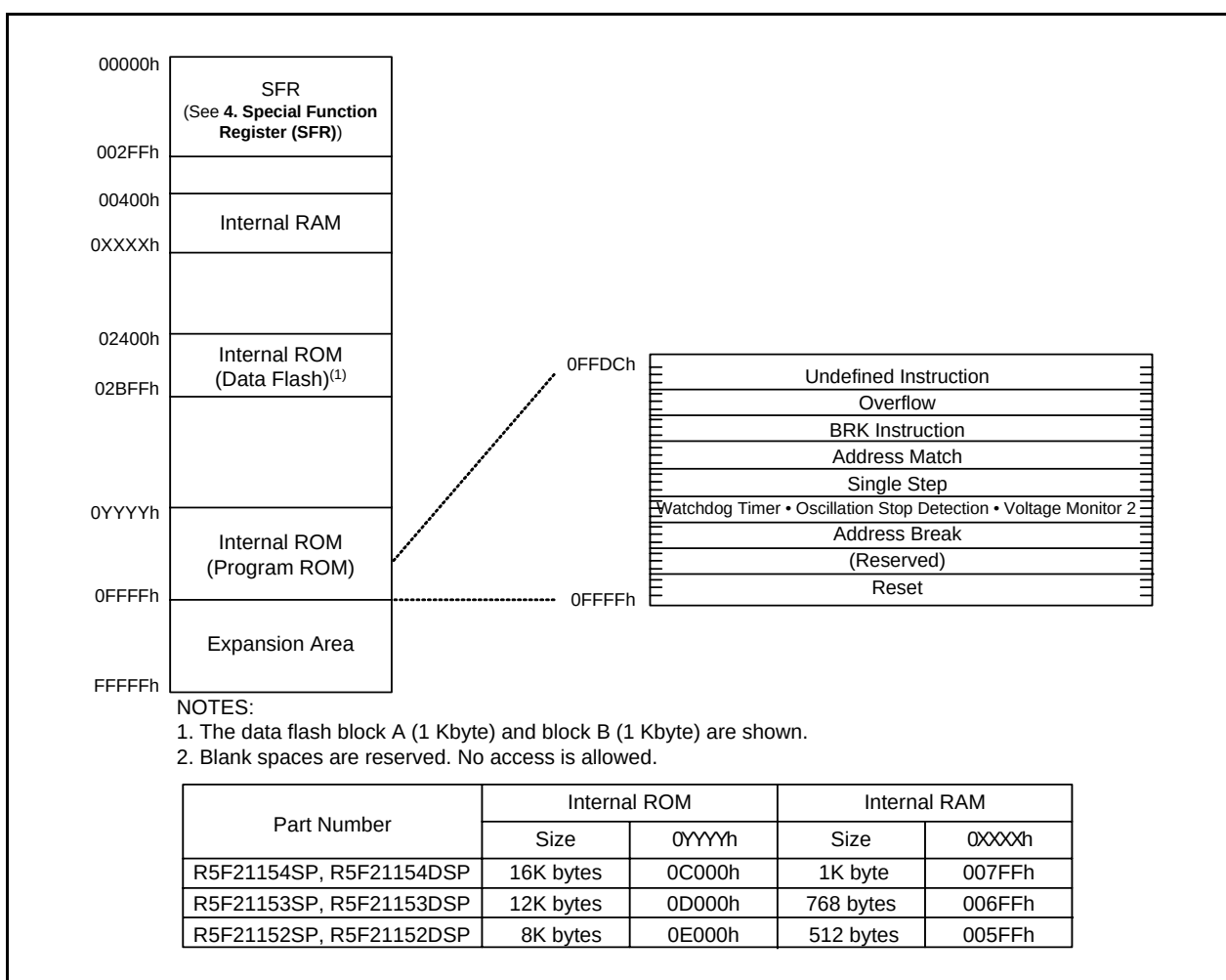


Figure 3.2 Memory Map of R8C/15 Group

4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information.

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OSD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00011111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	INT0 Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
0024h			
0025h			
0026h			
0027h			
0028h			
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾ 01000000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽²⁾	VW1C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.
- Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect this register.
- Owing to Hardware reset.
- Owing to Power-on reset or the voltage monitor 1 reset.
- Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect the b2 and b3.

Table 4.2 SFR Information(2)(1)

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register	SSUAIC	XXXXX000b
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer X Interrupt Control Register	TXIC	XXXXX000b
0057h			
0058h	Timer Z Interrupt Control Register	TZIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XXXXX000b
005Ah	INT3 Interrupt Control Register	INT3IC	XXXXX000b
005Bh	Timer C Interrupt Control Register	TCIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTES:

- Blank spaces are reserved. No access is allowed.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V _{CC}	Supply Voltage	V _{CC} = AV _{CC}	-0.3 to 6.5	V
AV _{CC}	Analog Supply Voltage	V _{CC} = AV _{CC}	-0.3 to 6.5	V
V _I	Input Voltage		-0.3 to V _{CC} +0.3	V
V _O	Output Voltage		-0.3 to V _{CC} +0.3	V
P _d	Power Dissipation	T _{opr} = 25°C	300	mW
T _{opr}	Operating Ambient Temperature		-20 to 85 / -40 to 85 (D version)	°C
T _{stg}	Storage Temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V _{CC}	Supply Voltage			2.7	—	5.5	V
AV _{CC}	Analog Supply Voltage			—	V _{CC} (3)	—	V
V _{SS}	Supply Voltage			—	0	—	V
AV _{SS}	Analog Supply Voltage			—	0	—	V
V _{IH}	Input "H" Voltage			0.8V _{CC}	—	V _{CC}	V
V _{IL}	Input "L" Voltage			0	—	0.2V _{CC}	V
I _{OH} (sum)	Peak Sum Output "H" Current	Sum of All Pins I _{OH} (peak)		—	—	-60	mA
I _{OH} (peak)	Peak Output "H" Current			—	—	-10	mA
I _{OH} (avg)	Average Output "H" Current			—	—	-5	mA
I _{OL} (sum)	Peak Sum Output "L" Currents	Sum of All Pins I _{OL} (peak)		—	—	60	mA
I _{OL} (peak)	Peak Output "L" Currents	Except P1_0 to P1_3		—	—	10	mA
		P1_0 to P1_3	Drive Capacity HIGH	—	—	30	mA
			Drive Capacity LOW	—	—	10	mA
I _{OL} (avg)	Average Output "L" Current	Except P1_0 to P1_3		—	—	5	mA
		P1_0 to P1_3	Drive Capacity HIGH	—	—	15	mA
			Drive Capacity LOW	—	—	5	mA
f _(XIN)	Main Clock Input Oscillation Frequency		3.0V ≤ V _{CC} ≤ 5.5V	0	—	20	MHz
			2.7V ≤ V _{CC} < 3.0V	0	—	10	MHz

NOTES:

1. V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V_{CC} = AV_{CC}.

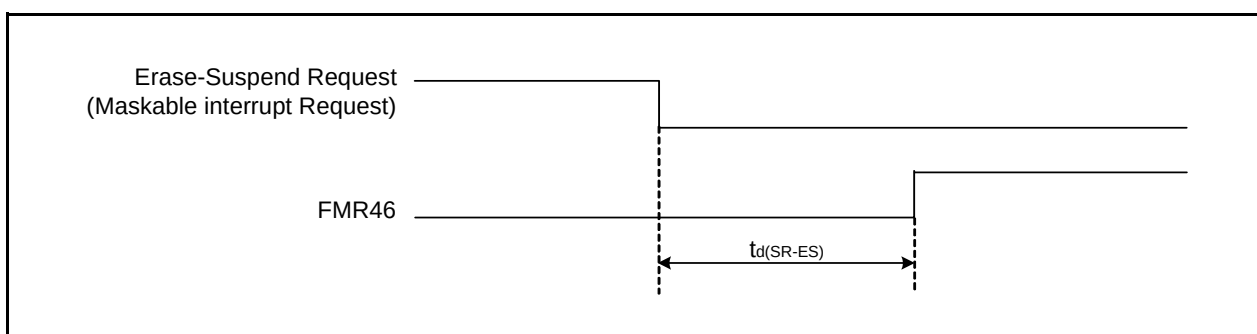


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage Detection Level ⁽³⁾		2.70	2.85	3.00	V
–	Voltage Detection Circuit Self Power Consumption	VCA26 = 1, V _{CC} = 5.0V	–	600	–	nA
t _{d(E-A)}	Waiting Time until Voltage Detection Circuit Operation Starts ⁽²⁾		–	–	100	μs
V _{ccmin}	Microcomputer Operating Voltage Minimum Value		2.7	–	–	V

NOTES:

1. The measurement condition is V_{CC} = AV_{CC} = 2.7V to 5.5V and T_{opr} = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to “1” again after setting the VCA26 bit in the VCA2 register to “0”.
3. Hold V_{det2} > V_{det1}.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det2}	Voltage Detection Level ⁽⁴⁾		3.00	3.30	3.60	V
–	Voltage Monitor 2 Interrupt Request Generation Time ⁽²⁾		–	40	–	μs
–	Voltage Detection Circuit Self Power Consumption	VCA27 = 1, V _{CC} = 5.0V	–	600	–	nA
t _{d(E-A)}	Waiting Time until Voltage Detection Circuit Operation Starts ⁽³⁾		–	–	100	μs

NOTES:

1. The measurement condition is V_{CC} = AV_{CC} = 2.7V to 5.5V and T_{opr} = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated since the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to “1” again after setting the VCA27 bit in the VCA2 register to “0”.
4. Hold V_{det2} > V_{det1}.

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-Speed On-Chip Oscillator Frequency When the Reset is Deasserted	$V_{CC} = 5.0V$, $T_{opr} = 25\text{ }^{\circ}\text{C}$	—	8	—	MHz
—	High-Speed On-Chip Oscillator Frequency Temperature • Supply Voltage Dependence	0 to +60 °C / 5 V $\pm$ 5 % ⁽²⁾	7.44	—	8.56	MHz
		–20 to +85 °C / 2.7 to 5.5 V ⁽²⁾	7.04	—	8.96	MHz
		–40 to +85 °C / 2.7 to 5.5 V ⁽²⁾	6.80	—	9.20	MHz

NOTES:

1. The measurement condition is $V_{CC} = AV_{CC} = 5.0V$ and $T_{opr} = 25\text{ }^{\circ}\text{C}$.
2. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization during Power-On ⁽²⁾		1	—	2000	μs
$t_{d(R-S)}$	STOP Exit Time ⁽³⁾		—	—	150	μs

NOTES:

1. The measurement condition is $V_{CC} = AV_{CC} = 2.7$ to $5.5V$ and $T_{opr} = 25\text{ }^{\circ}\text{C}$.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select⁽¹⁾

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK Clock Cycle Time			4	—	—	$t_{CYC}^{(2)}$
t_{HI}	SSCK Clock "H" Width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK Clock "L" Width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK Clock Rising Time	Master		—	—	1	$t_{CYC}^{(2)}$
		Slave		—	—	1	μs
t_{FALL}	SSCK Clock Falling Time	Master		—	—	1	$t_{CYC}^{(2)}$
		Slave		—	—	1	μs
t_{SU}	SSO, SSI Data Input Setup Time			100	—	—	ns
t_{H}	SSO, SSI Data Input Hold Time			1	—	—	$t_{CYC}^{(2)}$
t_{LEAD}	SCS Setup Time	Slave		$1t_{CYC}+50$	—	—	ns
t_{LAG}	SCS Hold Time	Slave		$1t_{CYC}+50$	—	—	ns
t_{OD}	SSO, SSI Data Output Delay Time			—	—	1	$t_{CYC}^{(2)}$
t_{SA}	SSI Slave Access Time			—	—	$1.5t_{CYC}+100$	ns
t_{OR}	SSI Slave Out Open Time			—	—	$1.5t_{CYC}+100$	ns

NOTES:

1. $V_{CC} = AV_{CC} = 2.7$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85\text{ }^{\circ}\text{C}$ / -40 to $85\text{ }^{\circ}\text{C}$, unless otherwise specified.
2. $1t_{CYC} = 1/f_1(s)$

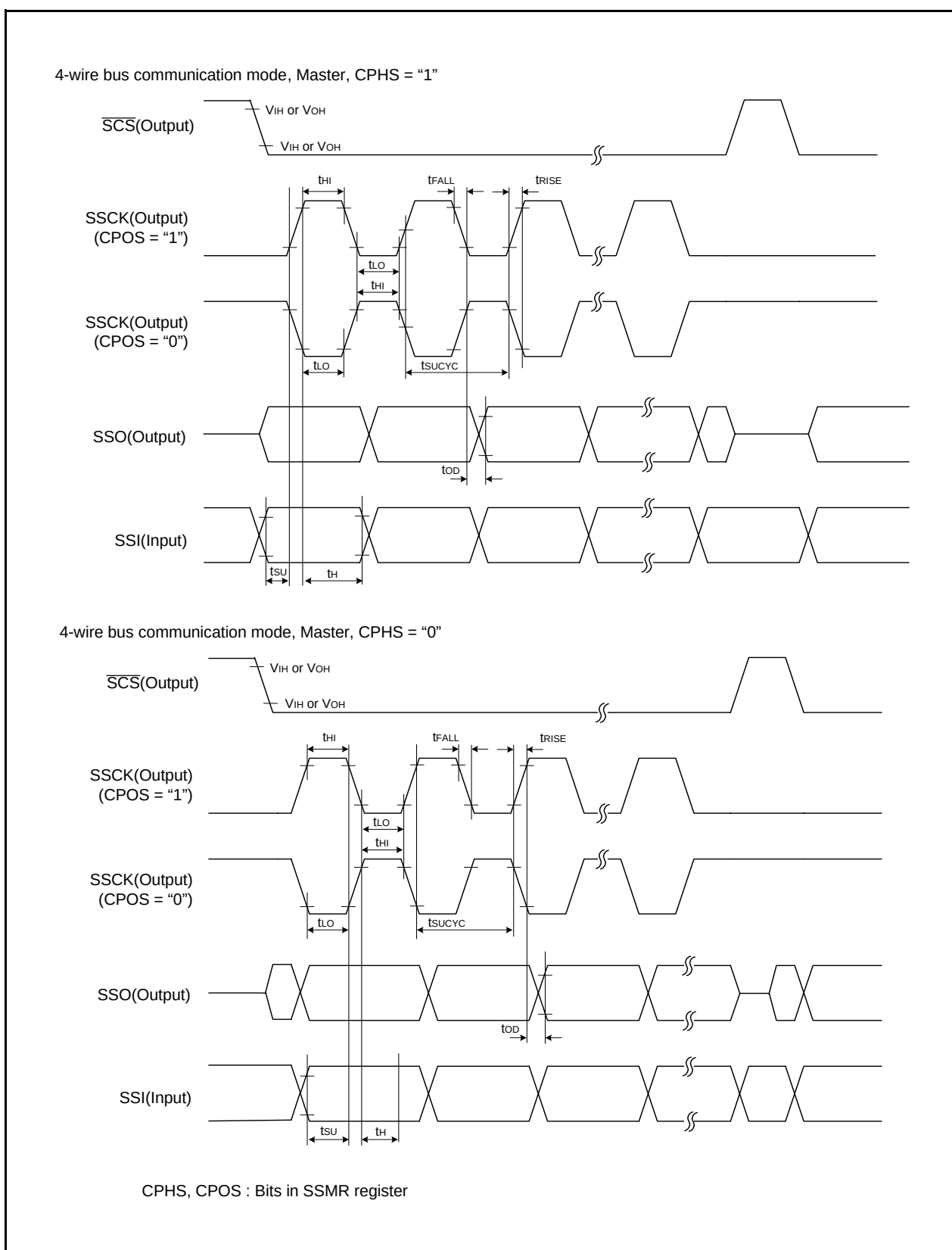


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Master)

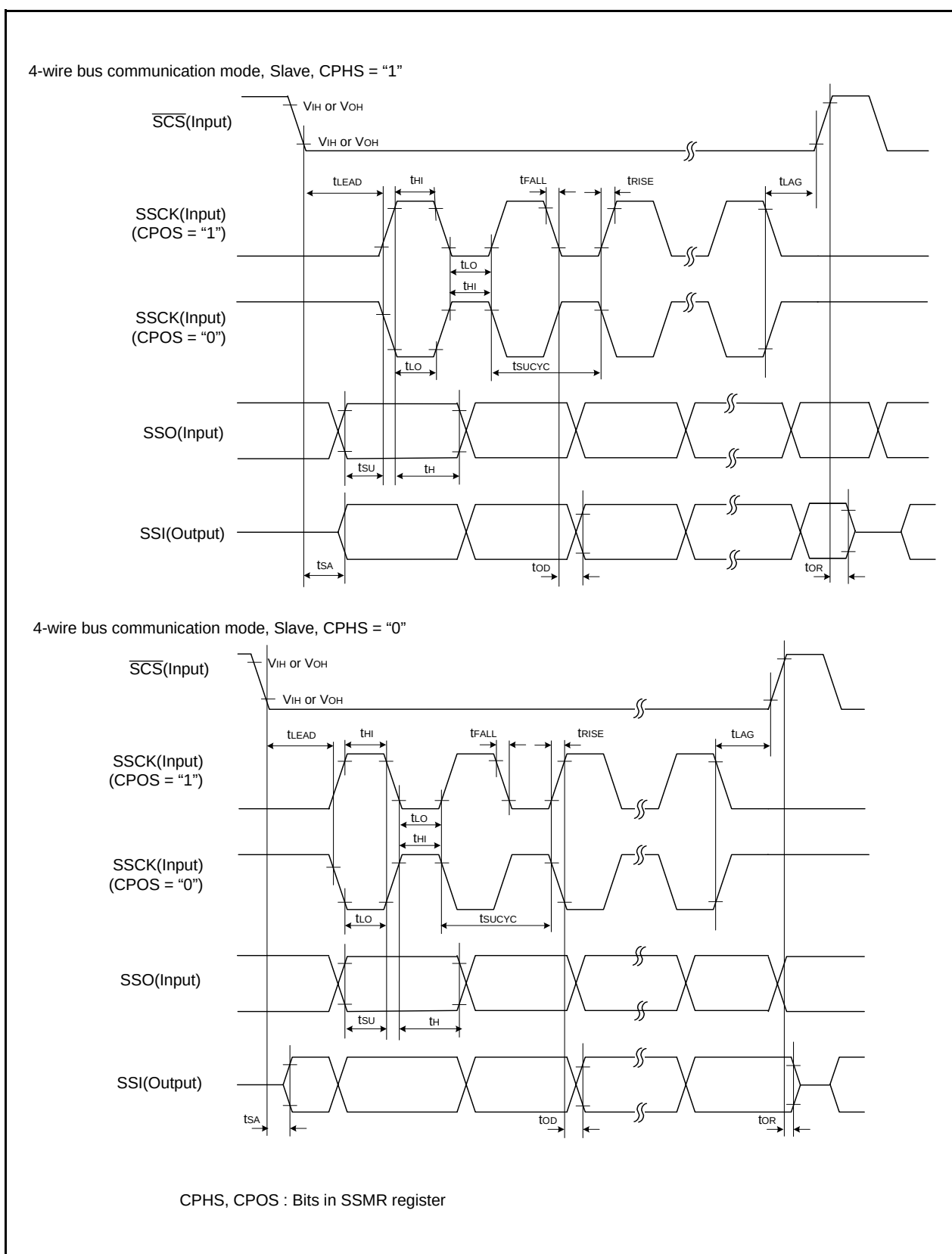


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Slave)

Table 5.13 Electrical Characteristics (1) [Vcc = 5V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output "H" Voltage	Except XOUT	IOH = -5mA		Vcc - 2.0	—	Vcc	V
			IOH = -200μA		Vcc - 0.3	—	Vcc	V
		XOUT	Drive capacity HIGH	IOH = -1mA	Vcc - 2.0	—	Vcc	V
			Drive capacity LOW	IOH = -500μA	Vcc - 2.0	—	Vcc	V
VOL	Output "L" Voltage	Except P1_0 to P1_3, XOUT	IOL = 5mA		—	—	2.0	V
			IOL = 200μA		—	—	0.45	V
		P1_0 to P1_3	Drive capacity HIGH	IOL = 15mA	—	—	2.0	V
			Drive capacity LOW	IOL = 5mA	—	—	2.0	V
			Drive capacity LOW	IOL = 200μA	—	—	0.45	V
			Drive capacity HIGH	IOL = 1mA	—	—	2.0	V
		XOUT	Drive capacity HIGH	IOL = 1mA	—	—	2.0	V
			Drive capacity LOW	IOL = 500μA	—	—	2.0	V
VT+-VT-	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RXD0, SSO			0.2	—	1.0	V
		RESET			0.2	—	2.2	V
IiH	Input "H" current		VI = 5V		—	—	5.0	μA
IiL	Input "L" current		VI = 0V		—	—	-5.0	μA
RPULLUP	Pull-Up Resistance		VI = 0V		30	50	167	kΩ
RfXIN	Feedback Resistance	XIN			—	1.0	—	MΩ
fRING-S	Low-Speed On-Chip Oscillator Frequency				40	125	250	kHz
VRAM	RAM Hold Voltage		During stop mode		2.0	—	—	V

NOTES:

1. Vcc = AVcc = 4.2 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN)=20MHz, unless otherwise specified.

Table 5.14 Electrical Characteristics (2) [Vcc = 5V] (Topr = -40 to 85 °C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power Supply Current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	9	15	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	8	14	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	5	–	mA
		Medium-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	4	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	3	–	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	2	–	mA
		High-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division	–	4	8	mA
			Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8	–	1.5	–	mA
		Low-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	470	900	μA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0	–	40	80	μA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0	–	38	76	μA
		Stop Mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	μA

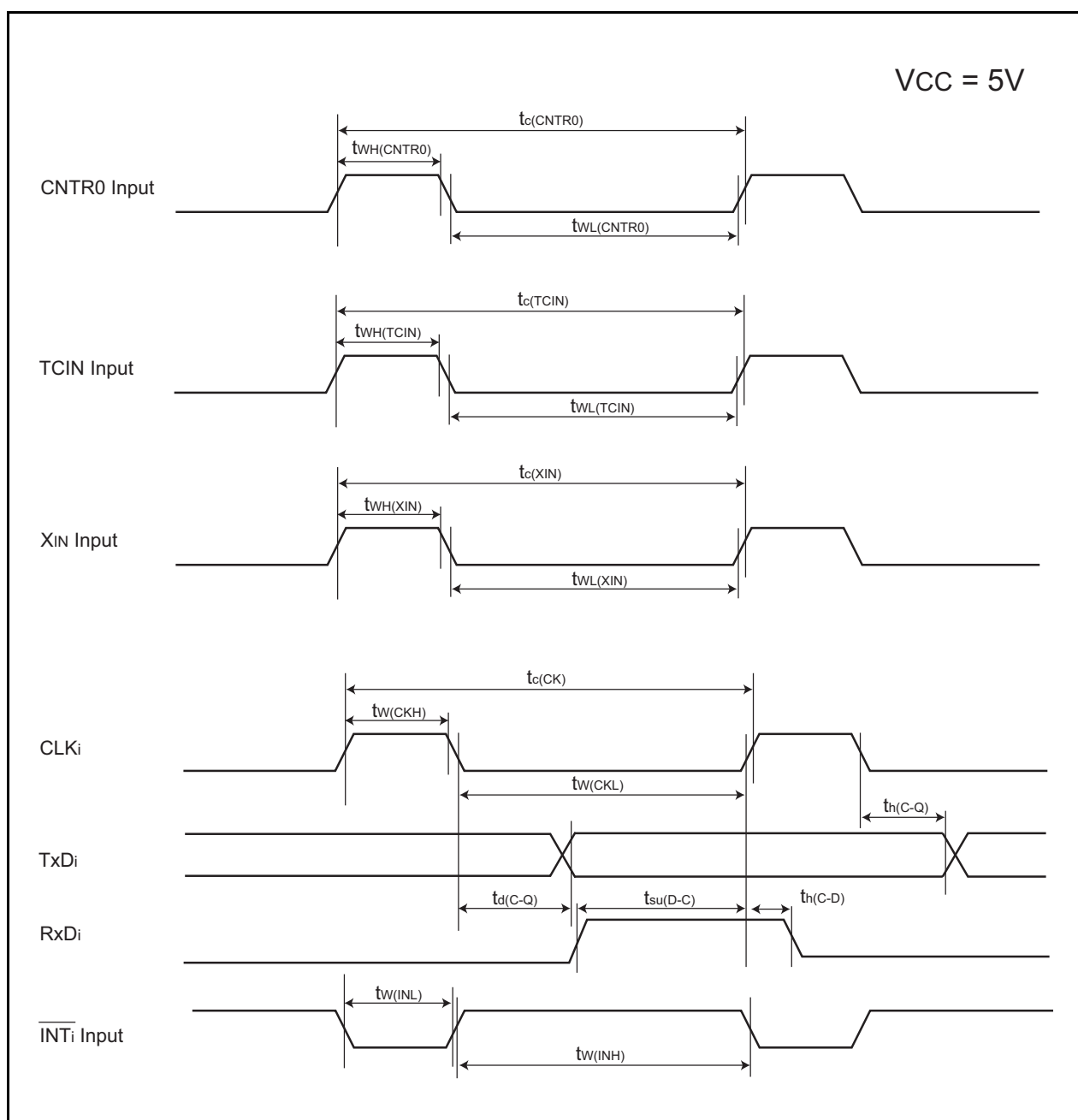


Figure 5.7 Timing Diagram When $V_{CC} = 5V$

Table 5.21 Electrical Characteristics (4) [Vcc = 3V] (Topr = -40 to 85 °C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power Supply Current (Vcc=2.7 to 3.3V) In single-chip mode, the output pins are open and other pins are Vss	High-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	8	13	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	7	12	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	5	–	mA
		Medium-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	3	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	2.5	–	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	1.6	–	mA
		High-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division	–	3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8	–	1.5	–	mA
		Low-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	420	800	μA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0	–	37	74	μA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0	–	35	70	μA
		Stop Mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.7	3.0	μA

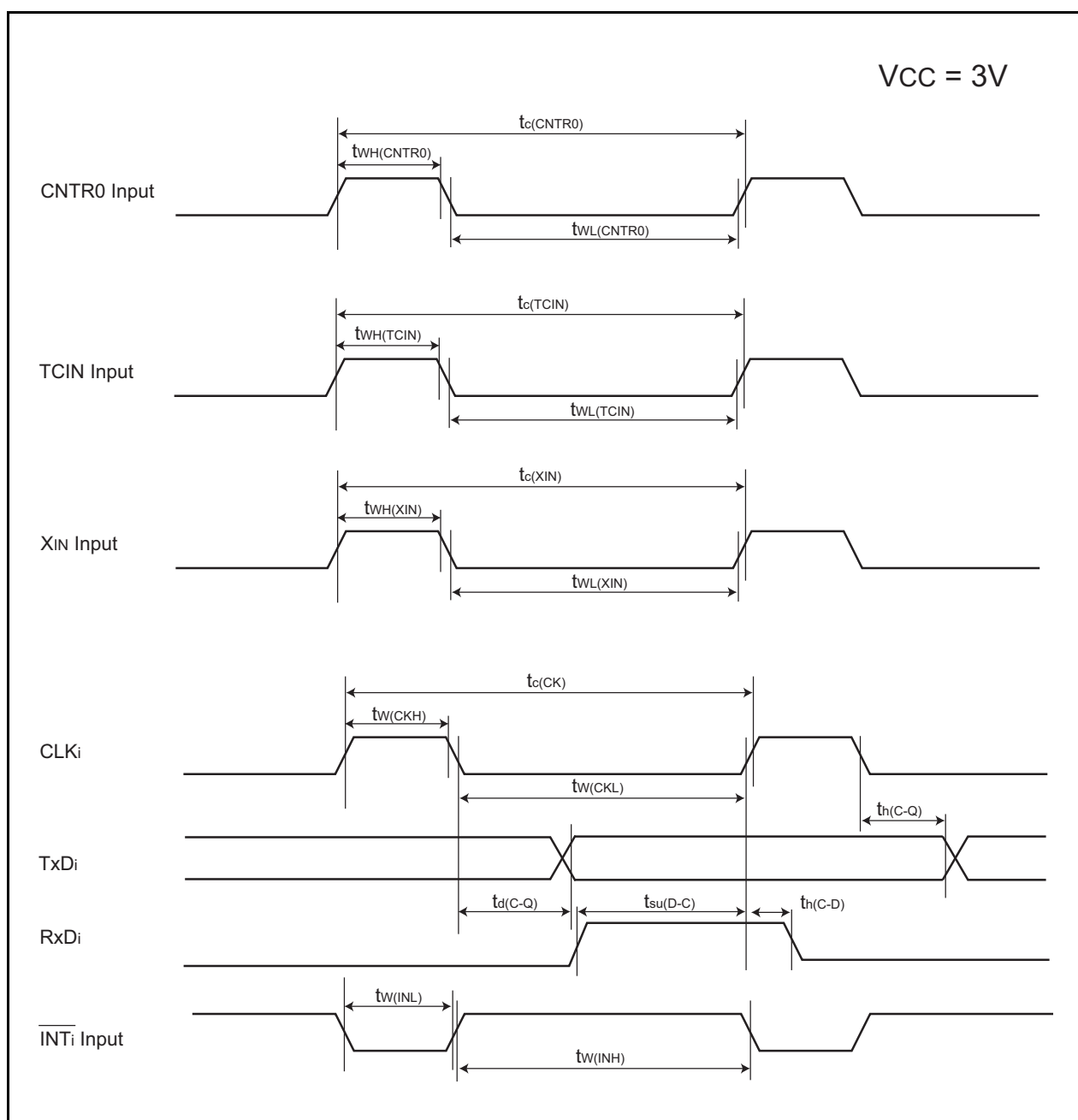


Figure 5.8 Timing Diagram When $V_{CC} = 3V$

REVISION HISTORY

R8C/14 Group, R8C/15 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Jan 30, 2006	8	Figure 1.5 PRDP0020BA-A Package Pin Assignment (top view) deleted Table 1.5 Pin Description; Timer C: "CMP0_0 to CMP0_3, CMP1_0 to CMP1_3" → "CMP0_0 to CMP0_2, CMP1_0 to CMP1_2" revised
		10	Figure 2.1 CPU Register; "Reserved Area" → "Reserved Bit" revised
		12	2.8.10 Reserved Area; "Reserved Area" → "Reserved Bit" revised
		13	Figure 3.1 Memory Map of R8C/14 Group revised
		14	3.2 R8C/15 Group; "(data area)" → "(data flash)", "(program area)" → "(program ROM)" revised Figure 3.2 Memory Map of R8C/15 Group revised
		15	Table 4.1 SFR Information(1); 0009h: "XXXXXX00b" → "00h" 000Ah: "00XXX000b" → "00h" 001Eh: "XXXXX000b" → "00h"
		17	Table 4.3 SFR Information(3); 0085h: "Prescaler Z" → "Prescaler Z Register" 0086h: "Timer Z Secondary" → "Timer Z Secondary Register" 0087h: "Timer Z Primary" → "Timer Z Primary Register" 008Ch: "Prescaler X" → "Prescaler X Register" 008Dh: "Timer X" → "Timer X Register" 0090h, 0091h: "Timer C" → "Timer C Register" revised
		21	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; • NOTES 1 to 7 added • "Topr" → "Ambient temperature", "Program area" → "Program ROM" revised
		22	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; • NOTE1 revised, NOTE9 added • "Topr" → "Ambient temperature", "Data area" → "Data flash" revised
		23	Figure 5.2 Time delay from Suspend Request until Erase Suspend revised
		24	Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset); NOTE2 revised Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset); NOTE1 revised
		25	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; revised Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select; revised
		30	Table 5.14 Electrical Characteristics (2) [Vcc = 5V]; revised
		31	"Timing Requirements (Unless ... at Ta = 25°C) [VCC = 5V]" → "Timing Requirements (Unless ... at Topr = 25°C) [VCC = 5V]" revised
		34	Table 5.18 Serial Interface; "35" → "50", "80" → "50"
		35	Table 5.21 Electrical Characteristics (4) [Vcc = 3V]; revised "Timing requirements (Unless ... at Ta = 25°C) [VCC = 3V]" → "Timing requirements (Unless ... at Topr = 25°C) [VCC = 3V]" revised
		37	Table 5.25 Serial Interface; "55" → "70", "160" → "80" Package Dimensions; Package "PRDP0020BA-A" deleted