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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	· ·
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21152sp-u0

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# RENESAS

R8C/14 Group, R8C/15 Group SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0102-0200 Rev.2.00 Jan 30, 2006

## 1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 20-pin plastic molded LSSOP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed.

Furthermore, the data flash ROM (1KB × 2blocks) is embedded in the R8C/15 group.

The difference between R8C/14 and R8C/15 groups is only the existence of the data flash ROM. Their peripheral functions are the same.

## 1.1 Applications

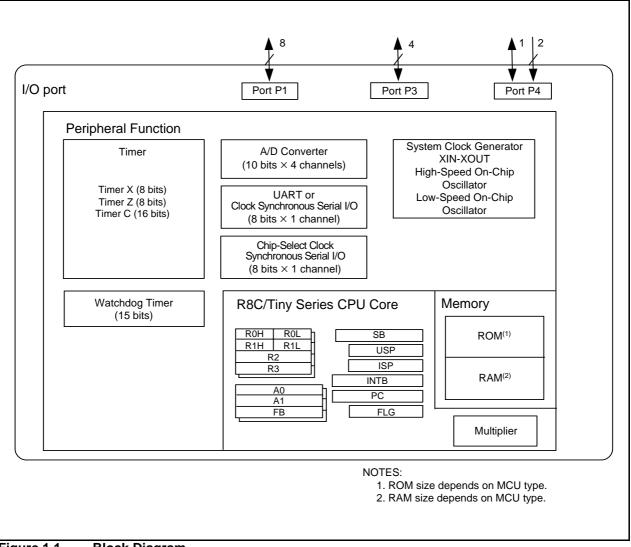
Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

	Item	Performance
CPU	Number of Basic Instructions	89 instructions
	Minimum Instruction	50ns (f(XIN)=20MHz, VCC=3.0 to 5.5V)
	Execution Time	100ns (f(XIN)=10MHz, VCC=2.7 to 5.5V)
	Operating Mode	Single-chip
	Memory Space	1 Mbyte
	Memory Capacity	See Table 1.4 R8C/15 Group Product Information
Peripheral	Port	I/O : 13 pins (including LED drive port),
Function		Input : 2 pins
	LED drive port	I/O port: 4 pins
	Timer	Timer X: 8 bits x 1 channel, Timer Z: 8 bits x 1 channel
		(Each timer equipped with 8-bit prescaler)
		Timer C: 16 bits × 1 channel
		(Circuits of input capture and output compare)
	Serial Interface	1 channel
		Clock synchronous serial I/O, UART
	Chip-select clock	1 channel
	synchronous serial I/O (SSU)	
	A/D Converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog Timer	15 bits × 1 channel (with prescaler)
		Reset start selectable, Count source protection mode
	Interrupt	Internal: 9 factors, External: 4 factors, Software: 4 factors
		Priority level: 7 levels
	Clock Generation Circuit	2 circuits
		<ul> <li>Main clock generation circuit (Equipped with a built-in</li> </ul>
		feedback resistor)
		On-chip oscillator (high speed, low speed)
		Equipped with frequency adjustment function on high-
	Oppillation Oton Data sticn	speed on-chip oscillator
	Oscillation Stop Detection	Main clock oscillation stop detection function
	Function	
	Voltage Detection Circuit	Included
	Power on Reset Circuit	
Electric	Supply Voltage	VCC=3.0 to 5.5V (f(XIN)=20MHz)
Characteristics		VCC=2.7 to 5.5V (f(XIN)=10MHz)
	Power Consumption	Typ. 9mA (VCC=5.0V, f(XIN)=20MHz)
		Typ. 5mA (VCC=3.0V, f(XIN)=10MHz)
		Typ. $35\mu A$ (VCC=3.0V, wait mode, peripheral clock off)
		Typ. 0.7µA (VCC=3.0V, stop mode)
Flash Memory	Program/Erase Supply	VCC=2.7 to 5.5V
	Voltage	
	Program/Erase Endurance	10,000 times (Data flash)
		1,000 times (Program ROM)
Operating Ambi	ent Temperature	-20 to 85°C
		-40 to 85°C (D Version)
Package		20-pin plastic mold LSSOP

## Table 1.2 Performance Outline of the R8C/15 Group

## 1.3 Block Diagram

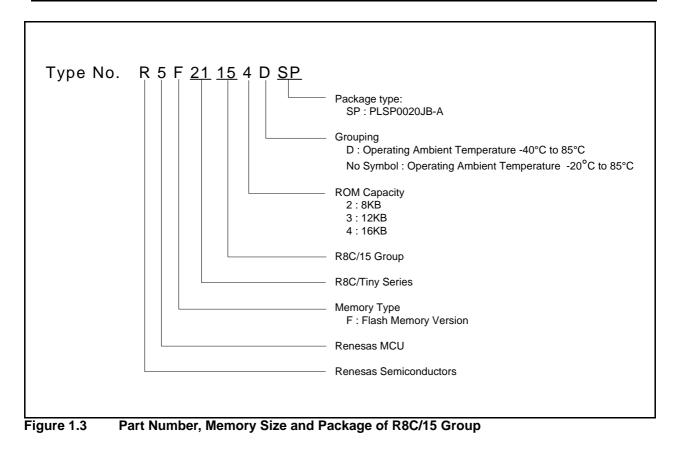
Figure 1.1 shows a Block Diagram.





Type No.	ROM ca	pacity	RAM	Package type	Remarks
Type No.	Program ROM	Data flash	capacity	Fackage type	ITEIIIaIKS
R5F21152SP	8 Kbytes	1 Kbyte x 2	512 bytes	PLSP0020JB-A	Flash memory version
R5F21153SP	12 Kbytes	1 Kbyte x 2	768 bytes	PLSP0020JB-A	
R5F21154SP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A	
R5F21152DSP	8 Kbytes	1 Kbyte x 2	512 bytes	PLSP0020JB-A	D version
R5F21153DSP	12 Kbytes	1 Kbyte x 2	768 bytes	PLSP0020JB-A	
R5F21154DSP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A	

### Table 1.4 Product Information of R8C/15 Group



As of Jan 2006

## 1.5 Pin Assignments

Figure 1.4 shows the PLSP0020JB-A Package Pin Assignment (top view).

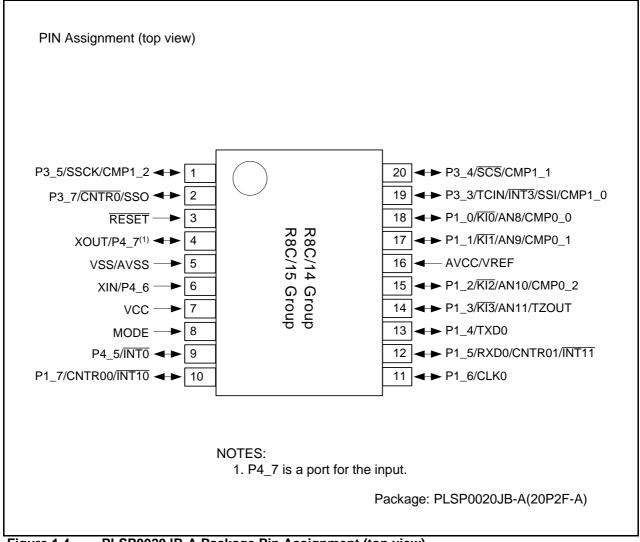


Figure 1.4 PLSP0020JB-A Package Pin Assignment (top view)

## 2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

## 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

## 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

## 2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

## 2.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

## 2.8.3 Zero Flag (Z)

The Z flag is set to "1" when an arithmetic operation resulted in 0; otherwise, "0".

## 2.8.4 Sign Flag (S)

The S flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, "0".

## 2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is "0". The register bank 1 is selected when this flag is set to "1".

## 2.8.6 Overflow Flag (O)

The O flag is set to "1" when the operation resulted in an overflow; otherwise, "0".

## 2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0", and are enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt request is acknowledged.

## 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is set to "0", USP is selected when the U flag is set to "1". The U flag is set to "0" when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

## 2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has greater priority than IPL, the interrupt is enabled.

## 2.8.10 Reserved Bit

When write to this bit, set to "0". When read, its content is indeterminate.

## 3. Memory

## 3.1 R8C/14 Group

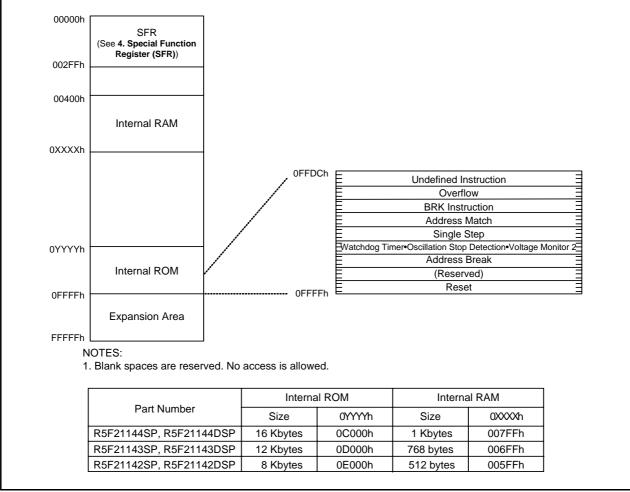
Figure 3.1 is a Memory Map of R8C/14 Group. The R8C/14 group provides 1-Mbyte address space from addresses 00000h to FFFFh.

The internal ROM is allocated lower addresses beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.





Memory Map of R8C/14 Group

## 3.2 R8C/15 Group

Figure 3.2 is a Memory Map of R8C/15 Group. The R8C/15 group provides 1-Mbyte address space from addresses 00000h to FFFFh.

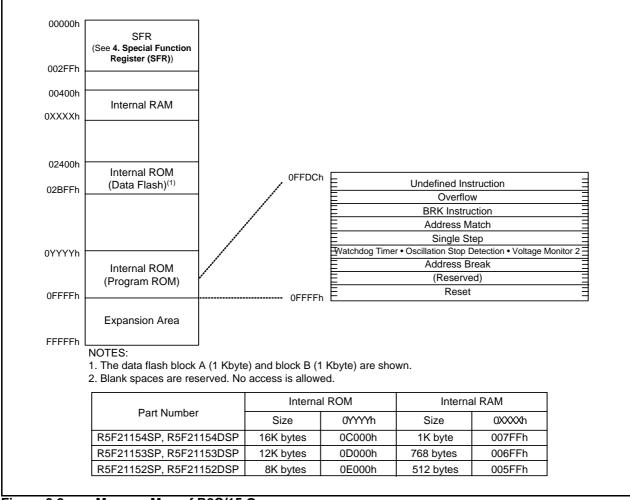
The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.

Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.





Memory Map of R8C/15 Group

## 4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information.

Table 4.1 SFR Information(1)<sup>(1)</sup>

Address 0000h			
	Register	Symbol	After reset
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	0010000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
0000Ah	Protect Register	PRCR	00h
000An		FROM	0011
000Bn	Oscillation Otom Datasticn Devictor	000	000004005
	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00011111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h	1		X0h
0017h			
0018h			
0019h			
0013h			
001An			
		0000	
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	INT0 Input Filter Select Register	INTOF	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h	······································		
002011			
002Ah			
002An			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1 <sup>(2)</sup>	VCA1	00001000b
0032h	Voltage Detection Register 2 <sup>(2)</sup>	VCA2	00h <sup>(3)</sup>
			0100000b <sup>(4)</sup>
0033h			
0033h			
0034h			
		10040	
0036h	Voltage Monitor 1 Circuit Control Register (2)	VW1C	0000X000b <sup>(3)</sup>
			0100X001b <sup>(4)</sup>
0037h	Voltage Monitor 2 Circuit Control Register (5)	VW2C	00h
0038h			
0039h			
0039h 003Ah			
0039h 003Ah 003Bh			
0039h 003Ah 003Bh 003Ch			
0039h 003Ah 003Bh 003Ch 003Dh			
0039h 003Ah 003Bh 003Ch			

X: Undefined

NOTES:

- 1. Blank spaces are reserved. No access is allowed.
- 2. Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect this register.

3. Owing to Hardware reset.

- 4. Owing to Power-on reset or the voltage monitor 1 reset.
- 5. Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect the b2 and b3.

Address	Register	Symbol	After reset
0040h	i vegisiei	Symbol	Alter reset
0040h			
0041h			
0042h			
0043h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU Interrupt Control Register	SSUAIC	XXXXX000b
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UARTO Transmit Interrupt Control Register	SOTIC	XXXXX000b
0052h	UARTO Receive Interrupt Control Register	SORIC	XXXXX000b
0053h			
0054h			
0055h			
0056h	Timer X Interrupt Control Register	TXIC	XXXXX000b
0057h			
0058h	Timer Z Interrupt Control Register	TZIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XXXXX000b
005Ah		INT3IC	XXXXX000b
	INT3 Interrupt Control Register Timer C Interrupt Control Register		XXXXX000b
005Bh	Compare 0 Interrupt Control Register	TCIC CMP0IC	
005Ch		INTOIC	XXXXX000b XX00X000b
005Dh	INT0 Interrupt Control Register	INTOIC	A000A000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h 0068h			
0068h			
0069h			
006Ah 006Bh			
006Bh			
006Ch 006Dh			
006Dh			
006Eh			
008Fn			
0070h			
0071h			
0072h			
0073h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			
1	1	1	1

## Table 4.2SFR Information(2)(1)

X: Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.

DOCUM         AD         XD         XA           DOCTH         XD         XA           DOCTH         XXA	Address	Register	Symbol	After reset
0007h		A/D Register		
0002h		, , , , , , , , , , , , , , , , , , ,		
0002h				
00C4h				
00026h				
00C6h				
0002h				
0002h	00C7h			
00CSh				
0026h				
0026h	00CAh			
00CCh				
00CEh				
00CFh	00CDh			
00D0h	00CEh			
00D1h	00CFh			
00D2h				
0003h         AD Control Register 2         ADCON2         00h           0015h         AD Control Register 0         ADCON2         00h           0015b         AD Control Register 0         ADCON1         00h           0015h         AD Control Register 1         ADCON1         00h           0015h         AD Control Register 1         ADCON1         00h           0015h         AD Control Register 1         ADCON1         00h           0015h         ADCON1         ADCON1         Image: Control Register 1           0015h         Image: Control Register 1         Image: Control Register 1         Image: Control Register 1           0015h         Image: Control Register 1         Image: Control Register 1         Image: Control Register 1         Image: Control Register 1           0015h         Port P1 Direction Register 1         P1         XXh         Image: Control Register 1           0015h         Port P3 Direction Register 1         P13         Image: Control Register 1         Image: Control Register 1         Image: Control Register 1           0015h         Port P4 Direction Register 1         PD4         Image: Control Register 1         Image: Control Register 1	00D1h			
ODD4h         AD Control Register 2         ADCON2         Obh           ODD5h         AD Control Register 0         ADCON1         00000XXb           ODD7h         AD Control Register 1         ADCON1         00h           ODD8h         Control Register 1         Control Register 1         Control Register 1           ODD5h         Control Register 2         P1         XXh           ODD5h         Control Register 2         P1         XXh           ODD5h         Control Register 2         P1         XXh           ODE2h         Port P1 Direction Register 3         P1         XXh           ODE5h         Port P3 Register 3         P3         XXh           ODE6h         Port P3 Register 3         P4         XXh           ODE5h         Port P4 Register 3         P4         Xh           ODE6h         Port P4 Register 3         P4         Xh           ODE5h         Port P4 Register 3         P4         Xh           ODE6h         P14 <td< td=""><td>00D2h</td><td></td><td></td><td></td></td<>	00D2h			
00D5h         AD Control Register 0         ADCON0         00000XXbb           00D5h         AD Control Register 1         ADCON0         00000XXb           00D5h         AD Control Register 1         ADCON1         00h           00D5h         ADCON1         00h         00h           00D5h         Part 1         ADCON1         00h           00D5h         Part 1         Part 1         Part 1           00D5h         Part 1         Rxh         Part 1           00D5h         Part 1         Rxh         Part 1           00D5h         Part 1         Rxh         Part 1           00E5h         Part 1         Rxh         Part 1           00E5h         Part 19 Register         Part 10         Part 10           00E5h         Part 19 Register         Part 20         Part 20           00E5h         Part 24 Register         Part 3         Xh           00E5h         Part 24 Register         Part 3         Nh           00E5h	00D3h			
00D5h         AD Control Register 0         ADCON0         00000XXbb           00D5h         AD Control Register 1         ADCON0         00000XXb           00D5h         AD Control Register 1         ADCON1         00h           00D5h         ADCON1         00h         00h           00D5h         Part 1         ADCON1         00h           00D5h         Part 1         Part 1         Part 1           00D5h         Part 1         Rxh         Part 1           00D5h         Part 1         Rxh         Part 1           00D5h         Part 1         Rxh         Part 1           00E5h         Part 1         Rxh         Part 1           00E5h         Part 19 Register         Part 10         Part 10           00E5h         Part 19 Register         Part 20         Part 20           00E5h         Part 24 Register         Part 3         Xh           00E5h         Part 24 Register         Part 3         Nh           00E5h		A/D Control Register 2	ADCON2	00h
00D7h         A/D Control Register 1         00h           00D8h         00h           0010h         00h <td>00D5h</td> <td></td> <td></td> <td></td>	00D5h			
00D7h         A/D Control Register 1         00h           00D8h         00h           0010h         00h <td>00D6h</td> <td>A/D Control Register 0</td> <td>ADCON0</td> <td>00000XXXb</td>	00D6h	A/D Control Register 0	ADCON0	00000XXXb
00D8h	00D7h	A/D Control Register 1	ADCON1	
00DAh	00D8h	-		
00DAh				
000Bh				
000Dh				
000Eh	00DCh			
000Ph         Pdt P1 Register         P1         XXh           00E1h         Port P1 Register         PD1         00h           00E2h         00h         00h         00h           00E3h         Port P1 Direction Register         PD1         00h           00E3h         Port P3 Register         P3         XXh           00E5h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         PD3         00h           00E8h         Port P4 Register         PD3         00h           00E8h         Port P4 Register         PD4         00h           00E8h         Port P4 Register         PD4         00h           00E8h         Port P4 Direction Register         PD4         00h           00F8h         Port P4         Port P4         Port P4           00F8h         Port P4         Port P4         Port P4           00F8h         Port P1 Dire Capacity Control Register 0         PUR0	00DDh			
O0E 0h         Port P1 Register         P1         XXh           O0E 2h         00E 3h         Port P1 Direction Register         PD1         00h           00E 3h         Port P1 Direction Register         PD1         00h           00E 3h         Port P3 Register         P3         XXh           00E 6h         P3 Direction Register         P03         00h           00E 7h         Port P3 Direction Register         P03         00h           00E 8h         Port P4 Register         P4         XXh           00E 8h         Port P4 Register         P4         Xh           00E 8h         Port P4 Direction Register         PD4         00h           00E 8h         Port P4 Direction Register         PO         00F <tr< td=""><td></td><td></td><td></td><td></td></tr<>				
OOE1h         Port P1 Register         P1         XXh           OOE2h         Port P1 Direction Register         PD1         00h           OOE4h         P3         XXh           OOE5h         Port P3 Register         P3         XXh           OOE5h         Port P3 Register         P03         00h           OOE5h         Port P4 Register         P03         00h           OOE5h         Port P4 Register         P4         XXh           OOE5h         Port P4 Direction Register         P04         00h           OOE5h         Port P4 Direction Register         P04         00h           OOE5h         OOE              OOE5h         OOE               OOE5h                 OOE5h                   OOE5h <t< td=""><td>00DFh</td><td></td><td></td><td></td></t<>	00DFh			
00E2h         00E3h         Port P1 Direction Register         PD1         00h           00E3h         Port P3 Direction Register         P3         XXh           00E5h         Port P3 Register         P03         0h           00E5h         Port P3 Direction Register         P03         0h           00E5h         Port P4 Register         P4         XXh           00E5h         Port P4 Register         P4         XXh           00E5h         Port P4 Register         P04         0h           00E5h         Port P4 Register         P04         0h           00E5h         Port P4 Direction Register         PD4         PD4           00E5h         Port P4 Direction Register         PD4         PD4           00F5h         PD4         PD4         PD4         PD4           00F5h         PD4         PD4         PD4         PD4           00F5h	00E0h			
ODE3h         Port P1 Direction Register         PD1         O0h           ODE4h         Port P3 Register         P3         XXh           ODE5h         Port P3 Direction Register         PD3         00h           ODE5h         Port P4 Register         PD3         00h           ODE5h         Port P4 Register         PD4         XXh           ODE5h         Port P4 Register         PD4         00h           ODE5h         Port P4 Direction Register         PD4         00h           ODE5h         Port P4         PO1         PO1         PO1           ODF5h         Port P4         PO1         PO1         PO1           ODF5h         Port P4         PO1         PO1         PO1           ODF5h         Po1         PO1         PO1         PO1           ODF6h         PO1         PO1         PO1         PO1           ODF6h	00E1h	Port P1 Register	P1	XXh
00E4h         Port P3 Register         P3         XXh           00E5h         Port P3 Direction Register         PD3         00h           00E5h         Port P4 Register         P4         XXh           00E5h         Port P4 Register         P4         XXh           00E5h         Port P4 Register         PD4         00h           00E5h         P014         00h         P014         P014           00E5h         P014         00h         P014         P014         P014           00E5h         P014         P	00E2h			
00E4h         Port P3 Register         P3         XXh           00E5h         Port P3 Direction Register         PD3         00h           00E5h         Port P4 Register         P4         XXh           00E5h         Port P4 Register         P4         XXh           00E5h         Port P4 Register         PD4         00h           00E5h         P014         00h         P014         P014           00E5h         P014         00h         P014         P014         P014           00E5h         P014         P	00E3h	Port P1 Direction Register	PD1	00h
00E6h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E8h         Port P4 Direction Register         P04         00h           00E8h         Port P4 Direction Register         P04         00h           00E8h         Port P4 Direction Register         P04         00h           00E6h         P04         00h         P04         00h           00E6h         P04         P04         P04         P04         P04           00E7h         P04         P04 <td>00E4h</td> <td></td> <td></td> <td></td>	00E4h			
00E6h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E8h         Port P4 Direction Register         P04         00h           00E8h         Port P4 Direction Register         P04         00h           00E8h         Port P4 Direction Register         P04         00h           00E6h         P04         00h         P04         00h           00E6h         P04         P04         P04         P04         P04           00E7h         P04         P04 <td>00E5h</td> <td>Port P3 Register</td> <td>P3</td> <td>XXh</td>	00E5h	Port P3 Register	P3	XXh
00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E8h         PD1 P4 Direction Register         PD4         00h           00E8h         PD4         00h         00h           00E8h         PD4         PD4         00h           00E8h         PD4         PD4         00h           00F7h         PD4         PD4         PD4	00E6h			
O0E9h         Port P4 Direction Register         PD4         O0h           00ECh		Port P3 Direction Register	PD3	00h
O0E9h         Port P4 Direction Register         PD4         O0h           00ECh		Port P4 Register	P4	XXh
00EBh	00E9h			
00ECh		Port P4 Direction Register	PD4	00h
00EDh				
00EEh	00ECh			
00EFh	00EDh			
00F0h	00EEh			
00F1h				
00F2h				
00F3h				
00F4h				
00F5h				
00F6h				
00F7h				
00F8h				
00F9h				
00FAh				
00FAh	00F9h			
00FCh       Pull-Up Control Register 0       PUR0       00XX0000b         00FDh       Pull-Up Control Register 1       PUR1       XXXXXX0Xb         00FEh       Port P1 Drive Capacity Control Register       DRR       00h         00FFh       Timer C Output Control Register       DRR       00h         01B3h       Flash Memory Control Register 4       FMR4       01000000b         01B4h       01B5h       Flash Memory Control Register 1       1000000xb         01B6h       01B7h       Flash Memory Control Register 0       FMR0	00FAh			
00FDh       Pull-Up Control Register 1       PUR1       XXXXX0Xb         00FEh       Port P1 Drive Capacity Control Register       DRR       00h         00FFh       Timer C Output Control Register       TCOUT       00h         01B3h       Flash Memory Control Register 4       FMR4       01000000b         01B4h       01B5h       Flash Memory Control Register 1       1000000Xb         01B6h       01B7h       Flash Memory Control Register 0       FMR0				
00FEh       Port P1 Drive Capacity Control Register       DR       00h         00FFh       Timer C Output Control Register       TCOUT       00h         01B3h       Flash Memory Control Register 4       FMR4       01000000b         01B4h       0185h       Flash Memory Control Register 1       1000000Xb         01B6h       FMR1       1000000Xb         01B7h       Flash Memory Control Register 0       FMR0       00000001b		Pull-Up Control Register 0		
00FFh     Timer C Output Control Register     TCOUT     00h       01B3h     Flash Memory Control Register 4     FMR4     01000000b       01B4h	00FDh	Pull-Up Control Register 1		
01B3h       Flash Memory Control Register 4       FMR4       01000000b         01B4h       01000000b       010000000b         01B5h       Flash Memory Control Register 1       FMR1       10000000b         01B6h       010000000b       010000000b       010000000b         01B7h       Flash Memory Control Register 0       FMR0       00000001b		Port P1 Drive Capacity Control Register		
01B4h       01B5h       Flash Memory Control Register 1       FMR1       1000000Xb         01B6h       01B7h       Flash Memory Control Register 0       FMR0       00000001b	00FFh	Timer C Output Control Register	TCOUT	00h
01B4h       01B5h       Flash Memory Control Register 1       FMR1       1000000Xb         01B6h       01B7h       Flash Memory Control Register 0       FMR0       00000001b				
01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h		Flash Memory Control Register 4	FMR4	0100000b
01B6h     01B7h     Flash Memory Control Register 0     FMR0     00000001b				
01B7h Flash Memory Control Register 0 FMR0 0000001b	01B5h	Flash Memory Control Register 1	FMR1	100000Xb
0FFFFh Optional Function Select Register OFS (2)	01B7h	Flash Memory Control Register 0	FMR0	0000001b
UFFFh         Uptional Function Select Register         OFS         (2)				
	UFFFFh	Optional Function Select Register	OFS	(2)

## Table 4.4SFR Information(4)<sup>(1)</sup>

X: Undefined

NOTES:

1. Blank columns, 0100h to 01B2h and 01B8h to 02FFh are all reserved. No access is allowed.

2. The OFS register cannot be changed by program. Use a flash programmer to write to it.

Symbol	Parameter	Conditions		Standard		Unit
Symbol	Farameter	Conditions	Min.	Тур.	Max.	Unit
-	Program/Erase Endurance <sup>(2)</sup>	R8C/14 Group	100 <sup>(3)</sup>	-	=	times
		R8C/15 Group	1,000(3)	-	-	times
-	Byte Program Time	Vcc = 5.0 V at Topr = 25 °C	-	50	400	μs
-	Block Erase Time	Vcc = 5.0 V at Topr = 25 °C	-	0.4	9	S
td(SR-ES)	Time Delay from Suspend Request until Erase Suspend		-	-	8	ms
-	Erase Suspend Request Interval		10	-	-	ms
-	Program, Erase Voltage		2.7	-	5.5	V
-	Read Voltage		2.7	-	5.5	V
-	Program, Erase Temperature		0	-	60	°C
_	Data Hold Time <sup>(7)</sup>	Ambient temperature = 55 °C	20	-	-	year

### Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

NOTES:

1. Vcc = AVcc = 2.7 to 5.5V at Topr = 0 to 60 °C, unless otherwise specified.

Definition of program and erase
 The program and erase endurance shows an erase endurance for every block.
 If the program and erase endurance is "n" times (n = 100, 10000), "n" times erase can be performed for every block.
 For example, if performing 1-byte write to the distinct addresses on Block A of 1Kbyte block 1,024 times and then erasing that block, program and erase endurance is counted as one time.

However, do not perform multiple programs to the same address for one time ease.(disable overwriting).

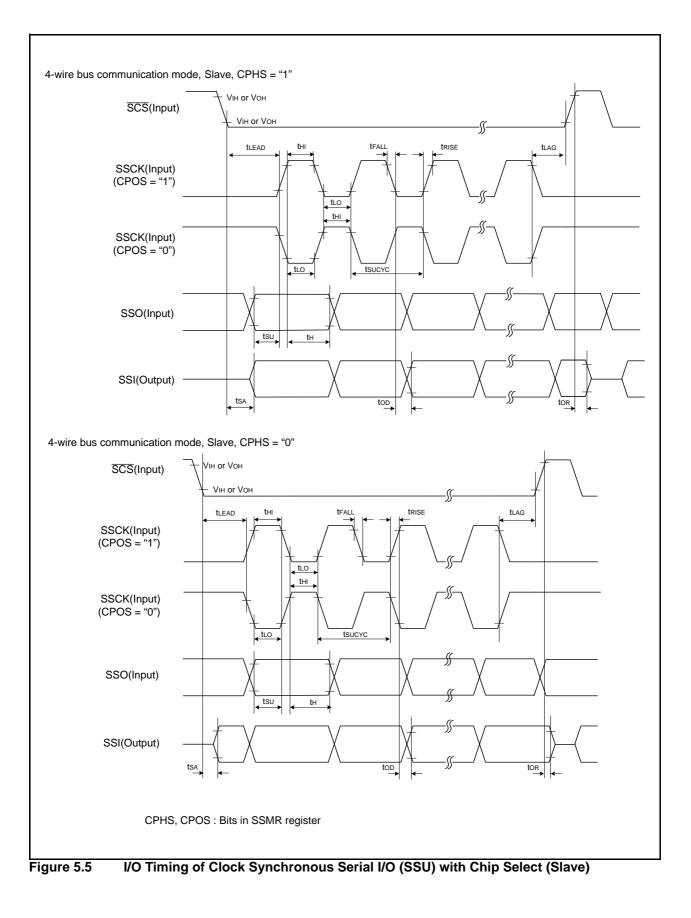
3. Endurace to guarantee all electrical characteristics after program and erase.(1 to "Min." value can be guaranateed).

4. In the case of a system to execute multiple programs, perform one erase after programming as reducing effective reprogram endurance not to leave blank area as possible such as programming write addresses in turn. If programming a set of 16 bytes, programming up to 128 sets and then erasing them one time can reduce effective reprogram endurance. Additionally, averaging erase endurance for Block A and B can reduce effective reprogram endurance more. To leave erase endurance for every block as information and determine the restricted endurance are recommended.

5. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.

6. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.

7. The data hold time incudes time that the power supply is off or the clock is not supplied.



Symbol	Parameter		Condition		Standard		Unit
Symbol	Falameter		Condition	Min.	Тур.	Max.	Unit
Icc	Power Supply Current (Vcc=3.3 to 5.5V) In single-chip mode,	High-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	_	9	15	mA
	the output pins are open and other pins are Vss		XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	_	8	14	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	-	5	_	mA
		Medium- Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	_	4	_	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	_	3	_	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	_	2	_	mA
	On-C Oscill	High-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division	_	4	8	mA
			Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8	_	1.5	_	mA
		Low-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	_	470	900	μΑ
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0	-	40	80	μΑ
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0	_	38	76	μΑ
		Stop Mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	_	0.8	3.0	μΑ

## Table 5.14 Electrical Characteristics (2) [Vcc = 5V] (Topr = -40 to 85 °C, unless otherwise specified.)

### Timing Requirements (Unless otherwise specified: Vcc = 5V, Vss = 0V at Topr = 25 °C) [ Vcc = 5V ]

### Table 5.15 XIN Input

Symbol	Parameter	Stan	dard	Unit
Symbol	Falanielei	Min.	Max.	Offic
tc(XIN)	XIN Input Cycle Time	50	-	ns
twh(XIN)	XIN Input "H" Width	25	-	ns
twl(XIN)	XIN Input "L" Width	25	-	ns

## Table 5.16 CNTR0 Input, CNTR1 Input, INT1 Input

Symbol	Parameter	Stan	00 -	Unit
Symbol	Falanielei	Min.	Max.	Onit
tc(CNTR0)	CNTR0 Input Cycle Time	100	_	ns
tWH(CNTR0)	CNTR0 Input "H" Width	40	=	ns
twl(CNTR0)	CNTR0 input "L" Width	40	-	ns

## Table 5.17TCIN Input, INT3 Input

Symbol	Parameter	Stan	dard	Unit
Symbol	Falanielei	Min.	Max.	Onit
tc(TCIN)	TCIN Input Cycle Time	400(1)	-	ns
tWH(TCIN)	TCIN Input "H" Width	200 <sup>(2)</sup>	-	ns
twl(tcin)	TCIN input "L" Width	200(2)	_	ns

NOTES:

1. When using Timer C input capture mode, adjust the cycle time (1/Timer C count source frequency x 3) or above.

2. When using Timer C input capture mode, adjust the width (1/Timer C count source frequency x 1.5) or above.

### Table 5.18 Serial Interface

Symbol	Parameter	Stan	Unit	
Symbol	Falameter	Min.	Max.	Unit
tc(CK)	CLKi Input Cycle Time	200	-	ns
tW(CKH)	CLKi Input "H" Width	100	-	ns
tW(CKL)	CLKi Input "L" Width	100	-	ns
td(C-Q)	TXDi Output Delay Time	-	50	ns
th(C-Q)	TXDi Hold Time	0	-	ns
tsu(D-C)	RXDi Input Setup Time	50	-	ns
th(C-D)	RCDi Input Hold Time	90	-	ns

### Table 5.19 External Interrupt INT0 Input

Symbol	Parameter -	Standard		Unit
Symbol		Min.	Max.	Unit
tw(INH)	INTO Input "H" Width	250 <sup>(1)</sup>	-	ns
tw(INL)	INTO Input "L" Width	250(2)	_	ns

NOTES:

1. When selecting the digital filter by the INTO input filter select bit, use the INTO input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

2. When selecting the digital filter by the INTO input filter select bit, use the INTO input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

Symbol	Parameter	Condition	Standard			Unit	
			Min.	Тур.	Max.	Unit	
	Power Supply Current (Vcc=2.7 to 3.3V) In single-chip mode,	High-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	_	8	13	mA
	the output pins are open and other pins are Vss		XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	_	7	12	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	-	5	-	mA
		Medium- Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	_	3	_	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	_	2.5	_	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	_	1.6	_	mA
		High-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division	_	3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8	_	1.5	_	mA
		Low-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	_	420	800	μΑ
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0	_	37	74	μΑ
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0	_	35	70	μΑ
		Stop Mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	_	0.7	3.0	μΑ

## Table 5.21 Electrical Characteristics (4) [Vcc = 3V] (Topr = -40 to 85 °C, unless otherwise specified.)

## Timing requirements (Unless otherwise specified: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc = 3V]

### Table 5.22 XIN Input

Symbol	Parameter -	Standard		Unit
Symbol		Min.	Max.	Unit
tc(XIN)	XIN Input Cycle Time	100	-	ns
twh(XIN)	XIN Input "H" Width	40	-	ns
twl(XIN)	XIN Input "L" Width	40	-	ns

## Table 5.23 CNTR0 Input, CNTR1 Input, INT1 Input

Symbol	Parameter -	Standard		Unit
Symbol		Min.	Max.	Unit
tc(CNTR0)	CNTR0 Input Cycle Time	300	-	ns
tWH(CNTR0)	CNTR0 Input "H" Width	120	-	ns
tWL(CNTR0)	CNTR0 Input "L" Width	120	-	ns

### Table 5.24TCIN Input, INT3 Input

Symbol	Parameter	Standard		Unit
Symbol		Min.	Max.	Unit
tc(TCIN)	TCIN Input Cycle Time	1,200 <sup>(1)</sup>	-	ns
twh(tcin)	TCIN Input "H" Width	600 <sup>(2)</sup>	-	ns
twl(tcin)	TCIN Input "L" Width	600 <sup>(2)</sup>	_	ns

NOTES:

1. When using the Timer C input capture mode, adjust the cycle time (1/Timer C count source frequency x 3) or above.

2. When using the Timer C input capture mode, adjust the width (1/Timer C count source frequency x 1.5) or above.

### Table 5.25 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	Unit
tc(CK)	CLKi Input Cycle Time	300	-	ns
tw(CKH)	CLKi Input "H" Width	150	-	ns
tW(CKL)	CLKi Input "L" Width	150	-	ns
td(C-Q)	TXDi Output Delay Time	-	80	ns
th(C-Q)	TXDi Hold Time	0	-	ns
tsu(D-C)	RXDi Input Setup Time	70	-	ns
th(C-D)	RCDi Input Hold Time	90	_	ns

### Table 5.26 External Interrupt INT0 Input

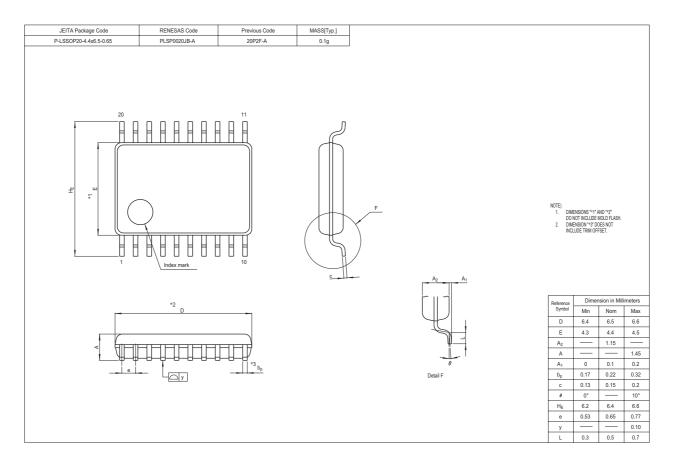
Symbol	Parameter -	Standard		Unit
Symbol		Min.	Max.	Unit
tw(INH)	INTO Input "H" Width	380 <sup>(1)</sup>	-	ns
tw(INL)	INTO Input "L" Width	380(2)	_	ns

NOTES:

1. When selecting the digital filter by the INTO input filter select bit, use the INTO input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

2. When selecting the digital filter by the INTO input filter select bit, use the INTO input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

## Package Dimensions



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