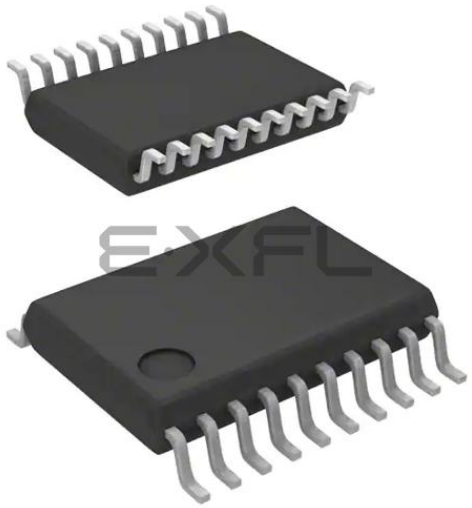
Renesas Electronics America Inc - R5F21153SP#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21153sp-u0

Table 1.2 Performance Outline of the R8C/15 Group

Item		Performance
CPU	Number of Basic Instructions	89 instructions
	Minimum Instruction Execution Time	50ns (f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns (f(XIN)=10MHz, VCC=2.7 to 5.5V)
	Operating Mode	Single-chip
	Memory Space	1 Mbyte
	Memory Capacity	See **Table 1.4 R8C/15 Group Product Information**
Peripheral Function	Port	I/O : 13 pins (including LED drive port), Input : 2 pins
	LED drive port	I/O port: 4 pins
	Timer	Timer X: 8 bits × 1 channel, Timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Circuits of input capture and output compare)
	Serial Interface	1 channel Clock synchronous serial I/O, UART
	Chip-select clock synchronous serial I/O (SSU)	1 channel
	A/D Converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog Timer	15 bits × 1 channel (with prescaler) Reset start selectable, Count source protection mode
	Interrupt	Internal: 9 factors, External: 4 factors, Software: 4 factors Priority level: 7 levels
	Clock Generation Circuit	2 circuits • Main clock generation circuit (Equipped with a built-in feedback resistor) • On-chip oscillator (high speed, low speed) Equipped with frequency adjustment function on high-speed on-chip oscillator
	Oscillation Stop Detection Function	Main clock oscillation stop detection function
	Voltage Detection Circuit	Included
	Power on Reset Circuit	Included
Electric Characteristics	Supply Voltage	VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz)
	Power Consumption	Typ. 9mA (VCC=5.0V, f(XIN)=20MHz) Typ. 5mA (VCC=3.0V, f(XIN)=10MHz) Typ. 35μA (VCC=3.0V, wait mode, peripheral clock off) Typ. 0.7μA (VCC=3.0V, stop mode)
Flash Memory	Program/Erase Supply Voltage	VCC=2.7 to 5.5V
	Program/Erase Endurance	10,000 times (Data flash)
		1,000 times (Program ROM)
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D Version)
Package		20-pin plastic mold LSSOP

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

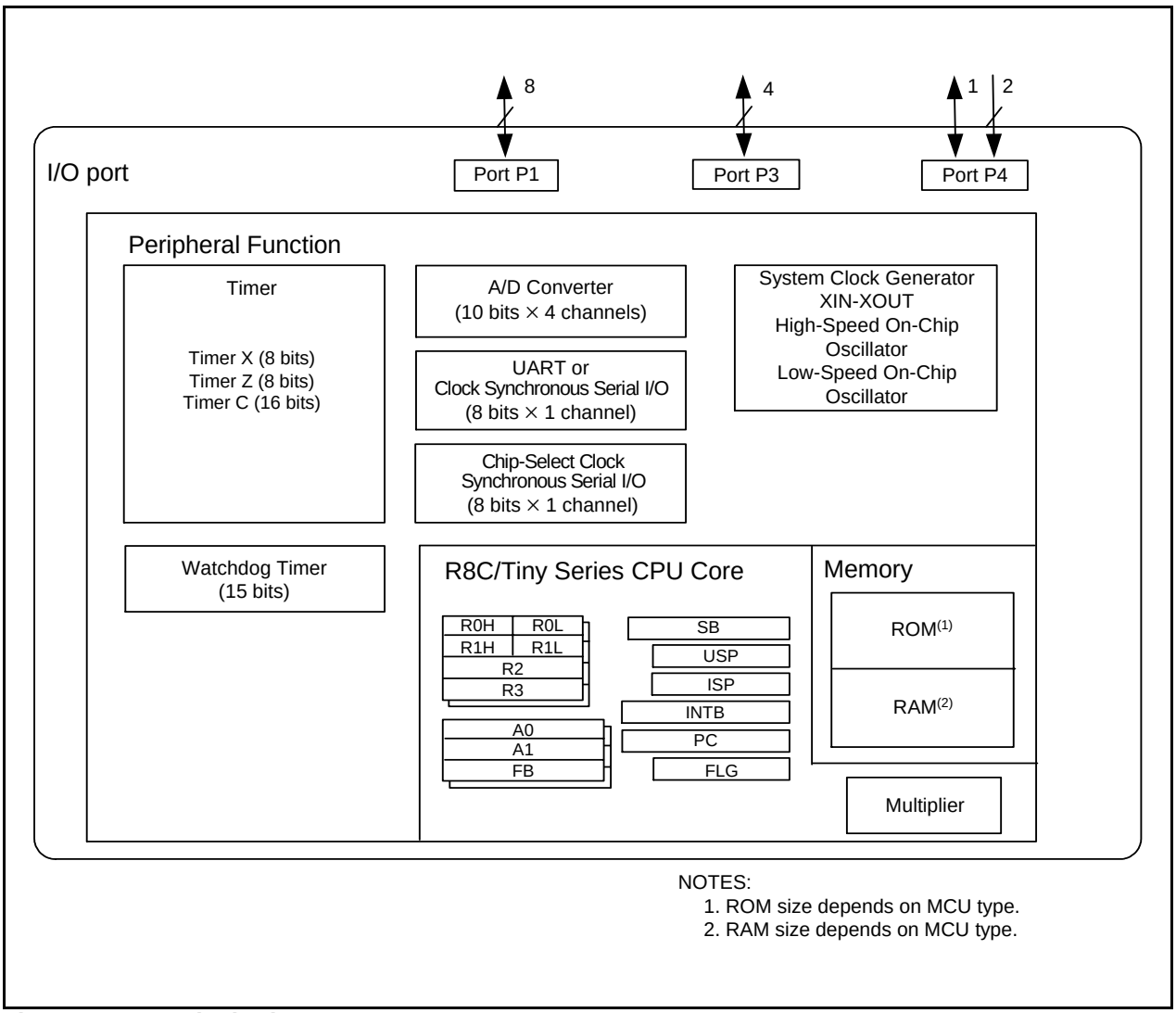


Figure 1.1 Block Diagram

Table 1.4 Product Information of R8C/15 Group **As of Jan 2006**

Type No.	ROM capacity		RAM capacity	Package type	Remarks
	Program ROM	Data flash			
R5F21152SP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	Flash memory version
R5F21153SP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21154SP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F21152DSP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	D version
R5F21153DSP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21154DSP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	

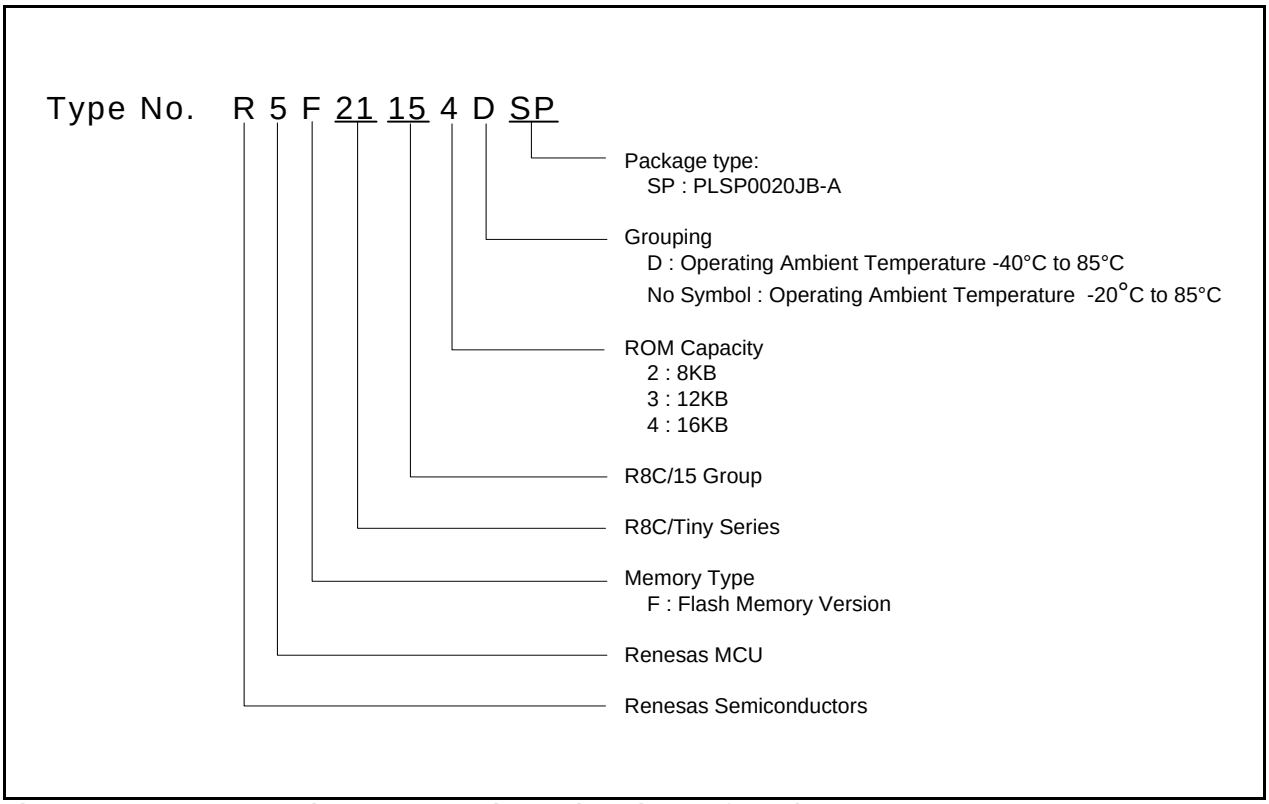


Figure 1.3 Part Number, Memory Size and Package of R8C/15 Group

1.5 Pin Assignments

Figure 1.4 shows the PLSP0020JB-A Package Pin Assignment (top view).

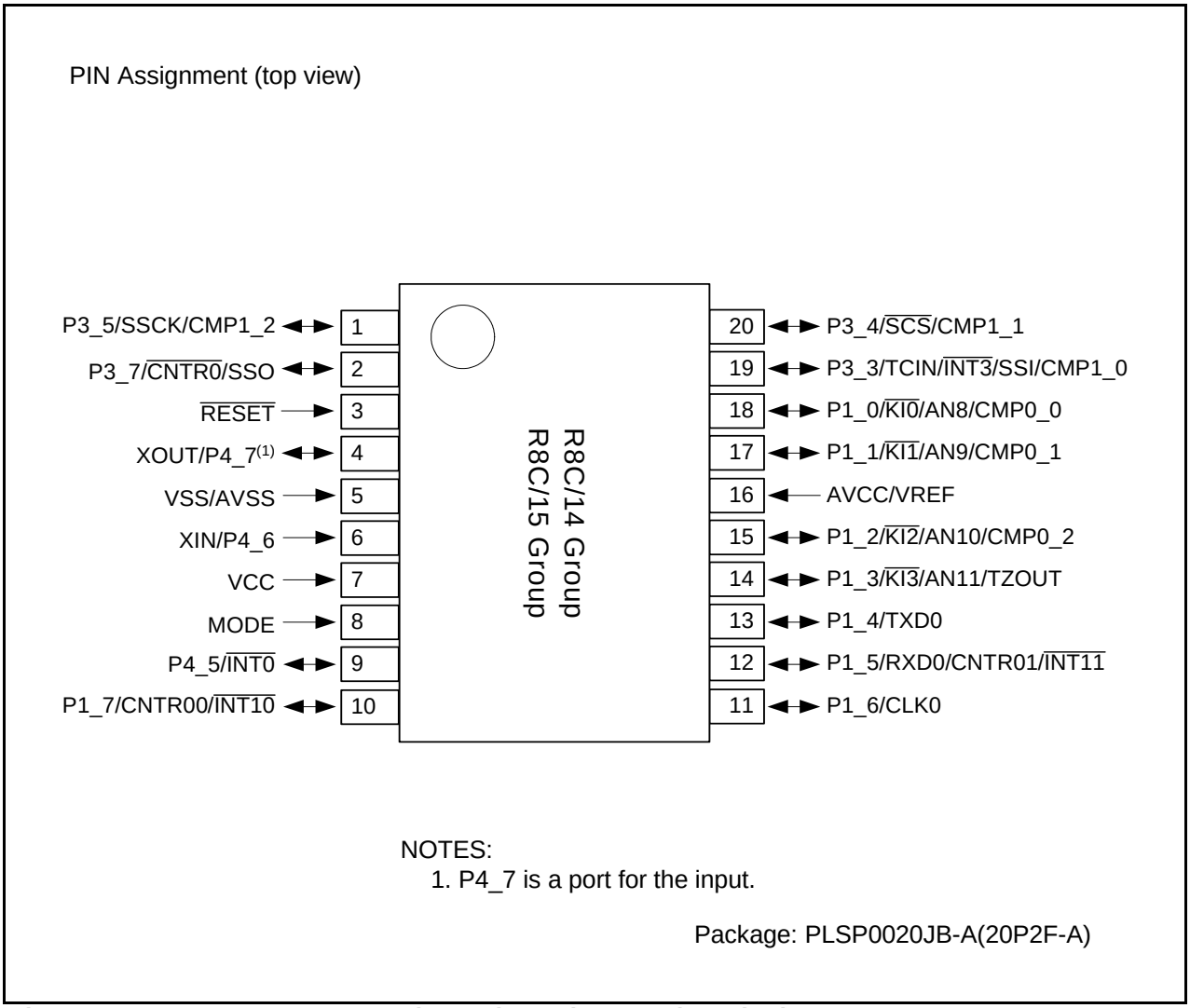


Figure 1.4 PLSP0020JB-A Package Pin Assignment (top view)

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to “0”.

2.8.3 Zero Flag (Z)

The Z flag is set to “1” when an arithmetic operation resulted in 0; otherwise, “0”.

2.8.4 Sign Flag (S)

The S flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, “0”.

2.8.5 Register Bank Select Flag (B)

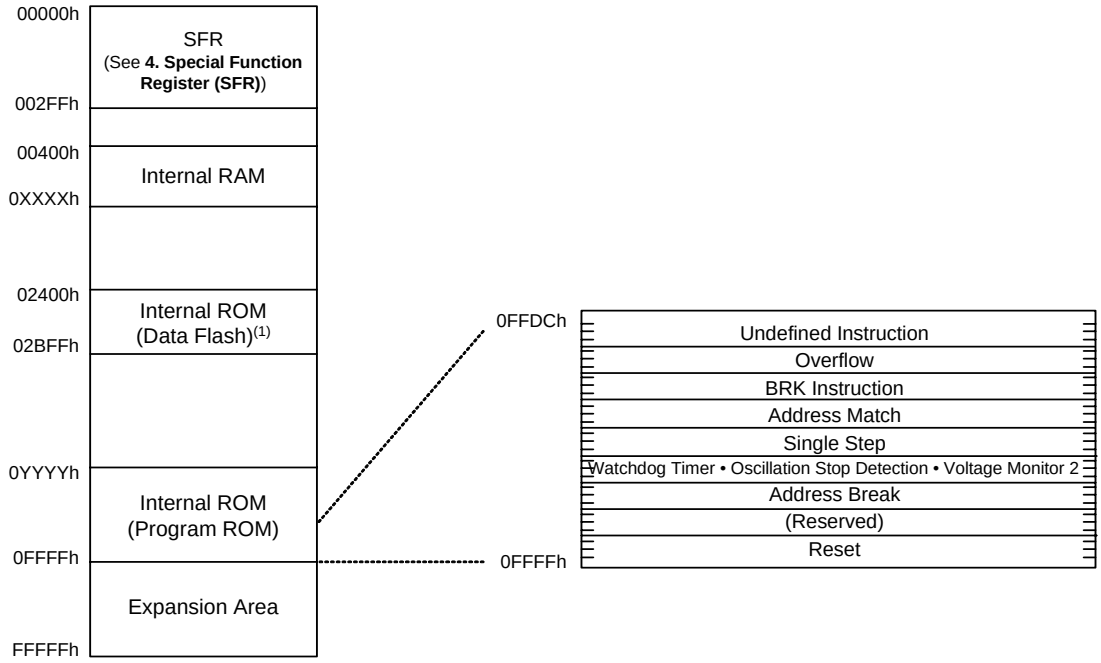
The register bank 0 is selected when the B flag is “0”. The register bank 1 is selected when this flag is set to “1”.

2.8.6 Overflow Flag (O)

The O flag is set to “1” when the operation resulted in an overflow; otherwise, “0”.

3.2 R8C/15 Group

Figure 3.2 is a Memory Map of R8C/15 Group. The R8C/15 group provides 1-Mbyte address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM is allocated higher addresses beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but for calling subroutines and stacks when interrupt request is acknowledged.
Special function registers (SFR) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated them. All addresses, which have nothing allocated within the SFR, are reserved area and cannot be accessed by users.



NOTES:
1. The data flash block A (1 Kbyte) and block B (1 Kbyte) are shown.
2. Blank spaces are reserved. No access is allowed.

Part Number	Internal ROM		Internal RAM	
	Size	0YYYYh	Size	0XXXXh
R5F21154SP, R5F21154DSP	16K bytes	0C000h	1K byte	007FFh
R5F21153SP, R5F21153DSP	12K bytes	0D000h	768 bytes	006FFh
R5F21152SP, R5F21152DSP	8K bytes	0E000h	512 bytes	005FFh

Figure 3.2 Memory Map of R8C/15 Group

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
0080h	Timer Z Mode Register	TZMR	00h
0081h			
0082h			
0083h			
0084h	Timer Z Waveform Output Control Register	PUM	00h
0085h	Prescaler Z Register	PREZ	FFh
0086h	Timer Z Secondary Register	TZSC	FFh
0087h	Timer Z Primary Register	TZPR	FFh
0088h			
0089h			
008Ah	Timer Z Output Control Register	TZOC	00h
008Bh	Timer X Mode Register	TXMR	00h
008Ch	Prescaler X Register	PREX	FFh
008Dh	Timer X Register	TX	FFh
008Eh	Timer Count Source Setting Register	TCSS	00h
008Fh			
0090h	Timer C Register	TC	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h	External Input Enable Register	INTEN	00h
0097h			
0098h	Key Input Enable Register	KIEN	00h
0099h			
009Ah	Timer C Control Register 0	TCC0	00h
009Bh	Timer C Control Register 1	TCC1	00h
009Ch	Capture, Compare 0 Register	TM0	00h
009Dh			00h(2)
009Eh	Compare 1 Register	TM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h	UART Transmit/Receive Control Register 2	UCON	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H	SSCRH	00h
00B9h	SS Control Register L	SSCRL	7Dh
00BAh	SS Mode Register	SSMR	18h
00BBh	SS Enable Register	SSER	00h
00BCh	SS Status Register	SSSR	00h
00BDh	SS Mode Register 2	SSMR2	00h
00BEh	SS Transmit Data Register	SSTDR	FFh
00BFh	SS Receive Data Register	SSRDR	FFh

X: Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.
2. When output compare mode (the TCC13 bit in the TCC1 register = 1) is selected, the value after reset is “FFFFh”.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated value	Unit
V_{CC}	Supply Voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog Supply Voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
V_I	Input Voltage		-0.3 to V_{CC}+0.3	V
V_O	Output Voltage		-0.3 to V_{CC}+0.3	V
P_d	Power Dissipation	T_{opr} = 25°C	300	mW
T_{opr}	Operating Ambient Temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage Temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply Voltage			2.7	–	5.5	V
AV_{CC}	Analog Supply Voltage			–	V_{CC}(3)	–	V
V_{SS}	Supply Voltage			–	0	–	V
AV_{SS}	Analog Supply Voltage			–	0	–	V
V_{IH}	Input “H” Voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” Voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak Sum Output “H” Current	Sum of All Pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak Output “H” Current			–	–	-10	mA
$I_{OH(avg)}$	Average Output “H” Current			–	–	-5	mA
$I_{OL(sum)}$	Peak Sum Output “L” Currents	Sum of All Pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak Output “L” Currents	Except P1_0 to P1_3		–	–	10	mA
		P1_0 to P1_3	Drive Capacity HIGH	–	–	30	mA
			Drive Capacity LOW	–	–	10	mA
$I_{OL(avg)}$	Average Output “L” Current	Except P1_0 to P1_3		–	–	5	mA
		P1_0 to P1_3	Drive Capacity HIGH	–	–	15	mA
			Drive Capacity LOW	–	–	5	mA
$f_{(XIN)}$	Main Clock Input Oscillation Frequency		3.0V ≤ V_{CC} ≤ 5.5V	0	–	20	MHz
			2.7V ≤ V_{CC} < 3.0V	0	–	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. The typical values when average output current is 100ms.
3. Hold V_{CC} = AV_{CC}.

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
–	Resolution		V_{ref} = V_{CC}	–	–	10	Bits
–	Absolute Accuracy	10-Bit Mode	ϕ_{AD} = 10MHz, V_{ref} = V_{CC} = 5.0V	–	–	±3	LSB
		8-Bit Mode	ϕ_{AD} = 10MHz, V_{ref} = V_{CC} = 5.0V	–	–	±2	LSB
		10-Bit Mode	ϕ_{AD} = 10MHz, V_{ref} = V_{CC} = 3.3V(3)	–	–	±5	LSB
		8-Bit Mode	ϕ_{AD} = 10MHz, V_{ref} = V_{CC} = 3.3V(3)	–	–	±2	LSB
R_{ladder}	Resistor Ladder		V_{ref} = V_{CC}	10	–	40	kΩ
t_{conv}	Conversion Time	10-Bit Mode	ϕ_{AD} = 10MHz, V_{ref} = V_{CC} = 5.0V	3.3	–	–	µs
		8-Bit Mode	ϕ_{AD} = 10MHz, V_{ref} = V_{CC} = 5.0V	2.8	–	–	µs
V_{ref}	Reference voltage			–	V_{CC}(4)	–	V
V_{IA}	Analog Input Voltage			0	–	V_{ref}	V
–	A/D Operating Clock Frequency(2)	Without Sample & Hold		0.25	–	10	MHz
		With Sample & Hold		1	–	10	MHz

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f1 exceeds 10MHz, divide the f1 and hold A/D operating clock frequency (ϕ_{AD}) 10MHz or below.
3. If the AVcc is less than 4.2V, divide the f1 and hold A/D operating clock frequency (ϕ_{AD}) f1/2 or below.
4. Hold V_{CC} = V_{ref}

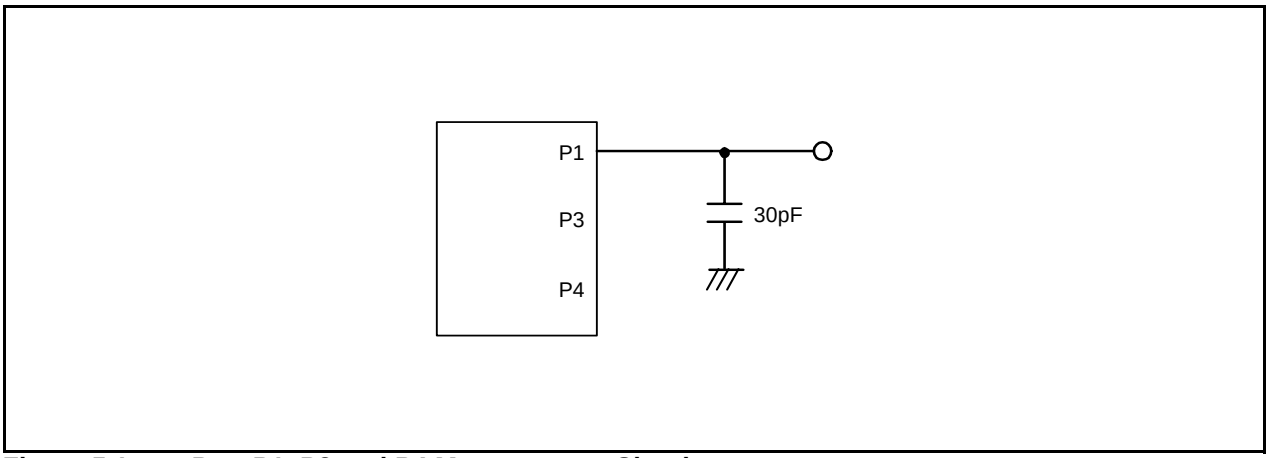


Figure 5.1 Port P1, P3 and P4 Measurement Circuit

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/Erase Endurance(2)		10,000(3)	–	–	times
–	Byte Program Time (Program/Erase Endurance ≤ 1,000 Times)	V_{CC} = 5.0 V at T_{opr} = 25 °C	–	50	400	µs
–	Byte Program Time (Program/Erase Endurance > 1,000 Times)	V_{CC} = 5.0 V at T_{opr} = 25 °C	–	65	–	µs
–	Block Erase Time (Program/Erase Endurance ≤ 1,000 Times)	V_{CC} = 5.0 V at T_{opr} = 25 °C	–	0.2	9	s
–	Block Erase Time (Program/Erase Endurance > 1,000 Times)	V_{CC} = 5.0 V at T_{opr} = 25 °C	–	0.3	–	s
$t_{d(SR-ES)}$	Time Delay from Suspend Request until Erase Suspend		–	–	8	ms
–	Erase Suspend Request Interval		10	–	–	ms
–	Program, Erase Voltage		2.7	–	5.5	V
–	Read Voltage		2.7	–	5.5	V
–	Program, Erase Temperature		-20(8)	–	85	°C
–	Data Hold Time(9)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = AVcc = 2.7 to 5.5V at T_{opr} = –20 to 85 °C / –40 to 85 °C, unless otherwise specified.
2. Definition of program and erase
   The program and erase endurance shows an erase endurance for every block.
   If the program and erase endurance is “n” times (n = 100, 10000), “n” times erase can be performed for every block.
   For example, if performing 1-byte write to the distinct addresses on Block A of 1Kbyte block 1,024 times and then erasing that block, program and erase endurance is counted as one time.
   However, do not perform multiple programs to the same address for one time ease.(disable overwriting).
3. Endurace to guarantee all electrical characteristics after program and erase.(1 to “Min.” value can be guaranateed).
4. Standard of Block A and Block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times aer the same as that in program area.
5. In the case of a system to execute multiple programs, perform one erase after programming as reducing effective reprogram endurance not to leave blank area as possible such as programming write addresses in turn . If programming a set of 16 bytes, programming up to 128 sets and then erasing them one time can reduce effective reprogram endurance. Additionally, averaging erase endurance for Block A and B can reduce effective reprogram endurance more. To leave erase endurance for every block as information and determine the restricted endurance are recommended.
6. If error occurs during block erase, attempt to execute the clear status register command, then the block erase command at least three times until the erase error does not occur.
7. Customers desiring Program/Erase failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time incudes time that the power supply is off or the clock is not supplied.

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

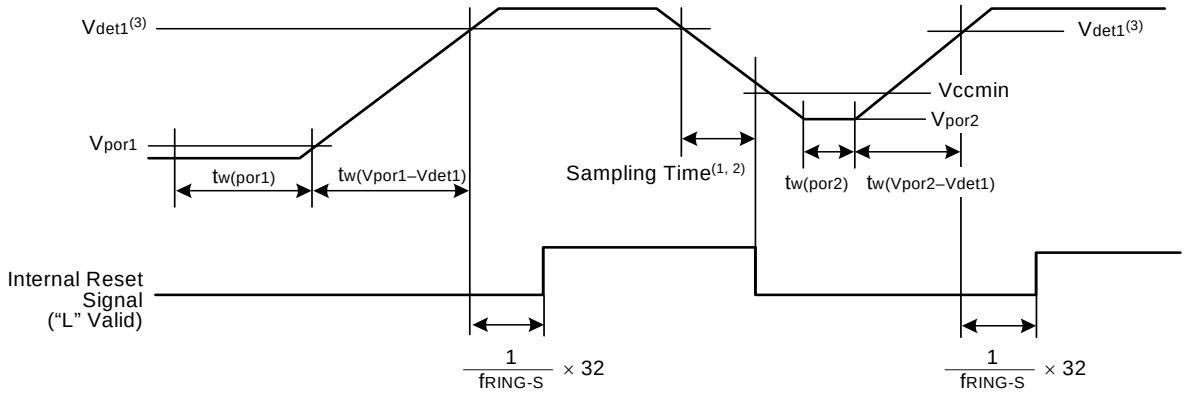
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por2}	Power-On Reset Valid Voltage	-20°C ≤ Topr < 85°C	–	–	V_{det1}	V
$t_{w(Vpor2-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted(1)	-20°C ≤ Topr < 85°C, $t_{w(por2)}$ ≥ 0s(3)	–	–	100	ms

NOTES:
1. This condition is not applicable when using with Vcc ≥ 1.0V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds10s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-On Reset Valid Voltage	-20°C ≤ Topr < 85°C	–	–	0.1	V
$t_{w(Vpor1-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 10s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 30s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 10s(2)	–	–	1	ms
$t_{w(Vpor1-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 1s(2)	–	–	0.5	ms

NOTES:
1. When not using the voltage monitor 1 reset, use with Vcc≥ 2.7V.
2. $t_{w(por1)}$ is time to hold the external power below effective voltage (V_{por1}).



NOTES:
1. Hold the voltage of the microcomputer operation voltage range (Vccmin or above) within sampling time.
2. A sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-Speed On-Chip Oscillator Frequency When the Reset is Deasserted	V_{CC} = 5.0V, T_{opr} = 25 °C	–	8	–	MHz
–	High-Speed On-Chip Oscillator Frequency Temperature • Supplay Voltage Dependence	0 to +60 °C / 5 V ± 5 %(2)	7.44	–	8.56	MHz
		–20 to +85 °C / 2.7 to 5.5 V(2)	7.04	–	8.96	MHz
		–40 to +85 °C / 2.7 to 5.5 V(2)	6.80	–	9.20	MHz

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 5.0V and T_{opr} = 25 °C.
2. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization during Power-On(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP Exit Time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 2.7 to 5.5V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK Clock Cycle Time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK Clock “H” Width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK Clock “L” Width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK Clock Rising Time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK Clock Falling Time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI Data Input Setup Time			100	–	–	ns
t_{H}	SSO, SSI Data Input Hold Time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ Setup Time	Slave		1t_{CYC}+50	–	–	ns
t_{LAG}	$\overline{SCS}$ Hold Time	Slave		1t_{CYC}+50	–	–	ns
t_{OD}	SSO, SSI Data Output Delay Time			–	–	1	t_{CYC}(2)
t_{SA}	SSI Slave Access Time			–	–	1.5t_{CYC}+100	ns
t_{OR}	SSI Slave Out Open Time			–	–	1.5t_{CYC}+100	ns

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V, V_{SS} = 0V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

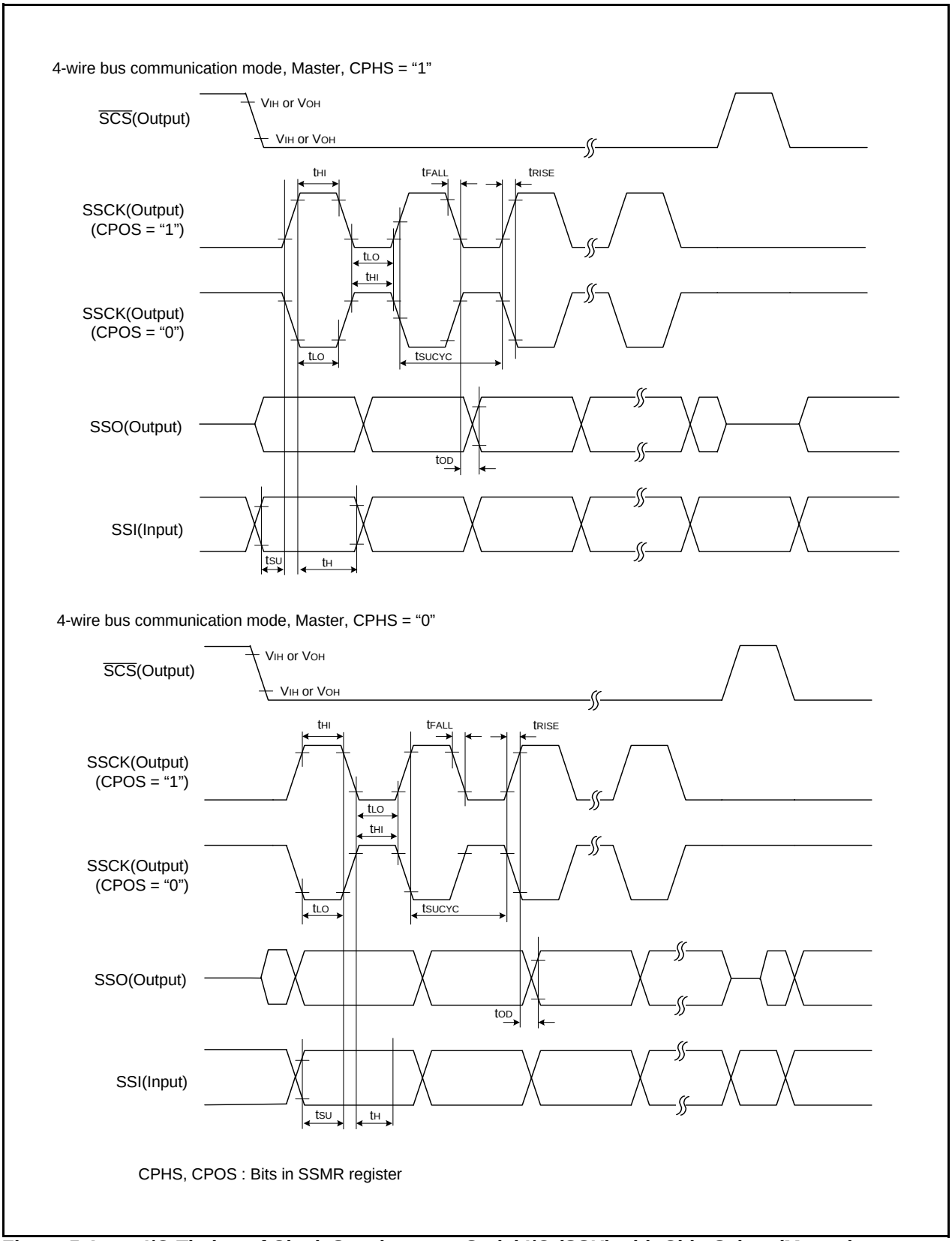


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Master)

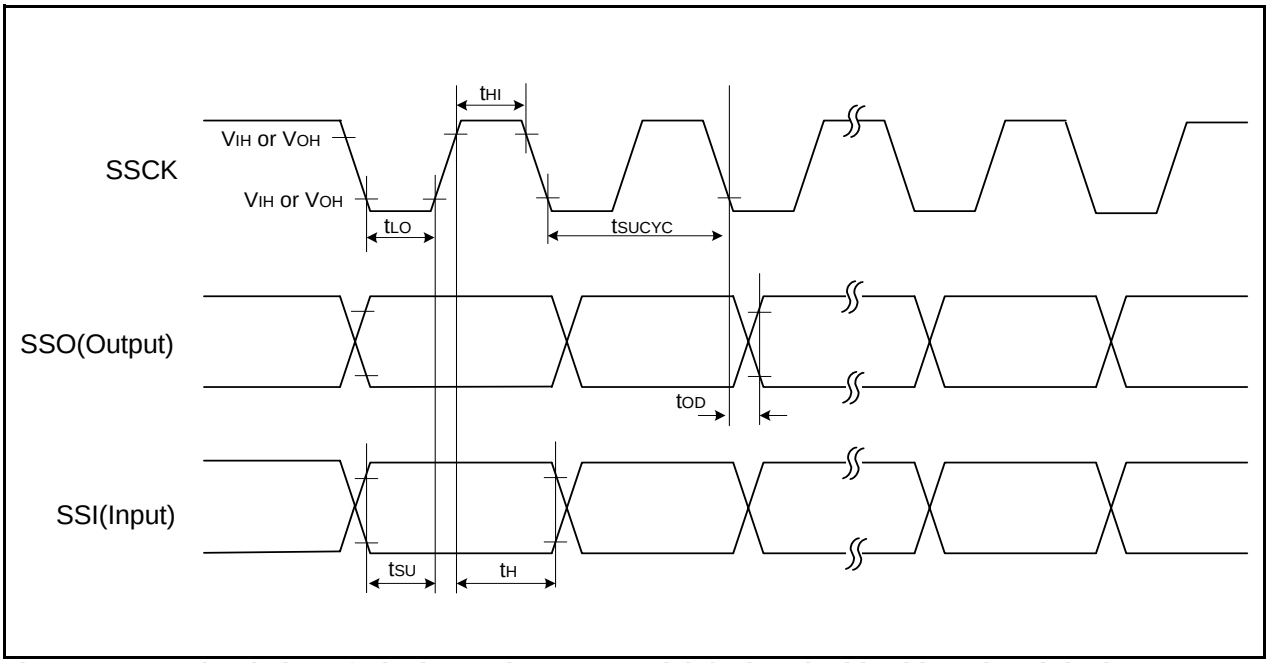


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Clock Synchronous Communication Mode)

Timing Requirements (Unless otherwise specified: Vcc = 5V, Vss = 0V at Topr = 25 °C) [Vcc = 5V]

Table 5.15 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN Input Cycle Time	50	–	ns
$t_{WH(XIN)}$	XIN Input “H” Width	25	–	ns
$t_{WL(XIN)}$	XIN Input “L” Width	25	–	ns

Table 5.16 CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 Input Cycle Time	100	–	ns
$t_{WH(CNTR0)}$	CNTR0 Input “H” Width	40	–	ns
$t_{WL(CNTR0)}$	CNTR0 input “L” Width	40	–	ns

Table 5.17 TCIN Input, $\overline{INT3}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN Input Cycle Time	400(1)	–	ns
$t_{WH(TCIN)}$	TCIN Input “H” Width	200(2)	–	ns
$t_{WL(TCIN)}$	TCIN input “L” Width	200(2)	–	ns

NOTES:
1. When using Timer C input capture mode, adjust the cycle time (1/Timer C count source frequency x 3) or above.
2. When using Timer C input capture mode, adjust the width (1/Timer C count source frequency x 1.5) or above.

Table 5.18 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200	–	ns
$t_{W(CKH)}$	CLKi Input “H” Width	100	–	ns
$t_{W(CKL)}$	CLKi Input “L” Width	100	–	ns
$t_{d(C-Q)}$	TXDi Output Delay Time	–	50	ns
$t_{h(C-Q)}$	TXDi Hold Time	0	–	ns
$t_{su(D-C)}$	RXDi Input Setup Time	50	–	ns
$t_{h(C-D)}$	RCDi Input Hold Time	90	–	ns

Table 5.19 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ Input “H” Width	250(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ Input “L” Width	250(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

Timing requirements (Unless otherwise specified: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc = 3V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN Input Cycle Time	100	–	ns
$t_{WH(XIN)}$	XIN Input “H” Width	40	–	ns
$t_{WL(XIN)}$	XIN Input “L” Width	40	–	ns

Table 5.23 CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 Input Cycle Time	300	–	ns
$t_{WH(CNTR0)}$	CNTR0 Input “H” Width	120	–	ns
$t_{WL(CNTR0)}$	CNTR0 Input “L” Width	120	–	ns

Table 5.24 TCIN Input, $\overline{INT3}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN Input Cycle Time	1,200(1)	–	ns
$t_{WH(TCIN)}$	TCIN Input “H” Width	600(2)	–	ns
$t_{WL(TCIN)}$	TCIN Input “L” Width	600(2)	–	ns

NOTES:
1. When using the Timer C input capture mode, adjust the cycle time (1/Timer C count source frequency x 3) or above.
2. When using the Timer C input capture mode, adjust the width (1/Timer C count source frequency x 1.5) or above.

Table 5.25 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	300	–	ns
$t_{W(CKH)}$	CLKi Input “H” Width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” Width	150	–	ns
$t_{d(C-Q)}$	TXDi Output Delay Time	–	80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0	–	ns
$t_{su(D-C)}$	RXDi Input Setup Time	70	–	ns
$t_{h(C-D)}$	RCDi Input Hold Time	90	–	ns

Table 5.26 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ Input “H” Width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ Input “L” Width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

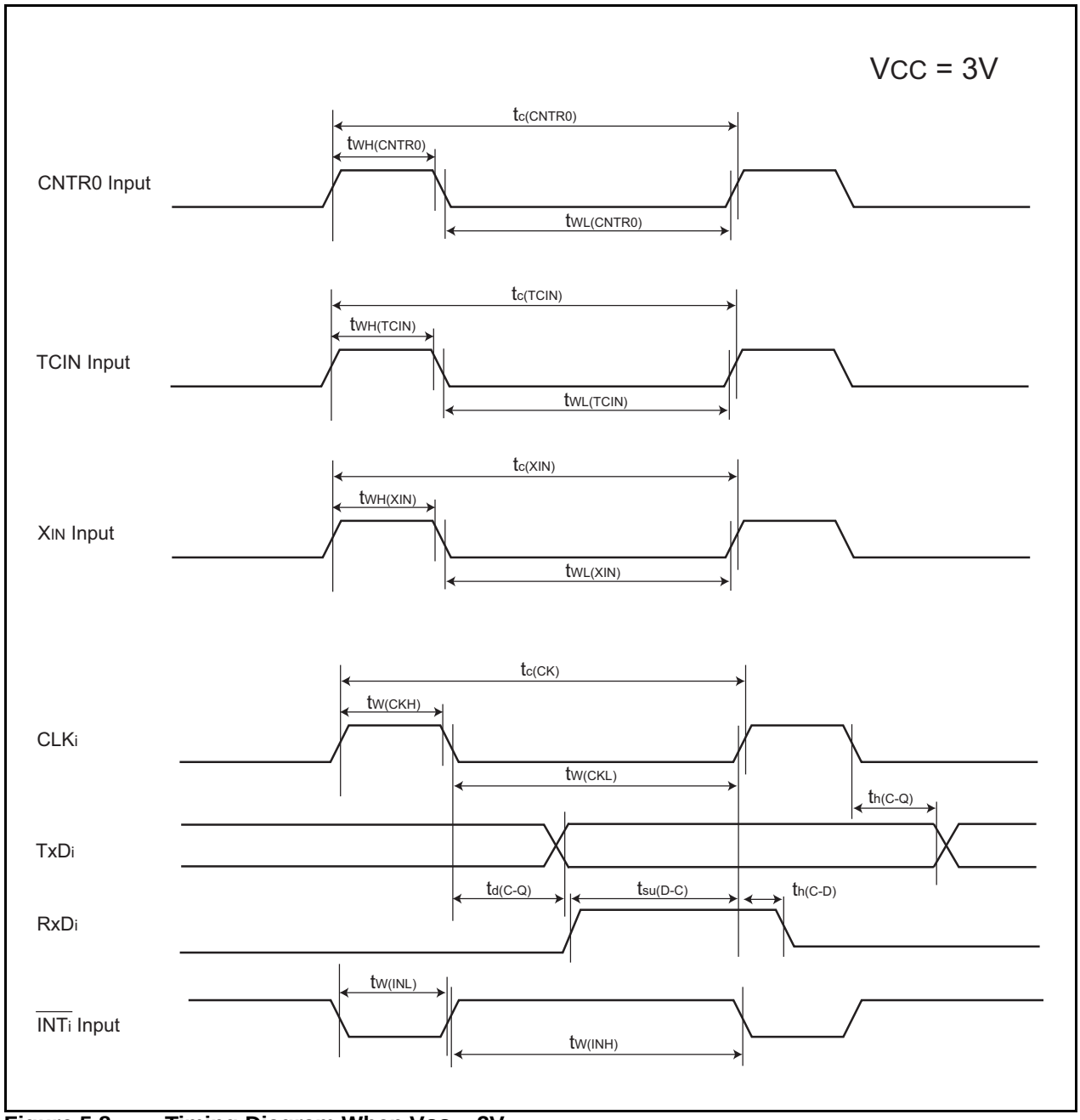
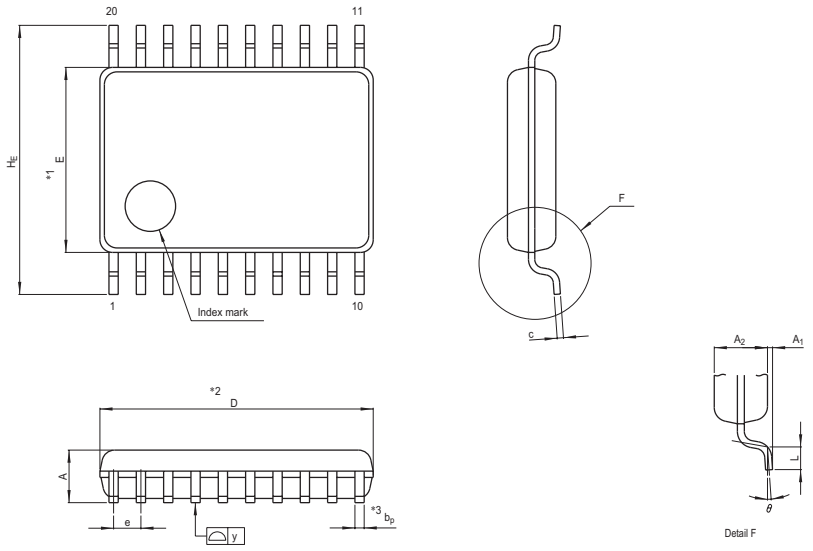


Figure 5.8 Timing Diagram When Vcc = 3V

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	——	1.15	——
A	——	——	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	——	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	——	——	0.10
L	0.3	0.5	0.7

REVISION HISTORY	R8C/14 Group, R8C/15 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Jan 30, 2006	8	Figure 1.5 PRDP0020BA-A Package Pin Assignment (top view) deleted Table 1.5 Pin Description; Timer C: "CMP0_0 to CMP0_3, CMP1_0 to CMP1_3" → "CMP0_0 to CMP0_2, CMP1_0 to CMP1_2" revised
		10	Figure 2.1 CPU Register; "Reserved Area" → "Reserved Bit" revised
		12	2.8.10 Reserved Area; "Reserved Area" → "Reserved Bit" revised
		13	Figure 3.1 Memory Map of R8C/14 Group revised
		14	3.2 R8C/15 Group; "(data area)" → "(data flash)", "(program area)" → "(program ROM)" revised Figure 3.2 Memory Map of R8C/15 Group revised
		15	Table 4.1 SFR Information(1); 0009h: "XXXXXX00b" → "00h" 000Ah: "00XXX000b" → "00h" 001Eh: "XXXXX000b" → "00h"
		17	Table 4.3 SFR Information(3); 0085h: "Prescaler Z" → "Prescaler Z Register" 0086h: "Timer Z Secondary" → "Timer Z Secondary Register" 0087h: "Timer Z Primary" → "Timer Z Primary Register" 008Ch: "Prescaler X" → "Prescaler X Register" 008Dh: "Timer X" → "Timer X Register" 0090h, 0091h: "Timer C" → "Timer C Register" revised
		21	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; • NOTES 1 to 7 added • "Topr" → "Ambient temperature", "Program area" → "Program ROM" revised
		22	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; • NOTE1 revised, NOTE9 added • "Topr" → "Ambient temperature", "Data area" → "Data flash" revised
		23	Figure 5.2 Time delay from Suspend Request until Erase Suspend revised
		24	Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset); NOTE2 revised Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset); NOTE1 revised
		25	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; revised Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select; revised
		30	Table 5.14 Electrical Characteristics (2) [Vcc = 5V]; revised
		31	"Timing Requirements (Unless ... at Ta = 25°C) [VCC = 5V]" → "Timing Requirements (Unless ... at Topr = 25°C) [VCC = 5V]" revised Table 5.18 Serial Interface; "35" → "50", "80" → "50"
		34	Table 5.21 Electrical Characteristics (4) [Vcc = 3V]; revised
		35	"Timing requirements (Unless ... at Ta = 25°C) [VCC = 3V]" → "Timing requirements (Unless ... at Topr = 25°C) [VCC = 3V]" revised Table 5.25 Serial Interface; "55" → "70", "160" → "80"
		37	Package Dimensions; Package "PRDP0020BA-A" deleted

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