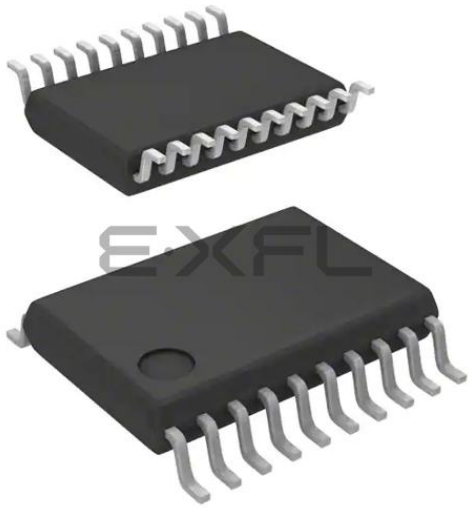

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, SSU, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21154sp-u0

1. Overview

This MCU is built using the high-performance silicon gate CMOS process using a R8C/Tiny Series CPU core and is packaged in a 20-pin plastic molded LSSOP. This MCU operates using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, it is capable of executing instructions at high speed.
Furthermore, the data flash ROM (1KB × 2blocks) is embedded in the R8C/15 group.
The difference between R8C/14 and R8C/15 groups is only the existence of the data flash ROM. Their peripheral functions are the same.

1.1 Applications

Electric household appliance, office equipment, housing equipment (sensor, security), general industrial equipment, audio, etc.

1.2 Performance Overview

Table 1.1 lists the Performance Outline of the R8C/14 Group and Table 1.2 lists the Performance Outline of the R8C/15 Group.

Table 1.1 Performance Outline of the R8C/14 Group

Item		Performance
CPU	Number of Basic Instructions	89 instructions
	Minimum Instruction Execution Time	50ns(f(XIN)=20MHz, VCC=3.0 to 5.5V) 100ns(f(XIN)=10MHz, VCC=2.7 to 5.5V)
	Operating Mode	Single-chip
	Memory Space	1 Mbyte
	Memory Capacity	See **Table 1.3 R8C/14 Group Product Information**
Peripheral Function	Port	I/O port : 13 pins (including LED drive port), Input : 2 pins
	LED Drive Port	I/O port: 4 pins
	Timer	Timer X: 8 bits × 1 channel, Timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Circuits of input capture and output compare)
	Serial Interface	1 channel Clock synchronous serial I/O, UART
	Chip-Select Clock Synchronous Serial I/O (SSU)	1 channel
	A/D Converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog Timer	15 bits ×1 channel (with prescaler) Reset start selectable, Count source protection mode
	Interrupt	Internal: 9 factors, External: 4 factors, Software: 4 factors, Priority level: 7 levels
	Clock Generation Circuit	2 circuits • Main clock oscillation circuit (Equipped with a built-in feedback resistor) • On-chip oscillator (high speed, low speed) Equipped with frequency adjustment function on high-speed on-chip oscillator
	Oscillation Stop Detection Function	Main clock oscillation stop detection function
	Voltage Detection Circuit	Included
	Power-On Reset Circuit	Included
Electric Characteristics	Supply Voltage	VCC=3.0 to 5.5V (f(XIN)=20MHz) VCC=2.7 to 5.5V (f(XIN)=10MHz)
	Power Consumption	Typ. 9mA (VCC=5.0V, f(XIN)=20MHz) Typ. 5mA (VCC=3.0V, f(XIN)=10MHz) Typ. 35μA (VCC=3.0V, wait mode, peripheral clock off) Typ. 0.7μA (VCC=3.0V, stop mode)
Flash Memory	Program/Erase Supply Voltage	VCC=2.7 to 5.5V
	Program/Erase Endurance	100 times
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D Version)
Package		20-pin plastic mold LSSOP

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

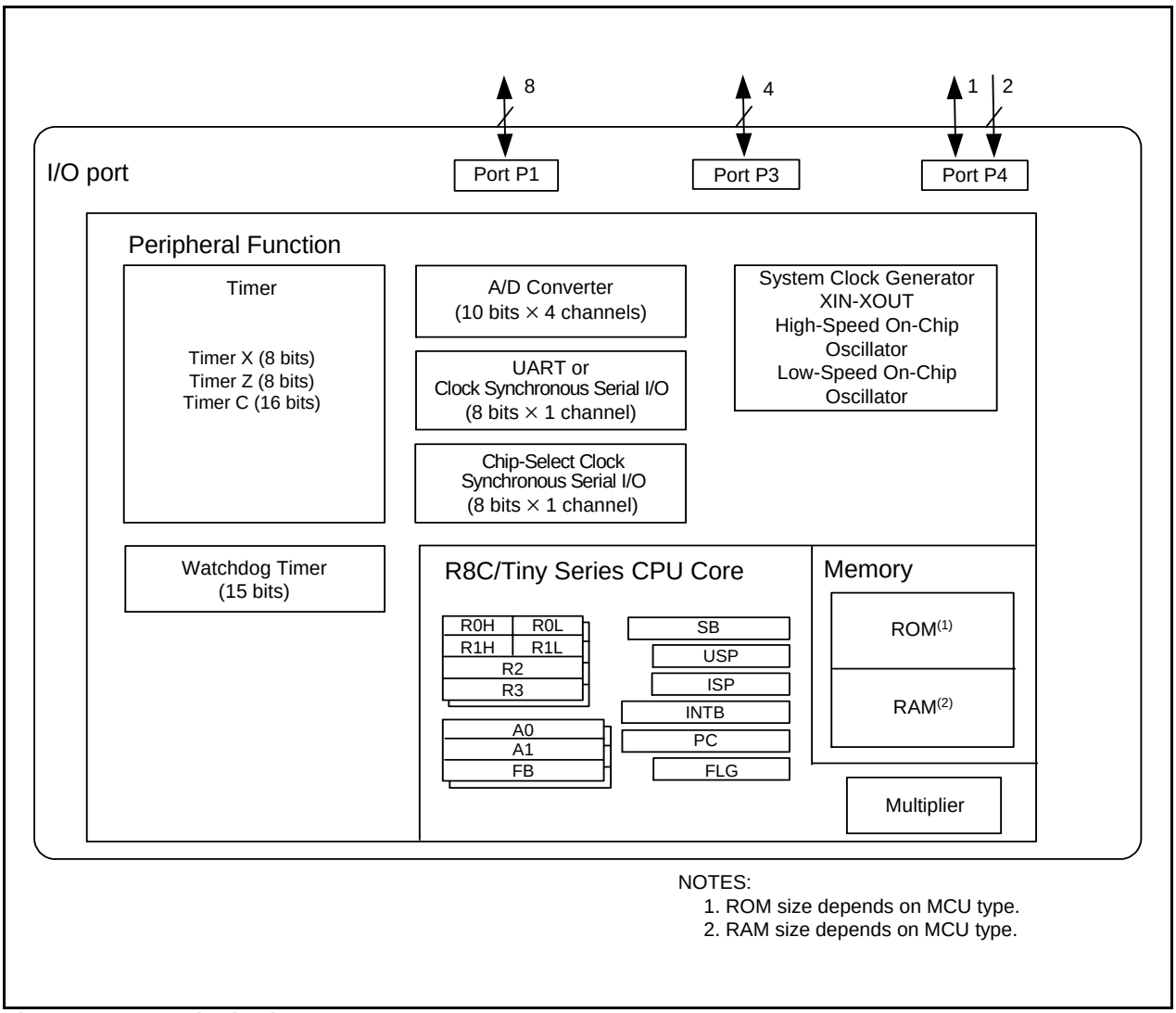


Figure 1.1 Block Diagram

1.5 Pin Assignments

Figure 1.4 shows the PLSP0020JB-A Package Pin Assignment (top view).

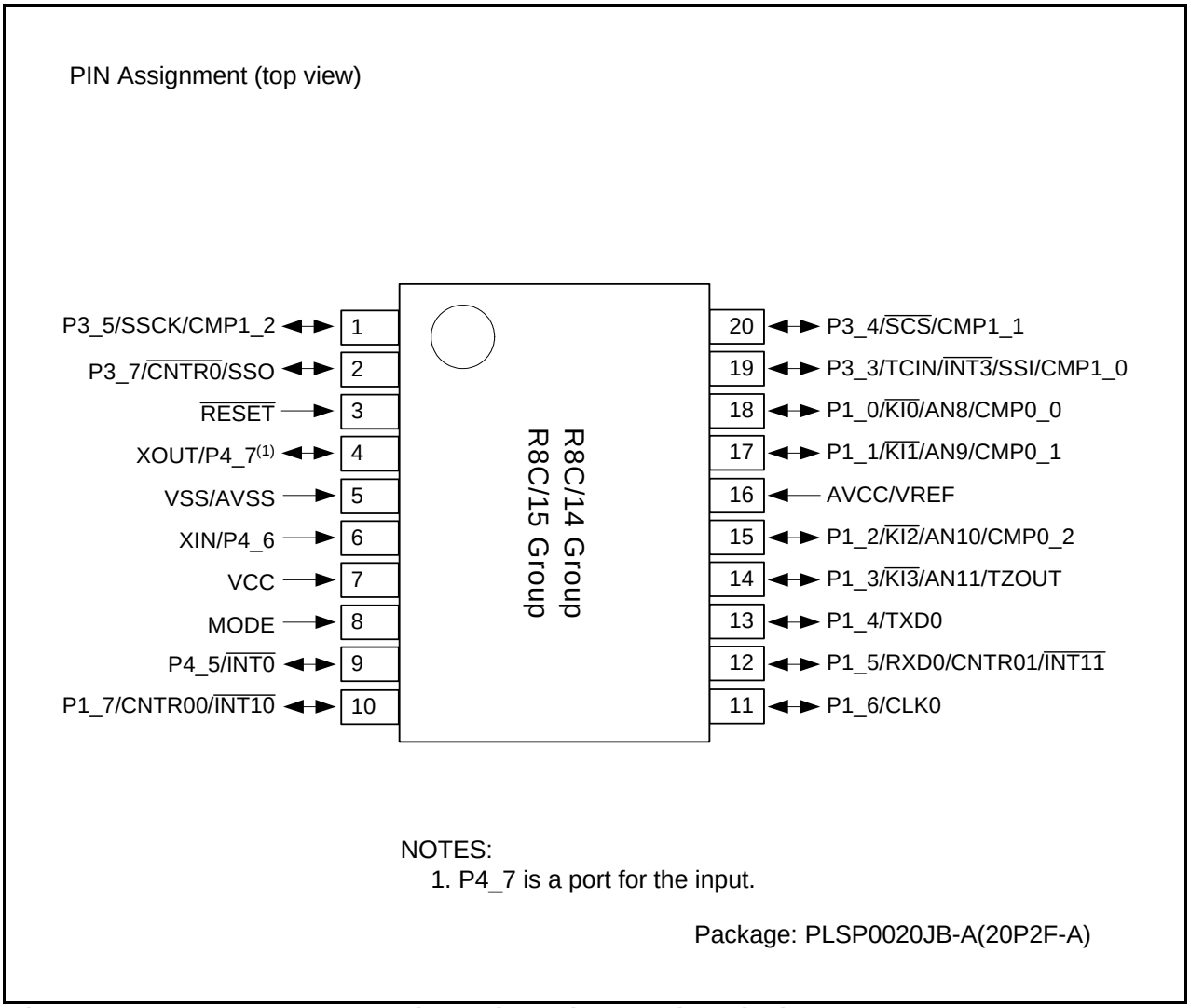


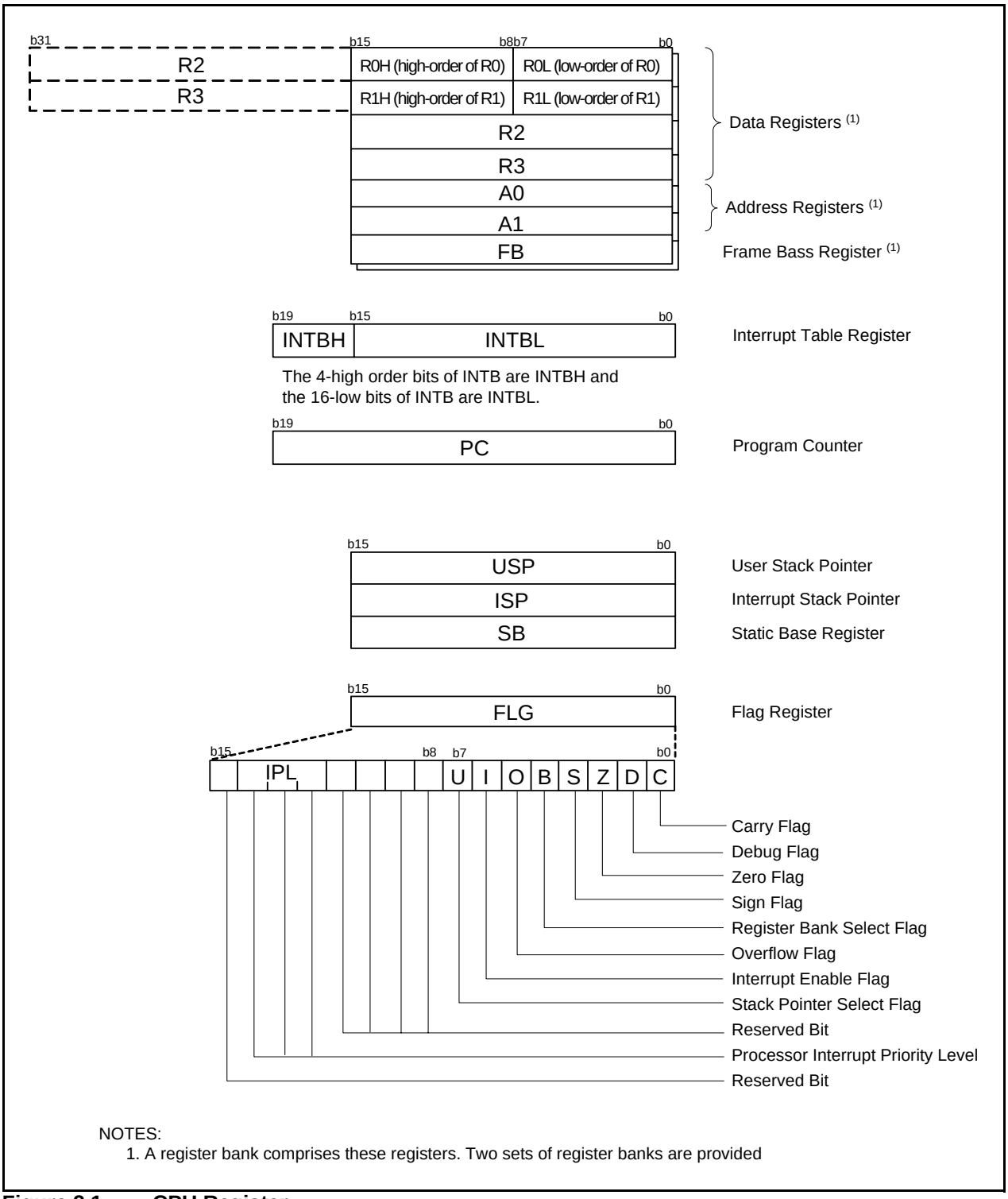
Figure 1.4 PLSP0020JB-A Package Pin Assignment (top view)

Table 1.6 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin of Peripheral Function				
			Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	A/D Converter
1		P3_5		CMP1_2		SSCK	
2		P3_7		$\overline{\text{CNTR0}}$		SSO	
3	$\overline{\text{RESET}}$						
4	XOUT	P4_7					
5	VSS/AVSS						
6	XIN	P4_6					
7	VCC						
8	MODE						
9		P4_5	$\overline{\text{INT0}}$				
10		P1_7	$\overline{\text{INT10}}$	CNTR00			
11		P1_6			CLK0		
12		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0		
13		P1_4			TXD0		
14		P1_3	$\overline{\text{KI3}}$	TZOUT			AN11
15		P1_2	$\overline{\text{KI2}}$	CMP0_2			AN10
16	AVCC/VREF						
17		P1_1	$\overline{\text{KI1}}$	CMP0_1			AN9
18		P1_0	$\overline{\text{KI0}}$	CMP0_0			AN8
19		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0		SSI	
20		P3_4		CMP1_1		$\overline{\text{SCS}}$	

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Register. The CPU contains 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. Two sets of register banks are provided.



NOTES:
1. A register bank comprises these registers. Two sets of register banks are provided

Figure 2.1 CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

R0 is a 16-bit register for transfer, arithmetic and logic operations. The same applies to R1 to R3. The R0 can be split into high-order bit (R0H) and low-order bit (R0L) to be used separately as 8-bit data registers. The same applies to R1H and R1L as R0H and R0L. R2 can be combined with R0 to be used as a 32-bit data register (R2R0). The same applies to R3R1 as R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. They also are used for transfer, arithmetic and logic operations. The same applies to A1 as A0. A0 can be combined with A0 to be used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC, 20 bits wide, indicates the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP and ISP, are 16 bits wide each. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is a 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic logic unit.

2.8.2 Debug Flag (D)

The D flag is for debug only. Set to “0”.

2.8.3 Zero Flag (Z)

The Z flag is set to “1” when an arithmetic operation resulted in 0; otherwise, “0”.

2.8.4 Sign Flag (S)

The S flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, “0”.

2.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is “0”. The register bank 1 is selected when this flag is set to “1”.

2.8.6 Overflow Flag (O)

The O flag is set to “1” when the operation resulted in an overflow; otherwise, “0”.

2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables a maskable interrupt.
An interrupt is disabled when the I flag is set to “0”, and are enabled when the I flag is set to “1”. The I flag is set to “0” when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is set to “0”, USP is selected when the U flag is set to “1”.
The U flag is set to “0” when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

When write to this bit, set to “0”. When read, its content is indeterminate.

4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. Tables 4.1 to 4.4 list the SFR information.

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00011111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	$\overline{\text{INT0}}$ Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 01000000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register [2]	VW1C	0000X000b[3] 0100X001b[4]
0037h	Voltage Monitor 2 Circuit Control Register [5]	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.
2. Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect this register.
3. Owing to Hardware reset.
4. Owing to Power-on reset or the voltage monitor 1 reset.
5. Software reset, the watchdog timer reset or the voltage monitor 2 reset does not affect the b2 and b3.

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
0080h	Timer Z Mode Register	TZMR	00h
0081h			
0082h			
0083h			
0084h	Timer Z Waveform Output Control Register	PUM	00h
0085h	Prescaler Z Register	PREZ	FFh
0086h	Timer Z Secondary Register	TZSC	FFh
0087h	Timer Z Primary Register	TZPR	FFh
0088h			
0089h			
008Ah	Timer Z Output Control Register	TZOC	00h
008Bh	Timer X Mode Register	TXMR	00h
008Ch	Prescaler X Register	PREX	FFh
008Dh	Timer X Register	TX	FFh
008Eh	Timer Count Source Setting Register	TCSS	00h
008Fh			
0090h	Timer C Register	TC	00h
0091h			00h
0092h			
0093h			
0094h			
0095h			
0096h	External Input Enable Register	INTEN	00h
0097h			
0098h	Key Input Enable Register	KIEN	00h
0099h			
009Ah	Timer C Control Register 0	TCC0	00h
009Bh	Timer C Control Register 1	TCC1	00h
009Ch	Capture, Compare 0 Register	TM0	00h
009Dh			00h(2)
009Eh	Compare 1 Register	TM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
00B0h	UART Transmit/Receive Control Register 2	UCON	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H	SSCRH	00h
00B9h	SS Control Register L	SSCRL	7Dh
00BAh	SS Mode Register	SSMR	18h
00BBh	SS Enable Register	SSER	00h
00BCh	SS Status Register	SSSR	00h
00BDh	SS Mode Register 2	SSMR2	00h
00BEh	SS Transmit Data Register	SSTDR	FFh
00BFh	SS Receive Data Register	SSRDR	FFh

X: Undefined

NOTES:

1. Blank spaces are reserved. No access is allowed.
2. When output compare mode (the TCC13 bit in the TCC1 register = 1) is selected, the value after reset is “FFFFh”.

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			XXh
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00000XXXb
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h			
00E1h	Port P1 Register	P1	XXh
00E2h			
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh	Pull-Up Control Register 0	PUR0	00XX0000b
00FDh	Pull-Up Control Register 1	PUR1	XXXXXX0Xb
00FEh	Port P1 Drive Capacity Control Register	DRR	00h
00FFh	Timer C Output Control Register	TCOUT	00h
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
0FFFFh	Optional Function Select Register	OFS	(2)

X: Undefined

NOTES:

1. Blank columns, 0100h to 01B2h and 01B8h to 02FFh are all reserved. No access is allowed.
2. The OFS register cannot be changed by program. Use a flash programmer to write to it.

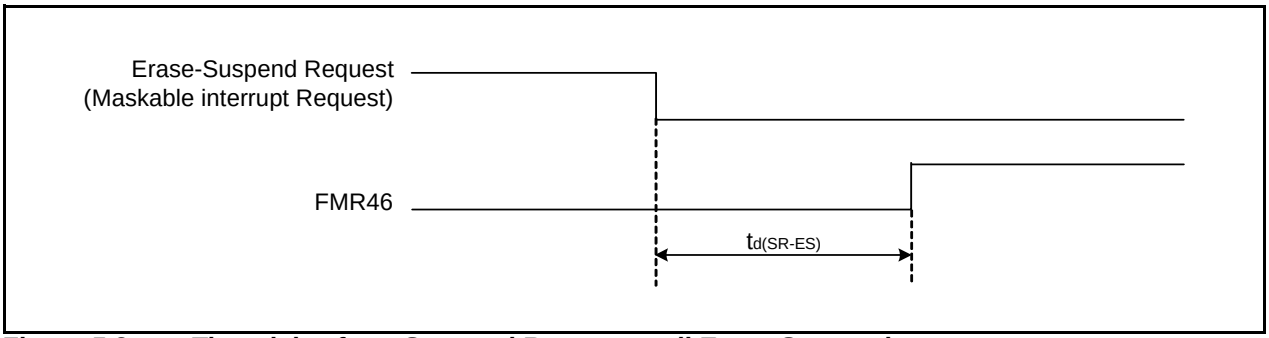


Figure 5.2 Time delay from Suspend Request until Erase Suspend

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage Detection Level(3)		2.70	2.85	3.00	V
–	Voltage Detection Circuit Self Power Consumption	VCA26 = 1, V_{CC} = 5.0V	–	600	–	nA
$t_{d(E-A)}$	Waiting Time until Voltage Detection Circuit Operation Starts(2)		–	–	100	µs
Vccmin	Microcomputer Operating Voltage Minimum Value		2.7	–	–	V

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 2.7V to 5.5V and T_{opr} = -40°C to 85 °C.
2. Necessary time until the voltage detection circuit operates when setting to “1” again after setting the VCA26 bit in the VCA2 register to “0”.
3. Hold $V_{det2} > V_{det1}$.

Table 5.7 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage Detection Level(4)		3.00	3.30	3.60	V
–	Voltage Monitor 2 Interrupt Request Generation Time(2)		–	40	–	µs
–	Voltage Detection Circuit Self Power Consumption	VCA27 = 1, V_{CC} = 5.0V	–	600	–	nA
$t_{d(E-A)}$	Waiting Time until Voltage Detection Circuit Operation Starts(3)		–	–	100	µs

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 2.7V to 5.5V and T_{opr} = -40°C to 85 °C.
2. Time until the voltage monitor 2 interrupt request is generated since the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to “1” again after setting the VCA27 bit in the VCA2 register to “0”.
4. Hold $V_{det2} > V_{det1}$.

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

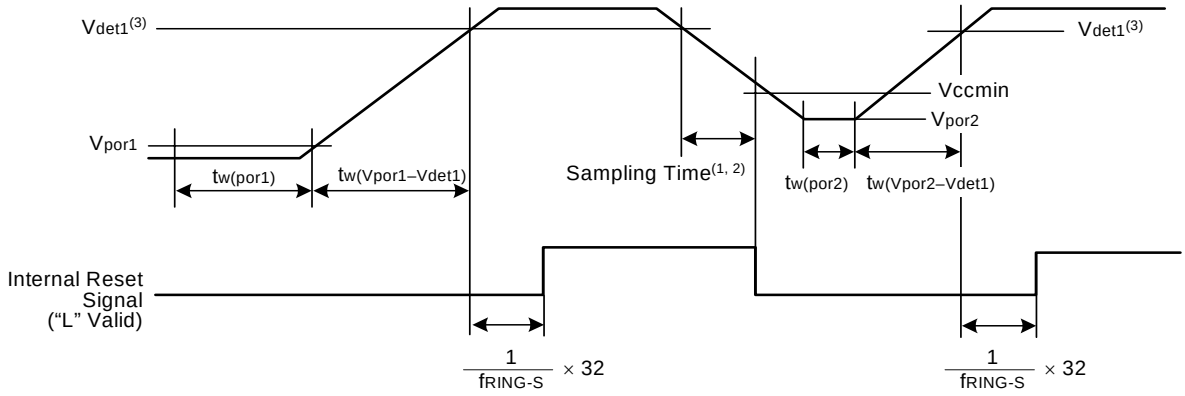
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por2}	Power-On Reset Valid Voltage	-20°C ≤ Topr < 85°C	–	–	V_{det1}	V
$t_{w(Vpor2-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted(1)	-20°C ≤ Topr < 85°C, $t_{w(por2)}$ ≥ 0s(3)	–	–	100	ms

NOTES:
1. This condition is not applicable when using with Vcc ≥ 1.0V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds10s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-On Reset Valid Voltage	-20°C ≤ Topr < 85°C	–	–	0.1	V
$t_{w(Vpor1-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 10s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 30s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 10s(2)	–	–	1	ms
$t_{w(Vpor1-Vdet1)}$	Supply Voltage Rising Time When Power-On Reset is Deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 1s(2)	–	–	0.5	ms

NOTES:
1. When not using the voltage monitor 1 reset, use with Vcc≥ 2.7V.
2. $t_{w(por1)}$ is time to hold the external power below effective voltage (V_{por1}).



NOTES:
1. Hold the voltage of the microcomputer operation voltage range (Vccmin or above) within sampling time.
2. A sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-Speed On-Chip Oscillator Frequency When the Reset is Deasserted	V_{CC} = 5.0V, T_{opr} = 25 °C	–	8	–	MHz
–	High-Speed On-Chip Oscillator Frequency Temperature • Supplay Voltage Dependence	0 to +60 °C / 5 V ± 5 %(2)	7.44	–	8.56	MHz
		–20 to +85 °C / 2.7 to 5.5 V(2)	7.04	–	8.96	MHz
		–40 to +85 °C / 2.7 to 5.5 V(2)	6.80	–	9.20	MHz

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 5.0V and T_{opr} = 25 °C.
2. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for Internal Power Supply Stabilization during Power-On(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP Exit Time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = AV_{CC} = 2.7 to 5.5V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts since the interrupt is acknowledged to exit stop mode.

Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select(1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK Clock Cycle Time			4	–	–	t_{CYC}(2)
t_{HI}	SSCK Clock “H” Width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK Clock “L” Width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK Clock Rising Time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{FALL}	SSCK Clock Falling Time	Master		–	–	1	t_{CYC}(2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI Data Input Setup Time			100	–	–	ns
t_{H}	SSO, SSI Data Input Hold Time			1	–	–	t_{CYC}(2)
t_{LEAD}	$\overline{SCS}$ Setup Time	Slave		1t_{CYC}+50	–	–	ns
t_{LAG}	$\overline{SCS}$ Hold Time	Slave		1t_{CYC}+50	–	–	ns
t_{OD}	SSO, SSI Data Output Delay Time			–	–	1	t_{CYC}(2)
t_{SA}	SSI Slave Access Time			–	–	1.5t_{CYC}+100	ns
t_{OR}	SSI Slave Out Open Time			–	–	1.5t_{CYC}+100	ns

NOTES:
1. V_{CC} = AV_{CC} = 2.7 to 5.5V, V_{SS} = 0V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

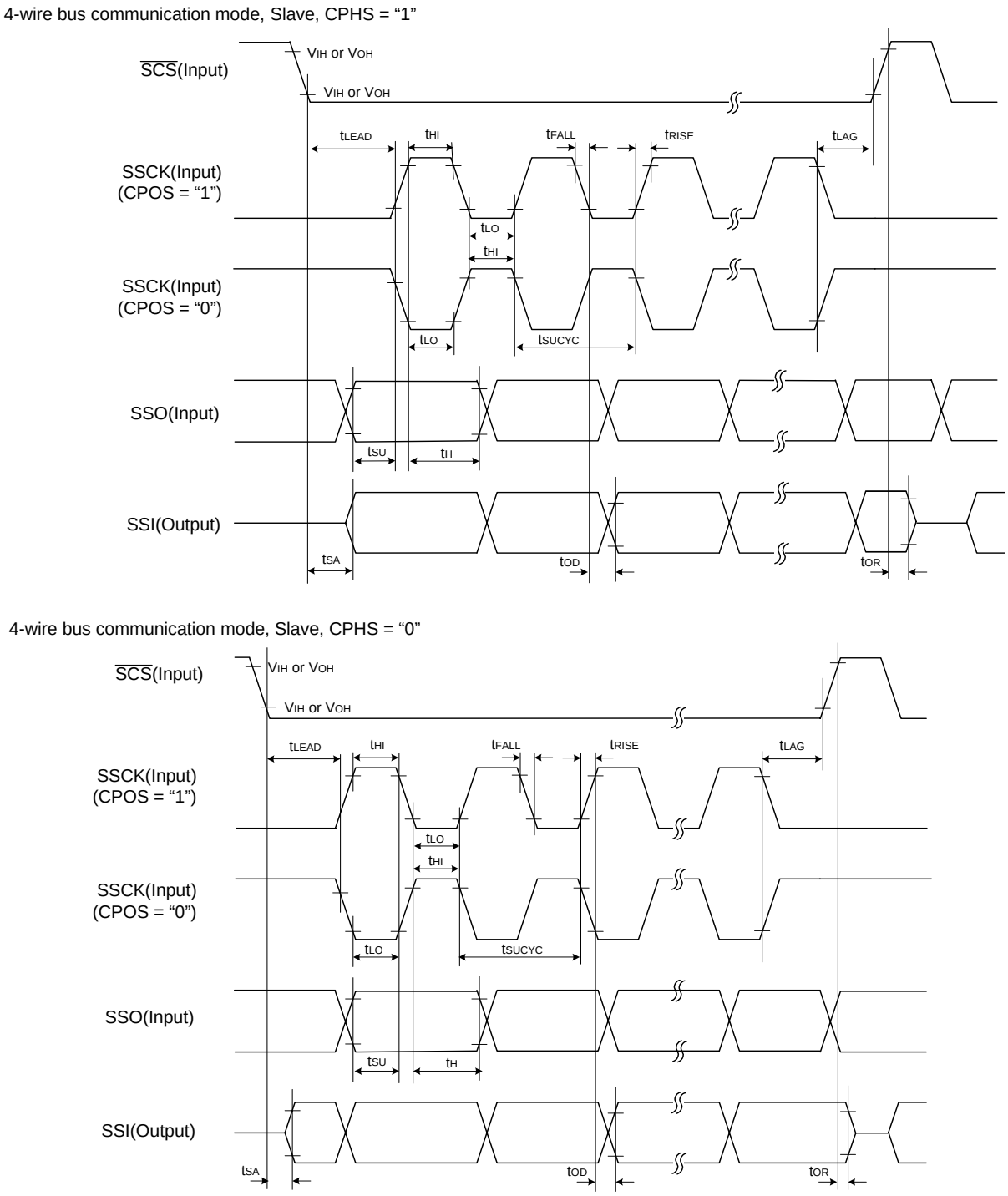


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O (SSU) with Chip Select (Slave)

Table 5.14 Electrical Characteristics (2) [Vcc = 5V] (Topr = -40 to 85 °C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power Supply Current (Vcc=3.3 to 5.5V) In single-chip mode, the output pins are open and other pins are Vss	High-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	9	15	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	8	14	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz No division	–	5	–	mA
		Medium-Speed Mode	XIN = 20MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	4	–	mA
			XIN = 16MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	3	–	mA
			XIN = 10MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	2	–	mA
		High-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz No division	–	4	8	mA
			Main clock off High-speed on-chip oscillator on=8MHz Low-speed on-chip oscillator on=125kHz Divide-by-8	–	1.5	–	mA
		Low-Speed On-Chip Oscillator Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz Divide-by-8	–	470	900	µA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock operation VCA26 = VCA27 = 0	–	40	80	µA
		Wait Mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on=125kHz While a WAIT instruction is executed Peripheral clock off VCA26 = VCA27 = 0	–	38	76	µA
		Stop Mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA26 = VCA27 = 0	–	0.8	3.0	µA

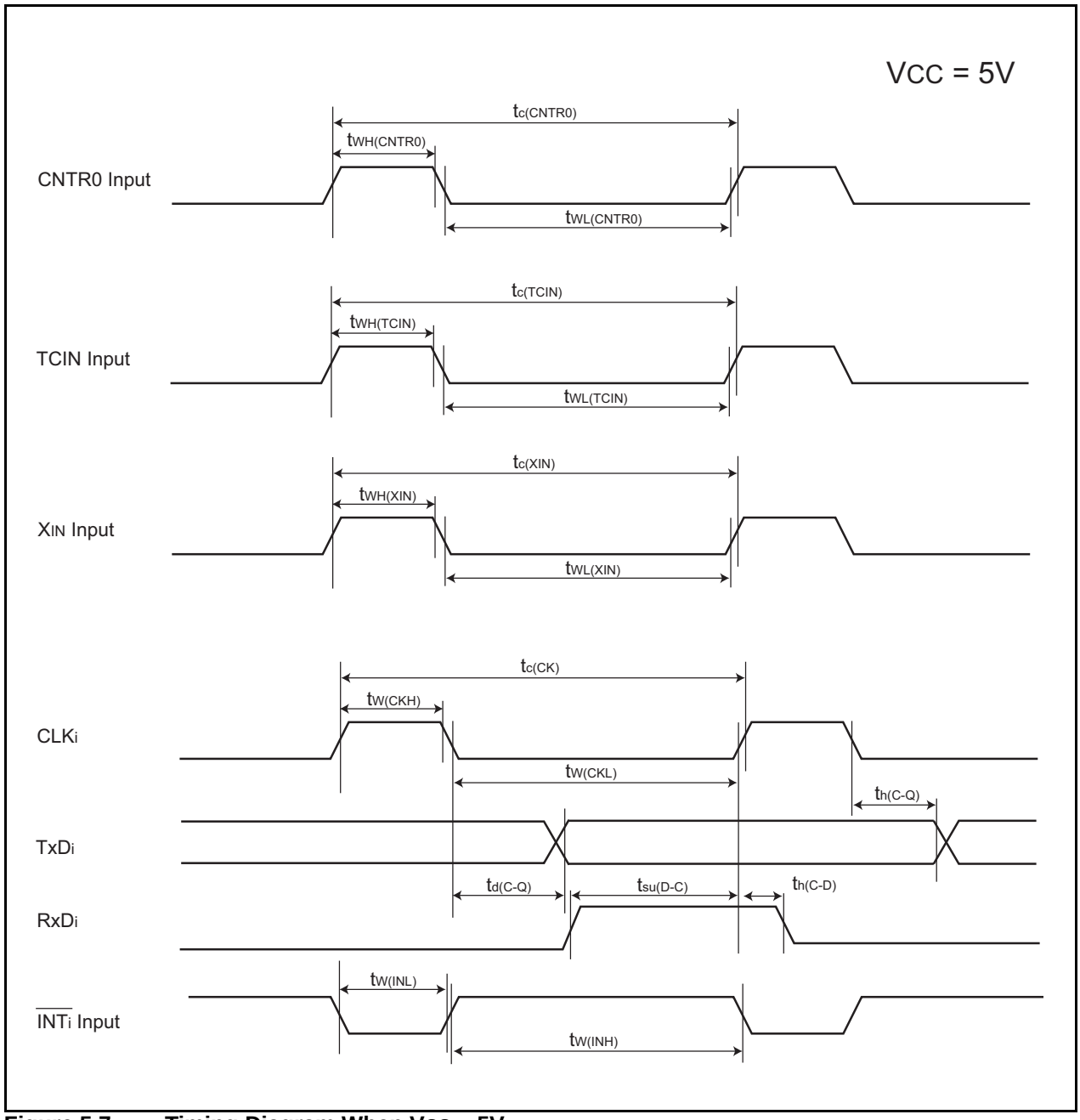


Figure 5.7 Timing Diagram When Vcc = 5V

Timing requirements (Unless otherwise specified: Vcc = 3V, Vss = 0V at Topr = 25 °C) [Vcc = 3V]

Table 5.22 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN Input Cycle Time	100	–	ns
$t_{WH(XIN)}$	XIN Input “H” Width	40	–	ns
$t_{WL(XIN)}$	XIN Input “L” Width	40	–	ns

Table 5.23 CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 Input Cycle Time	300	–	ns
$t_{WH(CNTR0)}$	CNTR0 Input “H” Width	120	–	ns
$t_{WL(CNTR0)}$	CNTR0 Input “L” Width	120	–	ns

Table 5.24 TCIN Input, $\overline{INT3}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN Input Cycle Time	1,200(1)	–	ns
$t_{WH(TCIN)}$	TCIN Input “H” Width	600(2)	–	ns
$t_{WL(TCIN)}$	TCIN Input “L” Width	600(2)	–	ns

NOTES:
1. When using the Timer C input capture mode, adjust the cycle time (1/Timer C count source frequency x 3) or above.
2. When using the Timer C input capture mode, adjust the width (1/Timer C count source frequency x 1.5) or above.

Table 5.25 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	300	–	ns
$t_{W(CKH)}$	CLKi Input “H” Width	150	–	ns
$t_{W(CKL)}$	CLKi Input “L” Width	150	–	ns
$t_{d(C-Q)}$	TXDi Output Delay Time	–	80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0	–	ns
$t_{su(D-C)}$	RXDi Input Setup Time	70	–	ns
$t_{h(C-D)}$	RCDi Input Hold Time	90	–	ns

Table 5.26 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ Input “H” Width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ Input “L” Width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input HIGH width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use the $\overline{INT0}$ input LOW width to the greater value, either (1/digital filter clock frequency x 3) or the minimum value of standard.

REVISION HISTORY	R8C/14 Group, R8C/15 Group Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Jan 30, 2006	8	Figure 1.5 PRDP0020BA-A Package Pin Assignment (top view) deleted Table 1.5 Pin Description; Timer C: "CMP0_0 to CMP0_3, CMP1_0 to CMP1_3" → "CMP0_0 to CMP0_2, CMP1_0 to CMP1_2" revised
		10	Figure 2.1 CPU Register; "Reserved Area" → "Reserved Bit" revised
		12	2.8.10 Reserved Area; "Reserved Area" → "Reserved Bit" revised
		13	Figure 3.1 Memory Map of R8C/14 Group revised
		14	3.2 R8C/15 Group; "(data area)" → "(data flash)", "(program area)" → "(program ROM)" revised Figure 3.2 Memory Map of R8C/15 Group revised
		15	Table 4.1 SFR Information(1); 0009h: "XXXXXX00b" → "00h" 000Ah: "00XXX000b" → "00h" 001Eh: "XXXXX000b" → "00h"
		17	Table 4.3 SFR Information(3); 0085h: "Prescaler Z" → "Prescaler Z Register" 0086h: "Timer Z Secondary" → "Timer Z Secondary Register" 0087h: "Timer Z Primary" → "Timer Z Primary Register" 008Ch: "Prescaler X" → "Prescaler X Register" 008Dh: "Timer X" → "Timer X Register" 0090h, 0091h: "Timer C" → "Timer C Register" revised
		21	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; • NOTES 1 to 7 added • "Topr" → "Ambient temperature", "Program area" → "Program ROM" revised
		22	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; • NOTE1 revised, NOTE9 added • "Topr" → "Ambient temperature", "Data area" → "Data flash" revised
		23	Figure 5.2 Time delay from Suspend Request until Erase Suspend revised
		24	Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset); NOTE2 revised Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset); NOTE1 revised
		25	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; revised Table 5.12 Timing Requirements of Clock Synchronous Serial I/O (SSU) with Chip Select; revised
		30	Table 5.14 Electrical Characteristics (2) [Vcc = 5V]; revised
		31	"Timing Requirements (Unless ... at Ta = 25°C) [VCC = 5V]" → "Timing Requirements (Unless ... at Topr = 25°C) [VCC = 5V]" revised Table 5.18 Serial Interface; "35" → "50", "80" → "50"
		34	Table 5.21 Electrical Characteristics (4) [Vcc = 3V]; revised
		35	"Timing requirements (Unless ... at Ta = 25°C) [VCC = 3V]" → "Timing requirements (Unless ... at Topr = 25°C) [VCC = 3V]" revised Table 5.25 Serial Interface; "55" → "70", "160" → "80"
		37	Package Dimensions; Package "PRDP0020BA-A" deleted

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