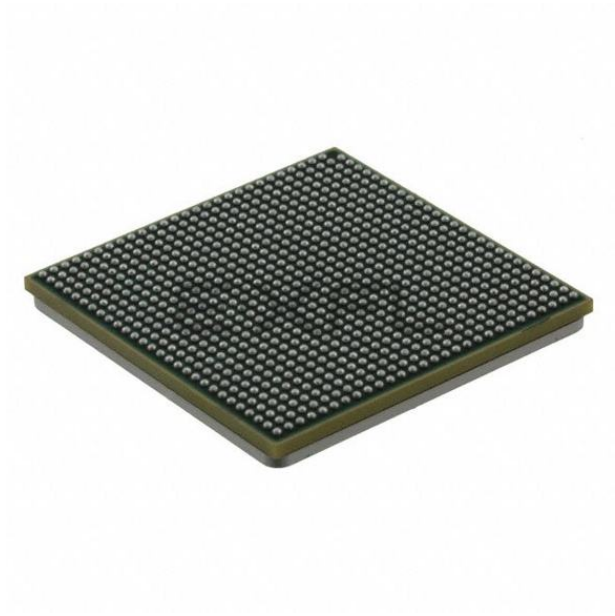

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	EBI/EMI, Ethernet, I²C, PCI, Serial RapidIO, SPI, TDM, UART, UTOPIA
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8144svt1000a

1 Pin Assignments and Reset States

This section includes diagrams of the MSC8144 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in Figure 3 and Figure 4 with their ball location index numbers.

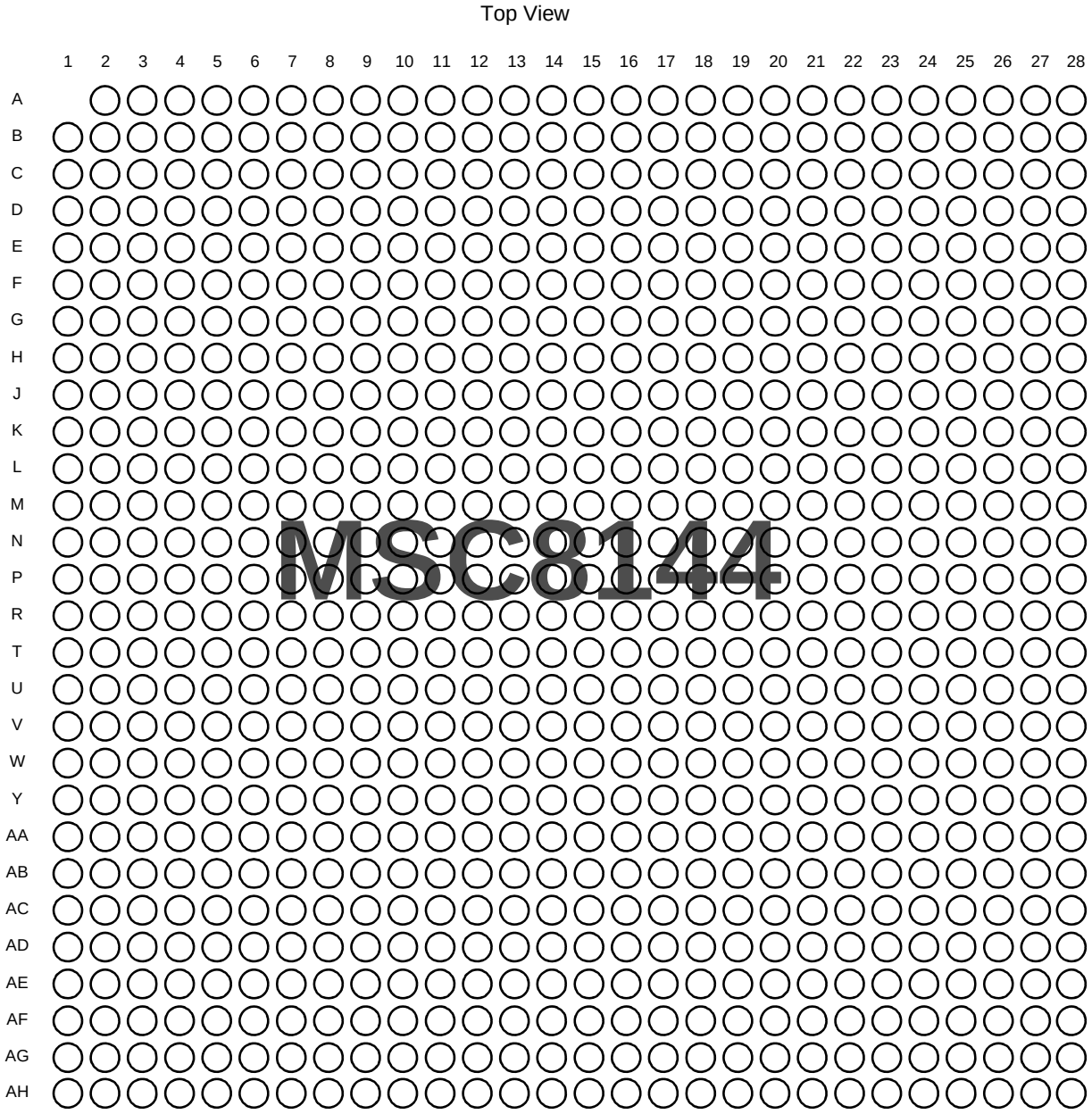


Figure 3. MSC8144 FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
M8	V_{DDIO}										V_{DDIO}
M9	V_{DD}										V_{DD}
M10	GND										GND
M11	V_{DD}										V_{DD}
M12	GND										GND
M13	V_{DD}										V_{DD}
M14	GND										GND
M15	V_{DD}										V_{DD}
M16	GND										GND
M17	V_{DD}										V_{DD}
M18	GND										GND
M19	V_{DD}										V_{DD}
M20	GND										GND
M21	V_{DD}										V_{DD}
M22	V_{DDDDR}										V_{DDDDR}
M23	$\overline{MCS1}$										V_{DDDDR}
M24	MA13										V_{DDDDR}
M25	MA2										V_{DDDDR}
M26	MA0										V_{DDDDR}
M27	GND										GND
M28	MCK1										V_{DDDDR}
N1	Reserved[1]										—
N2	V_{DDIO}										V_{DDIO}
N3	TMS										V_{DDIO}
N4	UTP_RD10/PCI_AD14[5]		UTOPIA		PCI	UTOPIA					V_{DDIO}
N5	V_{DDIO}		Power								V_{DDIO}
N6	UTP_RADDR1/PCI_AD8		UTOPIA		PCI	UTOPIA					V_{DDIO}
N7	UTP_TD9/PCI_AD31		UTOPIA		PCI	UTOPIA					V_{DDIO}
N8	TMR3/$\overline{PCI\_IRDY}$/GPIO19[3,6]/ UTP_TEOP		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
N9	GND										GND
N10	V_{DDM3}										V_{DDM3}
N11	V_{DD}										V_{DD}
N12	V_{DDM3}										V_{DDM3}
N13	V_{DD}										V_{DD}
N14	V_{DDM3}										V_{DDM3}
N15	V_{DD}										V_{DD}
N16	V_{DDM3}										V_{DDM3}
N17	V_{DD}										V_{DD}
N18	V_{DDM3}										V_{DDM3}
N19	V_{DD}										V_{DD}
N20	V_{DDM3}										V_{DDM3}
N21	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
R7	V_{DDIO}										V_{DDIO}
R8	$\overline{\text{PCI\_REQ}}$		PCI								V_{DDIO}
R9	GND										GND
R10	GND										GND
R11	GND										GND
R12	GND										GND
R13	GND										GND
R14	GND										GND
R15	GND										GND
R16	GND										GND
R17	GND										GND
R18	GND										GND
R19	GND										GND
R20	GND										GND
R21	GND										GND
R22	GND										GND
R23	MODT0										V_{DDDDR}
R24	MDIC1										V_{DDDDR}
R25	MDIC0										V_{DDDDR}
R26	$\overline{\text{MCAS}}$										V_{DDDDR}
R27	$\overline{\text{MWE}}$										V_{DDDDR}
R28	MCK2										V_{DDDDR}
T1	Reserved[1]										—
T2	UTP_RPRTY/PCI_AD21		UTOPIA		PCI	UTOPIA					V_{DDIO}
T3	UTP_RD13/PCI_AD17		UTOPIA		PCI	UTOPIA					V_{DDIO}
T4	V_{DDIO}										V_{DDIO}
T5	UTP_RD14/PCI_AD18		UTOPIA		PCI	UTOPIA					V_{DDIO}
T6	UTP_RD15/PCI_AD19		UTOPIA		PCI	UTOPIA					V_{DDIO}
T7	$\overline{\text{PCI\_TRDY}}$		PCI								V_{DDIO}
T8	$\overline{\text{PCI\_DEVSEL}}$/GPIO31/ $\overline{\text{IRQ3}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
T9	GND										GND
T10	GND										GND
T11	GND										GND
T12	GND										GND
T13	GND										GND
T14	GND										GND
T15	GND										GND
T16	GND										GND
T17	GND										GND
T18	GND										GND
T19	GND										GND
T20	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AE19	GND										GND
AE20	V_{DDM3IO}										V_{DDM3IO}
AE21	Reserved[1]										—
AE22	GND										GND
AE23	GND										GND
AE24	GND										GND
AE25	V_{DDDDR}										V_{DDDDR}
AE26	GND										GND
AE27	V_{DDDDR}										V_{DDDDR}
AE28	GND										GND
AF1	Reserved[1]										—
AF2	V_{DDIO}										V_{DDIO}
AF3	GND										GND
AF4	TDM0RDAT/ RCFG_CLKIN_RNG	RCFG_ CLKIN_ RNG	TDM								V_{DDIO}
AF5	TDM0TSYN/RCW_SRC2	RCW_ SRC2	TDM								V_{DDIO}
AF6	TDM1RDAT/RC0	RC0	TDM								V_{DDIO}
AF7	V_{DDIO}										V_{DDIO}
AF8	GND										GND
AF9	TDM2RDAT/RC4	RC4	TDM								V_{DDIO}
AF10	TDM2TCLK		TDM								V_{DDIO}
AF11	GPIO22/$\overline{IRQ4}$[3, 6]/SPIMOSI		GPIO/IRQ/SPI								V_{DDIO}
AF12	GND										GND
AF13	GND										GND
AF14	V_{DDM3IO}										V_{DDM3IO}
AF15	GND										GND
AF16	GND										GND
AF17	Reserved[1]										—
AF18	V_{DDM3IO}										V_{DDM3IO}
AF19	GND										GND
AF20	Reserved[1]										—
AF21	Reserved[1]										—
AF22	$\overline{M3\_RESET}$										V_{DDM3IO}
AF23	GND										GND
AF24	V_{DDDDR}										V_{DDDDR}
AF25	GND										GND
AF26	V_{DDDDR}										V_{DDDDR}
AF27	GND										GND
AF28	V_{DDDDR}										V_{DDDDR}
AG1	Reserved[1]										—
AG2	GPIO16/$\overline{IRQ0}$[3, 6]		GPIO/IRQ								V_{DDIO}
AG3	TDM0TCLK		TDM								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AG4	TDM0RSYN/RCW_SRC0	RCW_SRC0	TDM								V_{DDIO}
AG5	TDM0RCLK		TDM								V_{DDIO}
AG6	TDM0TDAT/RCW_SRC1	RCW_SRC1	TDM								V_{DDIO}
AG7	TDM2TSYN/RC7	RC7	TDM								V_{DDIO}
AG8	TDM2RCLK		TDM								V_{DDIO}
AG9	TDM2RSYN/RC5	RC5	TDM								V_{DDIO}
AG10	GPIO24/$\overline{\text{IRQ6}}$[3, 6]/$\overline{\text{SPISEL}}$		GPIO/IRQ/SPI								V_{DDIO}
AG11	GPIO23/$\overline{\text{IRQ5}}$[3, 6]/SPIMISO		GPIO/IRQ/SPI								V_{DDIO}
AG12	Reserved[1]										—
AG13	GND										GND
AG14	GND										GND
AG15	GND										GND
AG16	GND										GND
AG17	Reserved[1]										—
AG18	Reserved[1]										—
AG19	GND										GND
AG20	GND										GND
AG21	V_{DDM3IO}										V_{DDM3IO}
AG22	GND										GND
AG23	GND										GND
AG24	GND										GND
AG25	V_{DDDDR}										V_{DDDDR}
AG26	GND										GND
AG27	V_{DDDDR}										V_{DDDDR}
AG28	GND										GND
AH1	Reserved[1]										—
AH2	Reserved[1]										—
AH3	Reserved[1]										—
AH4	Reserved[1]										—
AH5	Reserved[1]										—
AH6	Reserved[1]										—
AH7	Reserved[1]										—
AH8	Reserved[1]										—
AH9	Reserved[1]										—
AH10	Reserved[1]										—
AH11	Reserved[1]										—
AH12	Reserved[1]										—
AH13	Reserved[1]										—
AH14	Reserved[1]										—
AH15	Reserved[1]										—
AH16	Reserved[1]										—

2.3 Default Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths.

Table 4. Output Drive Impedance

Driver Type	Output Impedance (Ω)
DDR signal	18
DDR2 signal	18 35 (half strength mode)

2.4 Thermal Characteristics

Table 5 describes thermal characteristics of the MSC8144 for the FC-PBGA packages.

Table 5. Thermal Characteristics for the MSC8144

Characteristic	Symbol	FC-PBGA 29 × 29 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	20	15	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	15	12	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	7		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.8		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature.

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8144.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8144.

Note: DDR SDRAM uses V_{DDDDR}(typ) = 2.5 V and DDR2 SDRAM uses V_{DDDDR}(typ) = 1.8 V.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MSC8144 when V_{DDDDR}(typ) = 1.8 V.

Table 6. DDR2 SDRAM DC Electrical Characteristics for V_{DDDDR} (typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage[1]	V_{DDDDR}	1.7	1.9	V
I/O reference voltage[2]	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage[3]	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V
Output leakage current[4]	I_{OZ}	–50	50	µA
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}.
4. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

2.6.3 Reset Timing

The MSC8144 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- JTAG reset
- RapidIO reset
- Software hard reset
- Software soft reset

All MSC8144 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. Table 17 describes the reset sources.

Table 17. Reset Sources

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	Initiates the power-on reset flow that resets the MSC8144 and configures various attributes of the MSC8144. On $\overline{\text{PORESET}}$, the entire MSC8144 device is reset. All PLLs states is reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the extended cores are reset, and system configuration is sampled. The reset source and word are configured only when $\overline{\text{PORESET}}$ is asserted.
External hard reset ($\overline{\text{HRESET}}$)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8144. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the extended cores are reset, and system configuration is sampled. Note that the RCW (reset Configuration Word) is not reloaded during $\overline{\text{HRESET}}$ assertion after out of power on reset sequence. The reset configuration word is described in the Reset chapter in the *MSC8144 Reference Manual*.
External soft reset ($\overline{\text{SRESET}}$)	Input/ Output	Initiates the soft reset flow. The MSC8144 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8144 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the extended cores are reset, and system configuration is maintained.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.
Software watchdog reset	Internal	When the MSC8144 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
RapidIO reset	Internal	When the RapidIO logic asserts the RapidIO hard reset signal, it generates an internal hard reset sequence.
Software hard reset	Internal	A hard reset sequence can be initialized by writing to a memory mapped register (RCR)
Software soft reset	Internal	A soft reset sequence can be initialized by writing to a memory mapped register (RCR)

Table 18 summarizes the reset actions that occur as a result of the different reset sources.

Table 18. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset ($\overline{\text{PORESET}}$)	Hard Reset ($\overline{\text{HRESET}}$)	Soft Reset ($\overline{\text{SRESET}}$)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (Refer to **Section 2.6.3.2** for details).	Yes	No	No	No
PLL state reset	Yes	No	No	No
Select reset configuration source	Yes	No	No	No
System reset configuration write	Yes	No	No	No

Figure 8 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

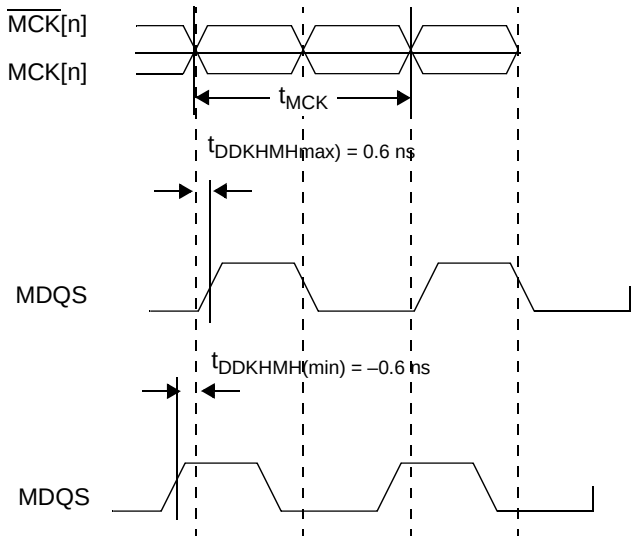


Figure 8. Timing for t_{DDKHMH}

Figure 9 shows the DDR SDRAM output timing diagram.

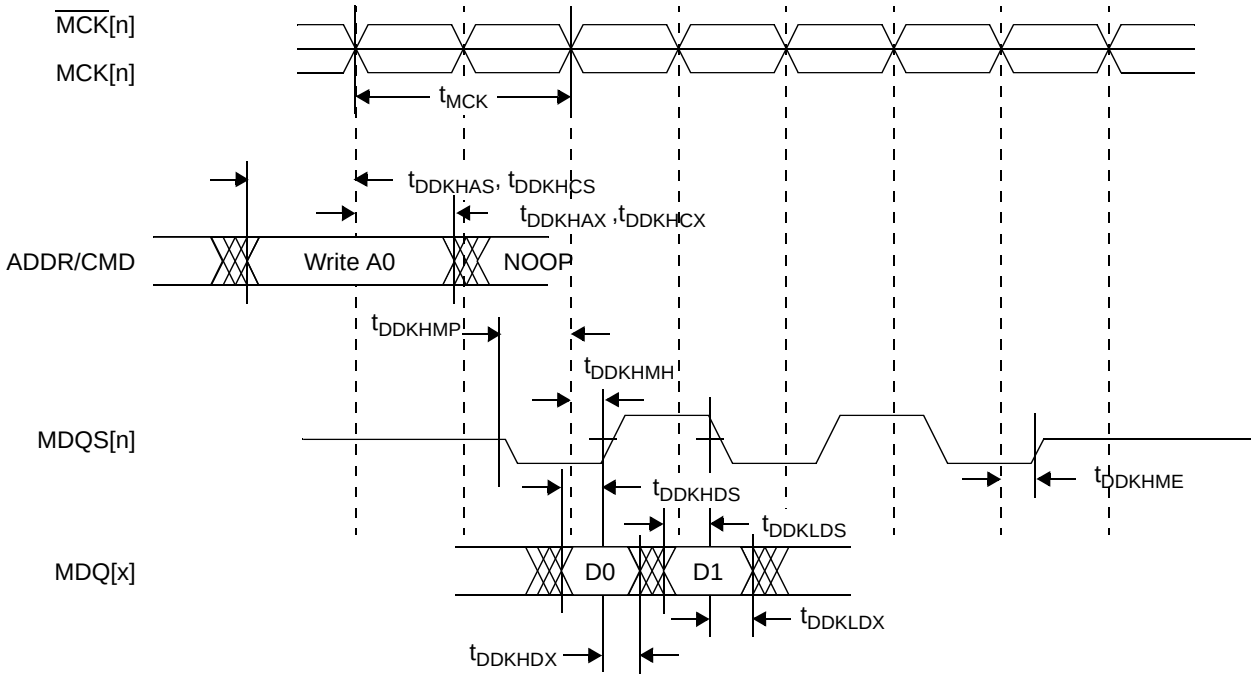


Figure 9. DDR SDRAM Output Timing

Figure 10 provides the AC test load for the DDR bus.

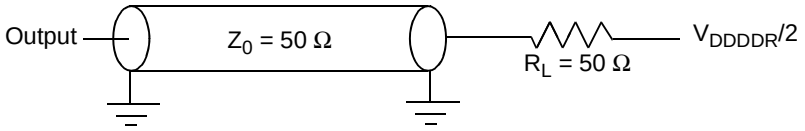


Figure 10. DDR AC Test Load

2.6.5 Serial RapidIO Timing and SGMII Timing

2.6.5.1 AC Requirements for SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$

Table 24 lists AC signal specifications.

Table 24. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Signal Specifications

Parameter Description	Symbol	Min	Typical	Max	Units	Comments
REFCLK cycle time	t_{REF}	—	10 (8, 6.4)	—	ns	8 ns applies only to serial RapidIO system with 125-MHz reference clock. 6.4 ns applies only to serial RapidIO systems with a 156.25 MHz reference clock. **Note:** SGMII uses the 8 ns (125 MHz) value only.

2.6.5.2 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 11 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between voltage levels A and B, where A > B.

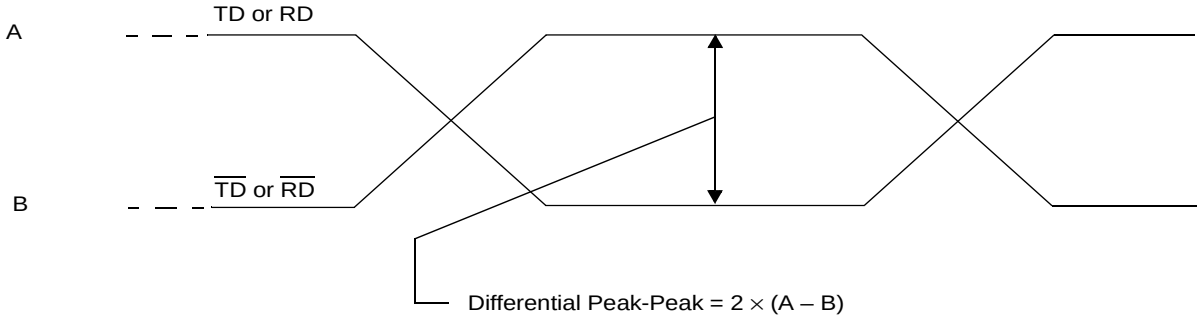


Figure 11. Differential V_{PP} of Transmitter or Receiver

Note: This explanation uses generic TD/$\overline{\text{TD}}$/RD/$\overline{\text{RD}}$ signal names. These correspond to SRIO_TXD/$\overline{\text{SRIO\_TXD}}$/ SRIO_RXD/$\overline{\text{SRIO\_RXD}}$ respectively.

2.6.5.6 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 32, Table 33, and Table 34) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 14 with the parameters specified in Table 35. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω ±5% differential resistive load.

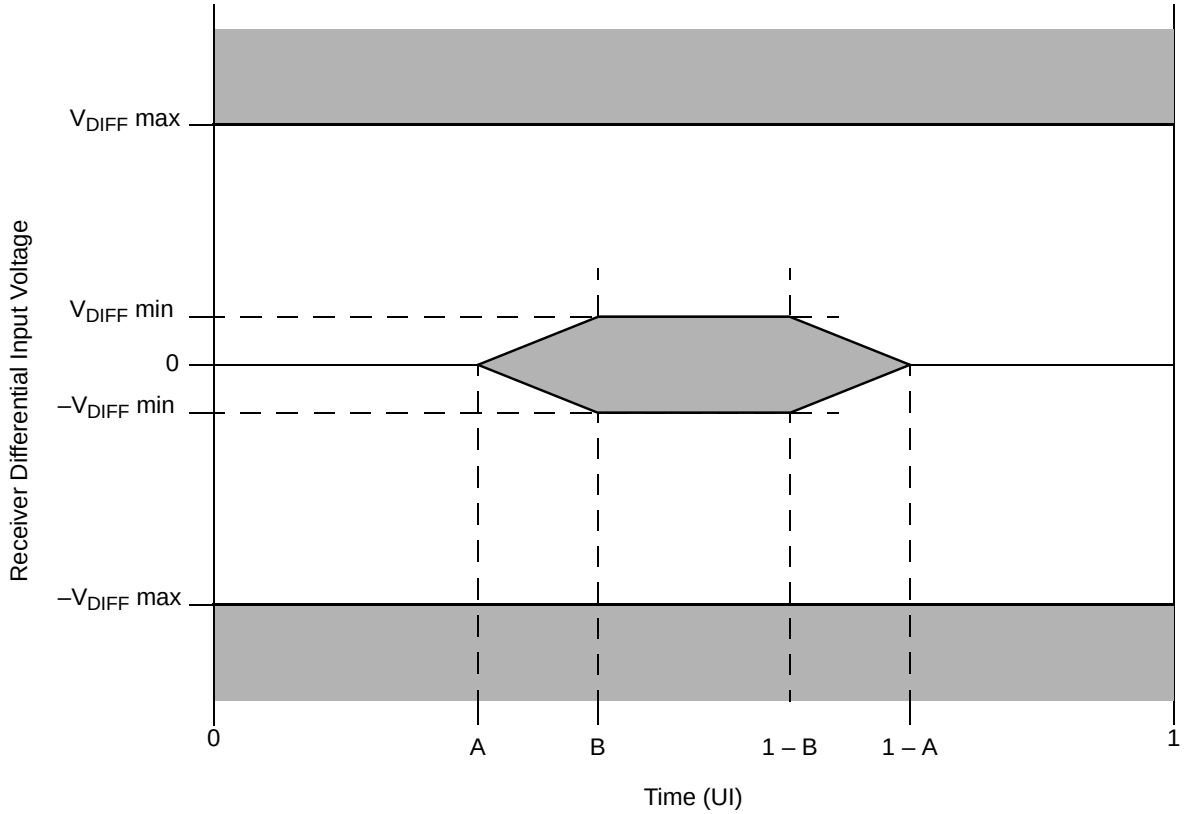


Figure 14. Receiver Input Compliance Mask

Table 35. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

2.6.5.7 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of **IEEE** Std. 802.3ae-2002™, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of **IEEE** Std. 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of **IEEE** Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

Figure 31 shows the RGMII AC timing and multiplexing diagrams.

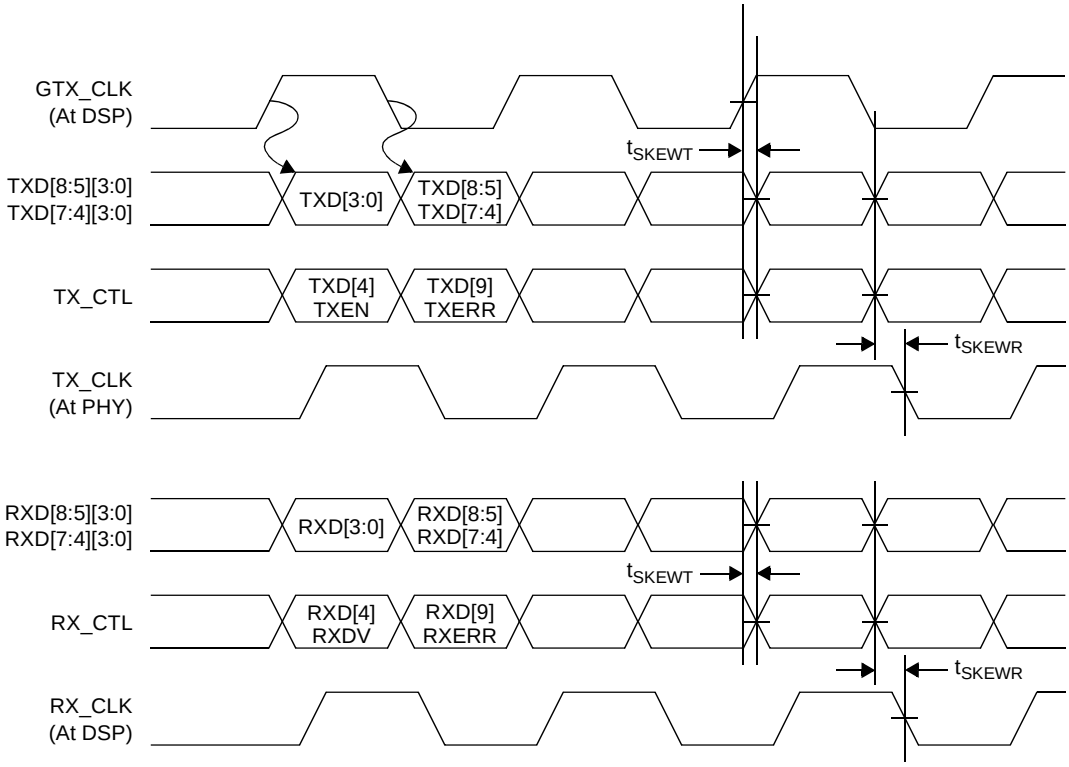


Figure 31. RGMII AC Timing and Multiplexing

2.6.11 ATM/UTOPIA/POS Timing

Table 47 provides the ATM/UTOPIA/POS input and output AC timing specifications.

Table 47. ATM/UTOPIA/POS AC Timing (External Clock) Specifications

Characteristic	Symbol	Min	Max	Unit
Outputs—External clock delay	t_{UEKHOV}	1	9	ns
Outputs—External clock High Impedance[1]	t_{UEKHOX}	1	9	ns
Inputs—External clock input setup time	t_{UEIVKH}	4		ns
Inputs—External clock input hold time	t_{UEIXKH}	1		ns

Notes:
1. Not tested. Guaranteed by design.
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. Although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 32 provides the AC test load for the ATM/UTOPIA/POS.

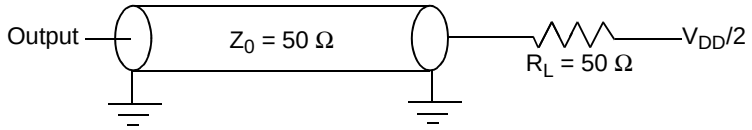


Figure 32. ATM/UTOPIA/POS AC Test Load

Figure 33 shows the ATM/UTOPIA/UTOPIA timing with external clock.

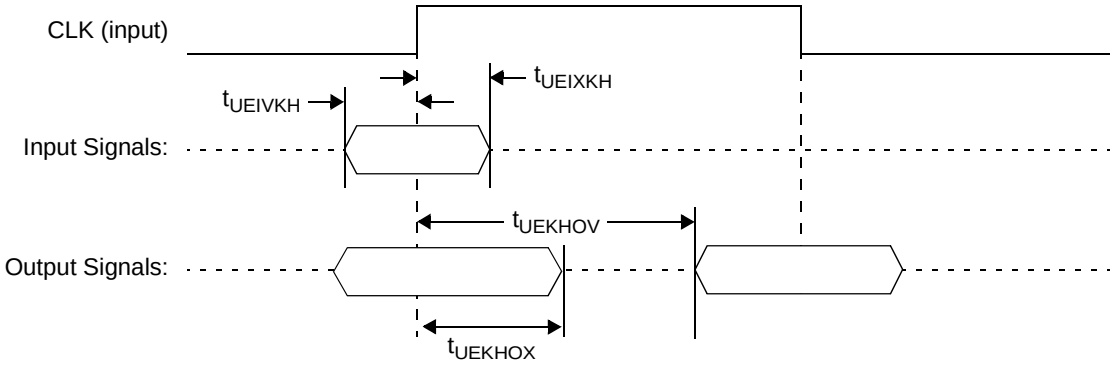


Figure 33. ATM/UTOPIAPOS AC Timing (External Clock)

2.6.12 SPI Timing

Table 48 lists the SPI input and output AC timing specifications.

Table 48. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}		6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—Master mode (internal clock input) setup time	t_{NIIVKH}	4		ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 34 provides the AC test load for the SPI.

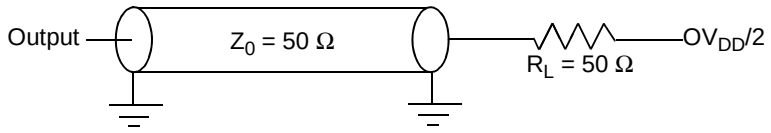
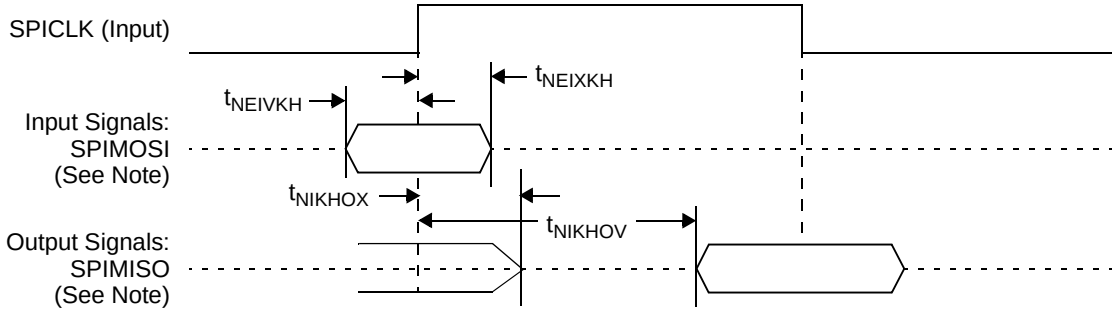


Figure 34. SPI AC Test Load

Figure 35 and Figure 36 represent the AC timings from Table 48. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

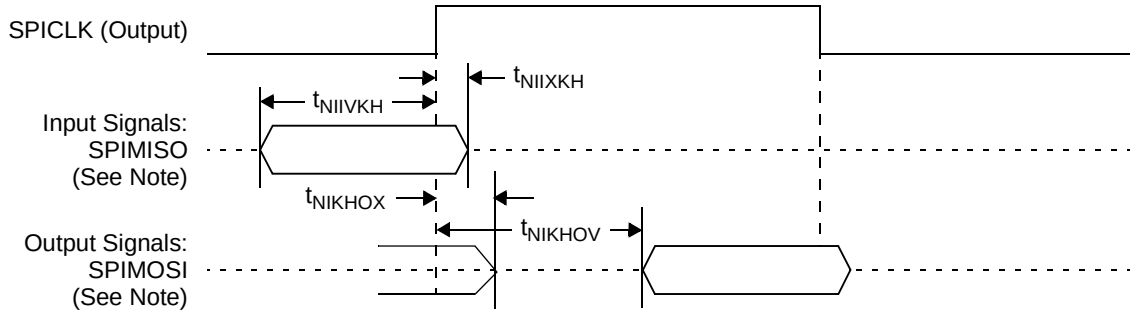
Figure 35 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Slave Mode (External Clock)

Figure 36 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 36. SPI AC Timing in Master Mode (Internal Clock)

2.6.13 Asynchronous Signal Timing

Table 49. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN cycle[1]
Output	t_{OUT}	Asynchronous	Application dependent
Note: 1. Relevant for EE0, $\overline{\text{IRQ}}$[15–0], and $\overline{\text{NMI}}$ only.			

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a GPI, the input should be driven until it is acknowledged by the device; the GPIO input status is read from a register.

- *EE port.* Signals EE0, EE1, EE2_0, EE2_1, EE2_2, and EE2_3.
- *Boot function*. Signal STOP_BS.
- *I^2C interface*. Signals I2C_SCL and I2C_SDA.
- *Interrupt inputs*. Signals $\overline{\text{IRQ}}$[15–0] and $\overline{\text{NMI}}$.
- *Interrupt outputs*. Signals $\overline{\text{INT\_OUT}}$ and $\overline{\text{NMI\_OUT}}$ (pulse width is 10 ns).

Figure 37 shows the behavior of the asynchronous signals.

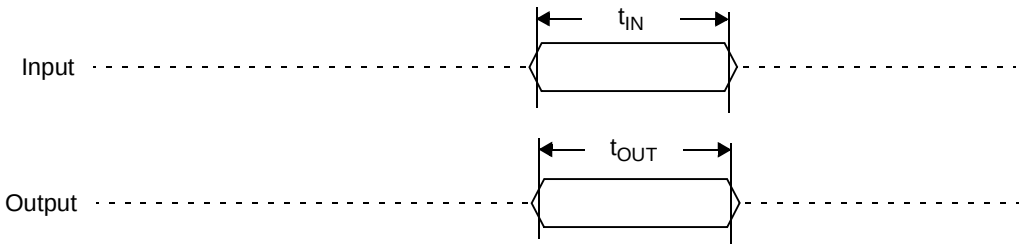


Figure 37. Asynchronous Signal Timing

3.2 Power Supply Design Considerations

Each PLL supply must have an external RC filter for the V_{DDPLL} input. The filter is a 10 Ω resistor in series with two 2.2 µF, low ESL (<0.5 nH) and low ESR capacitors. All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately (see Figure 43). For optimal noise filtering, place the circuit as close as possible to its V_{DDPLL} inputs. These traces should be short and direct.

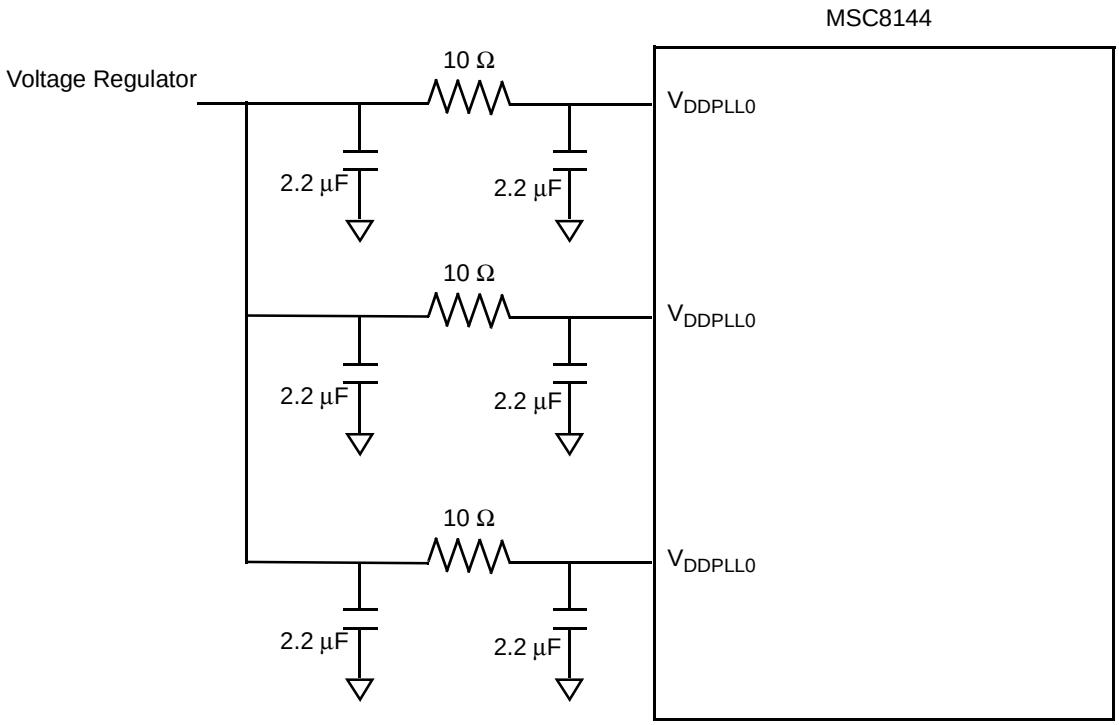


Figure 43. PLL Supplies

Table 58. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
GE1_SGMII_TX	NC
GE1_TD[0-3]	NC
GE1_TX_CLK	GND
GE1_TX_EN	NC
GE1_TX_ER	NC

3.4.4.2 Ethernet Controller 2 (GE2) Related Pins

Note: Table 59 through Table 61 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.4.4.2.1 GE2 interface Is Not Used

Table 59 assumes that the GE2 pins are not used for any purpose (including any multiplexed function) and that V_{DDGE2} is tied to GND.

Table 59. Connectivity of GE2 Related Pins When the GE2 Interface Is Not Used

Signal Name	Pin Connection
GE2_RD[0-3]	NC
GE2_RX_CLK	NC
GE2_RX_DV	NC
GE2_RX_ER	NC
GE2_SGMII_RX	GND_{SXC}
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	Nc
GE2_TD[0–3]	Nc
GE2_TX_EN	NC

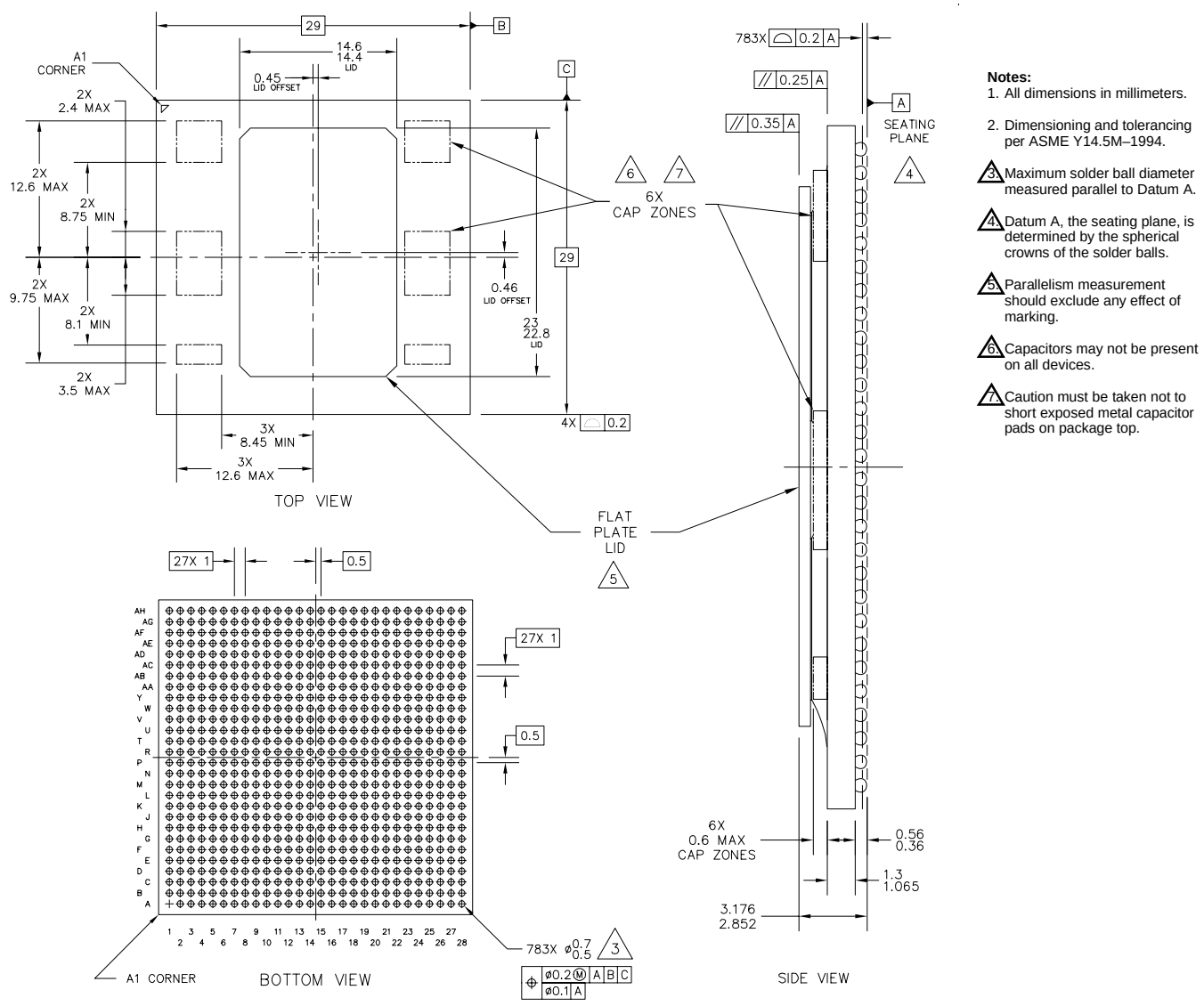
3.4.4.2.2 Subset of GE2 Pins Required

When only a subset of the whole GE2 interface is used, such as for RMII, the unused GE2 pins should be connected as described in Table 60. The table assumes that the unused GE2 pins are not used for any purpose (including any multiplexed functions) and that V_{DDGE2} is tied to either 2.5 V or 3.3 V.

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required

Signal Name	Pin Connection
GE2_RD[0-3]	GND
GE2_RX_CLK	GND
GE2_RX_DV	GND
GE2_RX_ER	GND
GE2_SGMII_RX	GND_{SXC}

5 Package Information



Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement should exclude any effect of marking.
6. Capacitors may not be present on all devices.
7. Caution must be taken not to short exposed metal capacitor pads on package top.

CASE NO. 1842-04

Figure 44. MSC8144 Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

- *MSC8144 Technical Data Sheet* (MSC8144). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8144 device.
- *MSC8144 Reference Manual* (MSC8144RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes.* Cover various programming topics related to the StarCore DSP core and the MSC8144 device.
- *SC3400 DSP Core Reference Manual*. Covers the SC3400 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8144 SC3400 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

Table 66. Document Revision History (continued)

Rev.	Date	Description
7	Dec 2007	• Changed minimum voltage level for V_{DDM3} to 1.213 (1.25 – 3%) in Table 3. • Added POS to titles in **Section 2.6.6**. • Added additional signals to titles in **Section 2.6.8**. Added high and low voltage ranges to Table 19. • Added ATM and POS to headings in **Section 2.7.11**. Changed characteristics to generic input/output in Table 52, Figure 33, and Figure 34. • Replaced **Sections 2.7.13** and **2.7.14** with new **Section 2.7.13**, *Asynchronous Signal Timing*. Renumbered subsequent sections, tables, and figures. • Added POS to all UTOPIA references in **Section 3.4.5**.
8	Dec 2007	• Changed GCR4 program value to 0x0004C130 in Note 7 in Table 51.
9	Mar 2008	• Changed description of Table 20 in **Section 2.7.2**.
10	Apr 2008	• Added [3] to the PLL supply voltage row in **Table 2**. • Changed the first sentence in **Section 3.4.8** to reflect that **Table 70** indicates what to do with pins if they are "not" required by the design. Changed the Pin Connection for GPIO[0–31] to GND. • Updated ordering information in **Section 4**. • Multiple corrections of minor punctuation errors.
11	Aug 2008	• Removed the comment about preliminary estimates before Table 4 and removed non-DDR rows in the table. • Table 9 and Table 11 for DDR and DDR2 SDRAM capacitance removed and subsequent tables renumbered. • Changed units for I_{OH} and I_{OL} to mA in Table 9. • Removed signal low and high input current from Table 12. • Added a note to Table 15 to exclude TDM and TMS. Removed reference to overshoot and undershoot and associated figure. • Changed minimum clock frequency to 33 MHz and maximum clock frequency to 133 MHz in Table 16. • Deleted old Table 17 Clock Parameters. • Changed minimum input clock frequency to 33 MHz in Table 19. • Changed the t_{DDKHAX} minimum value in Table 23 to 1.85 ns. • Removed t_{REFPJ} and t_{REFCJ} from Table 24 because the specifications are not required or tested. • Removed $t_{PCRSTCLK}$, $t_{PCRSTOFF}$, t_{PCRST}, and t_{PCRHFA} from Table 36 because the specifications are not required or tested. • Removed t_{UAVKH} and t_{UAVXH} from Table 38 because the specifications are not required or tested. • The parameters t_{MDCH}, t_{MDCR}, and t_{MDHF} were removed from Table 40 because the specifications are not required or tested. • The parameters t_{MTXH}/t_{MTX}, t_{MTXR}, and t_{MTXF} were removed from Table 41 because the specifications are not required or tested. • The parameters t_{MRXH}/t_{MRX}, t_{MRXR}, and t_{MRXF} were removed from Table 42 because the specifications are not required or tested. • The parameters t_{RMXH}/t_{RMX}, t_{RMXR}, and t_{RMXF} were removed from Table 43 because the specifications are not required or tested. • Removed the parameters t_{RGT}, t_{RGTH}/t_{RGT} (1000Base-T), t_{RGTH}/t_{RGT} (10Base-T), t_{RGTR}, t_{RGTF}, t_{G12}, and t_{G125H}/t_{G125} were removed from Table 45 and Table 46 because the specifications are not required or tested. • Changed t_{UEKHOX} to guaranteed by design in Table 47. • Updated Figure 35 and Figure 36 SPI timing diagrams. • Removed TCK rise and fall time from Table 50. • Updated orderable part numbers in **Section 4**.
12	Aug 2008	• Changed b8t to bit in the M3 memory description on the first page. • Changed maximum input high voltage (VIH) for SPI to 3.465 in the first row of Table 14. • Changed packet processor to QUICC Engine Subsystem in the last row of Table 18.
13	Feb 2009	• In Figure 31, for GTX_CLK, changed (at transmitter) to (at DSP) and for RX_CLK, changed (at PHY) to (at DSP). • Updated package drawing to the latest revision, Case No. 1842-04 in Figure 44.
14	Jul 2009	• Updated MV_{REF} equations and temperature ranges in Table 3. • Updated orderable part numbers to **Section 4**.
15	Nov 2009	• Updated Core and PLL input voltage tolerance in Table 3.
16	May 2010	• Corrected typo in Table 23. Changed MCLK minimum time to 5 ns.