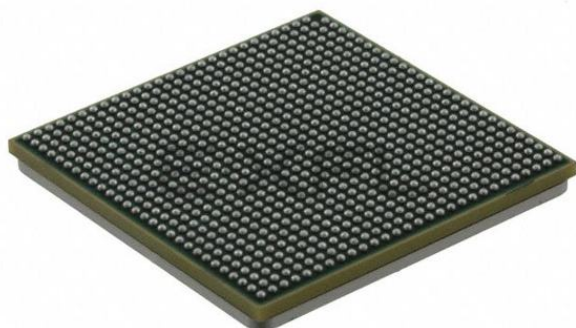




Welcome to [E-XFL.COM](#)

Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Obsolete
Type	SC3400 Core
Interface	EBI/EMI, Ethernet, I ² C, PCI, Serial RapidIO, SPI, TDM, UART, UTOPIA
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8144svt1000b

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2				PCI	Ethernet 2			V _{DDGE2}
A4	V _{DDGE2}										V _{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2				PCI	Ethernet 2			V _{DDGE2}
A6	GE2_TD0/PCI_CBE0		Ethernet 2				PCI	Ethernet 2			V _{DDGE2}
A7	SRIO_IMP_CAL_RX										V _{DDSCX}
A8	Reserved ¹										—
A9	Reserved ¹										—
A10	Reserved ¹										—
A11	Reserved ¹										—
A12	SRIO_RXD0										V _{DDSCX}
A13	V _{DDSCX}										V _{DDSCX}
A14	SRIO_RXD1										V _{DDSCX}
A15	V _{DDSCX}										V _{DDSCX}
A16	SRIO_REF_CLK										V _{DDSCX}
A17	V _{DDRIOPLL}										GND _{RIOPLL}
A18	GND _{SCX}										GND _{SCX}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V _{DDSCX}
A20	V _{DDSCX}										V _{DDSCX}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V _{DDSCX}
A22	V _{DDSCX}										V _{DDSCX}
A23	SRIO_IMP_CAL_TX										V _{DDSCP}
A24	MDQ28										V _{DDDDR}
A25	MDQ29										V _{DDDDR}
A26	MDQ30										V _{DDDDR}
A27	MDQ31										V _{DDDDR}
A28	MDQS3										V _{DDDDR}
B1	Reserved ¹										—
B2	GE2_TD1/PCI_CBE1		Ethernet 2				PCI	Ethernet 2			V _{DDGE2}
B3	GE2_TX_EN/PCI_CBE2		Ethernet 2				PCI	Ethernet 2			V _{DDGE2}
B4	GE_MDIO		Ethernet								V _{DDGE2}
B5	GND										GND
B6	GE_MDC		Ethernet								V _{DDGE2}
B7	GND _{SCX}										GND _{SCX}
B8	Reserved ¹										—
B9	Reserved ¹										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power- On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E6	V _{DDGE1}										V _{DDGE1}
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E8	Reserved ¹										—
E9	Reserved ¹										—
E10	GND										GND
E11	V _{DD}										V _{DD}
E12	GND										GND
E13	V _{DD}										V _{DD}
E14	GND										GND
E15	V _{DD}										V _{DD}
E16	GND										GND
E17	V _{DD}										V _{DD}
E18	GND										GND
E19	V _{DD}										V _{DD}
E20	GND										GND
E21	V _{DD}										V _{DD}
E22	GND										GND
E23	V _{DDDDR}										V _{DDDDR}
E24	MDQ20										V _{DDDDR}
E25	GND										GND
E26	V _{DDDDR}										V _{DDDDR}
E27	GND										GND
E28	MDQS2										V _{DDDDR}
F1	Reserved ¹										—
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
F3	V _{DDGE1}										V _{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
F6	GND										GND
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
F8	V _{DDGE1}										V _{DDGE1}
F9	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power- On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
G23	MBA1										V _{DDDDR}
G24	MA3										V _{DDDDR}
G25	MA8										V _{DDDDR}
G26	V _{DDDDR}										V _{DDDDR}
G27	GND										GND
G28	MCK0										V _{DDDDR}
H1	Reserved ¹										—
H2	CLKIN										V _{DDIO}
H3	HRESET										V _{DDIO}
H4	PCI_CLK_IN										V _{DDIO}
H5	NMI										V _{DDIO}
H6	URXD/GPIO14/IRQ8/ RC_LDF ^{3, 6}	RC_LDF	UART/GPIO/IRQ								V _{DDIO}
H7	GE1_RX_ER/PCI_AD6/ GPIO25/IRQ15 ^{3, 6}		GPIO/ IRQ	Ethernet 1	PCI			GPIO/ IRQ	Ethernet 1		V _{DDIO}
H8	GE1_CRS/PCI_AD5		PCI	Ethernet 1	PCI			Ethernet 1			V _{DDIO}
H9	GND										GND
H10	V _{DD}										V _{DD}
H11	GND										GND
H12	V _{DD}										V _{DD}
H13	GND										GND
H14	V _{DD}										V _{DD}
H15	V _{DD}										V _{DD}
H16	V _{DD}										V _{DD}
H17	GND										GND
H18	V _{DD}										V _{DD}
H19	GND										GND
H20	V _{DD}										V _{DD}
H21	V _{DD}										V _{DD}
H22	V _{DDDDR}										V _{DDDDR}
H23	MBA0										V _{DDDDR}
H24	MA15										V _{DDDDR}
H25	V _{DDDDR}										V _{DDDDR}
H26	MA9										V _{DDDDR}
H27	MA7										V _{DDDDR}
H28	MCK0										V _{DDDDR}
J1	Reserved ¹										—
J2	GND										GND
J3	V _{DDIO}										V _{DDIO}
J4	STOP_BS										V _{DDIO}
J5	NMI_OUT ⁴										V _{DDIO}
J6	INT_OUT ⁴										V _{DDIO}
J7	SDA/GPIO27 ^{3, 4, 6}		I2C/GPIO								V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V _{DDIO}										V _{DDIO}
J9	V _{DD}										V _{DD}
J10	GND										GND
J11	V _{DD}										V _{DD}
J12	GND										GND
J13	V _{DD}										V _{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V _{DD}										V _{DD}
J18	GND										GND
J19	V _{DD}										V _{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V _{DDDDR}										V _{DDDDR}
J25	GND										GND
J26	V _{DDDDR}										V _{DDDDR}
J27	GND										GND
J28	V _{DDDDR}										V _{DDDDR}
K1	Reserved ¹										—
K2	Reserved ¹										—
K3	Reserved ¹										—
K4	Reserved ¹										—
K5	V _{DDPLL2A}										V _{DDPLL2A}
K6	GND										GND
K7	V _{DDPLL0A}										V _{DDPLL0A}
K8	V _{DDPLL1A}										V _{DDPLL1A}
K9	V _{DD}										V _{DD}
K10	GND										GND
K11	V _{DD}										V _{DD}
K12	GND										GND
K13	V _{DD}										V _{DD}
K14	V _{DD}										V _{DD}
K15	V _{DD}										V _{DD}
K16	V _{DD}										V _{DD}
K17	V _{DD}										V _{DD}
K18	GND										GND
K19	V _{DD}										V _{DD}
K20	GND										GND
K21	V _{DD}										V _{DD}
K22	V _{DDDDR}										V _{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
K23	MBA2										V _{DDDDR}
K24	MA10										V _{DDDDR}
K25	MA12										V _{DDDDR}
K26	MA14										V _{DDDDR}
K27	MA4										V _{DDDDR}
K28	MV _{REF}										V _{DDDDR}
L1	Reserved ¹										—
L2	CLKOUT										V _{DDIO}
L3	TMR1/UTP_IR/PCI_CBE3/ GPIO17 ^{3, 6}		UTOPIA		TMR/ GPIO	UTOPIA	PCI		UTOPIA		V _{DDIO}
L4	TMR4/PCI_PAR/GPIO20 ^{3, 6} / UTP_REOP		TIMER/GPIO				PCI		TIMER/GPIO		V _{DDIO}
L5	GND										GND
L6	TMR2/PCI_FRAME/ GPIO18 ^{3, 6}		TIMER/GPIO				PCI		TIMER/GPIO	UTOPIA	V _{DDIO}
L7	SCL/GPIO26 ^{3, 4, 6}		I ² C/GPIO								V _{DDIO}
L8	UTXD/GPIO15/IRQ9 ^{3, 6}		UART/GPIO/IRQ								V _{DDIO}
L9	GND										GND
L10	V _{DD}										V _{DD}
L11	GND										GND
L12	V _{DD}										V _{DD}
L13	GND										GND
L14	V _{DD}										V _{DD}
L15	Reserved ¹										GND
L16	V _{DD}										V _{DD}
L17	GND										GND
L18	V _{DD}										V _{DD}
L19	GND										GND
L20	V _{DD}										V _{DD}
L21	GND										GND
L22	GND										GND
L23	MCKE1										V _{DDDDR}
L24	MA1										V _{DDDDR}
L25	V _{DDDDR}										V _{DDDDR}
L26	GND										GND
L27	V _{DDDDR}										V _{DDDDR}
L28	MCK1										V _{DDDDR}
M1	Reserved ¹										—
M2	TRST										V _{DDIO}
M3	EE0										V _{DDIO}
M4	EE1										V _{DDIO}
M5	UTP_RCLK/PCI_AD13		UTOPIA		PCI		UTOPIA				V _{DDIO}
M6	UTP_RADDR0/PCI_AD7		UTOPIA		PCI		UTOPIA				V _{DDIO}
M7	UTP_TD8/PCI_AD30		UTOPIA		PCI		UTOPIA				V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
N22	GND										GND
N23	MODT1										V _{DDDDR}
N24	MCKE0										V _{DDDDR}
N25	V _{DDDDR}										V _{DDDDR}
N26	MA5										V _{DDDDR}
N27	MA6										V _{DDDDR}
N28	MA11										V _{DDDDR}
P1	Reserved ¹										—
P2	TDI ⁵										V _{DDIO}
P3	UTP_RD11/PCI_AD15		UTOPIA		PCI	UTOPIA					V _{DDIO}
P4	GND										GND
P5	UTP_RADDR3/PCI_AD10		UTOPIA		PCI	UTOPIA					V _{DDIO}
P6	UTP_RADDR2/PCI_AD9		UTOPIA		PCI	UTOPIA					V _{DDIO}
P7	PCI_GNT/GPIO29/IRQ7 ^{3, 6}		GPIO/IRQ		PCI		GPIO/IRQ				V _{DDIO}
P8	PCI_STOP/GPIO30/IRQ2 ^{3, 6}		GPIO/IRQ		PCI		GPIO/IRQ				V _{DDIO}
P9	GND										GND
P10	GND										GND
P11	V _{DDM3}										V _{DDM3}
P12	GND										GND
P13	V _{DDM3}										V _{DDM3}
P14	GND										GND
P15	V _{DDM3}										V _{DDM3}
P16	GND										GND
P17	V _{DDM3}										V _{DDM3}
P18	GND										GND
P19	V _{DDM3}										V _{DDM3}
P20	GND										GND
P21	GND										GND
P22	V _{DDDDR}										V _{DDDDR}
P23	MCS0										V _{DDDDR}
P24	MRAS										V _{DDDDR}
P25	GND										GND
P26	V _{DDDDR}										V _{DDDDR}
P27	GND										GND
P28	MCK2										V _{DDDDR}
R1	Reserved ¹										—
R2	TCK										V _{DDIO}
R3	TDO										V _{DDIO}
R4	UTP_RD12/PCI_AD16		UTOPIA		PCI	UTOPIA					V _{DDIO}
R5	UTP_RCLAV_PDRPA/PCI_AD12		UTOPIA		PCI	UTOPIA					V _{DDIO}
R6	UTP_RADDR4/PCI_AD11		UTOPIA		PCI	UTOPIA					V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AE19	GND										GND
AE20	V _{DDM3IO}										V _{DDM3IO}
AE21	Reserved ¹										—
AE22	GND										GND
AE23	GND										GND
AE24	GND										GND
AE25	V _{DDDDR}										V _{DDDDR}
AE26	GND										GND
AE27	V _{DDDDR}										V _{DDDDR}
AE28	GND										GND
AF1	Reserved ¹										—
AF2	V _{DDIO}										V _{DDIO}
AF3	GND										GND
AF4	TDM0RDAT/ RCFG_CLKIN_RNG	RCFG_ CLKIN_ RNG	TDM								V _{DDIO}
AF5	TDM0TSYN/RCW_SRC2	RCW_ SRC2	TDM								V _{DDIO}
AF6	TDM1RDAT/RC0	RC0	TDM								V _{DDIO}
AF7	V _{DDIO}										V _{DDIO}
AF8	GND										GND
AF9	TDM2RDAT/RC4	RC4	TDM								V _{DDIO}
AF10	TDM2TCLK		TDM								V _{DDIO}
AF11	GPIO22/ $\overline{\text{IRQ}}4^{3, 6}$ /SPIMOSI		GPIO/IRQ/SPI								V _{DDIO}
AF12	GND										GND
AF13	GND										GND
AF14	V _{DDM3IO}										V _{DDM3IO}
AF15	GND										GND
AF16	GND										GND
AF17	Reserved ¹										—
AF18	V _{DDM3IO}										V _{DDM3IO}
AF19	GND										GND
AF20	Reserved ¹										—
AF21	Reserved ¹										—
AF22	M3_RESET										V _{DDM3IO}
AF23	GND										GND
AF24	V _{DDDDR}										V _{DDDDR}
AF25	GND										GND
AF26	V _{DDDDR}										V _{DDDDR}
AF27	GND										GND
AF28	V _{DDDDR}										V _{DDDDR}
AG1	Reserved ¹										—
AG2	GPIO16/ $\overline{\text{IRQ}}0^{3, 6}$		GPIO/IRQ								V _{DDIO}
AG3	TDM0TCLK		TDM								V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AH17	Reserved ¹										—
AH18	Reserved ¹										—
AH19	Reserved ¹										—
AH20	Reserved ¹										—
AH21	Reserved ¹										—
AH22	Reserved ¹										—
AH23	Reserved ¹										—
AH24	Reserved ¹										—
AH25	Reserved ¹										—
AH26	Reserved ¹										—
AH27	Reserved ¹										—
AH28	Reserved ¹										—
Notes: 1. Reserved signals should be disconnected for compatibility with future revisions of the device. 2. For signals with same functionality in all modes the appropriate cells are empty. 3. The choice between GPIO function and other function is by GPIO registers setup. For configuration details, see Chapter 23, GPIO in the <i>MSC8144 Reference Manual</i>. 4. Open-drain signal. 5. Internal 20 KΩ pull-up resistor. 6. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See Chapter 23, GPIO of the <i>MSC8144 Reference Manual</i> for configuration details.											

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8144.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8144.

Note: DDR SDRAM uses $V_{DDDDR}(\text{typ}) = 2.5 \text{ V}$ and DDR2 SDRAM uses $V_{DDDDR}(\text{typ}) = 1.8 \text{ V}$.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MSC8144 when $V_{DDDDR}(\text{typ}) = 1.8 \text{ V}$.

Table 6. DDR2 SDRAM DC Electrical Characteristics for $V_{DDDDR}(\text{typ}) = 1.8 \text{ V}$

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage ¹	V_{DDDDR}	1.7	1.9	V
I/O reference voltage ²	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage ³	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	-0.3	$MV_{REF} - 0.125$	V
Output leakage current ⁴	I_{OZ}	-50	50	μA
Output high current ($V_{OUT} = 1.420 \text{ V}$)	I_{OH}	-13.4	—	mA
Output low current ($V_{OUT} = 0.280 \text{ V}$)	I_{OL}	13.4	—	mA
Notes: V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}. - Output leakage is measured with all outputs are disabled, $0 \text{ V} \leq V_{OUT} \leq V_{DDDDR}$.				

2.5.2 Serial RapidIO DC Electrical Characteristics

DC receiver logic levels are not defined since the receiver is AC-coupled.

2.5.2.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks `SRIO_REF_CLK` and `SRIO_REF_CLK` are AC-coupled differential inputs. Each differential clock input has an internal $50\ \Omega$ termination to `GNDSXC`. The reference clock must be able to drive this termination. The recommended minimum operating voltage is $-0.4\ \text{V}$; the recommended maximum operating voltage is $1.32\ \text{V}$; and the maximum absolute voltage is $1.72\ \text{V}$.

The maximum average current allowed in each input is $8\ \text{mA}$. This current limitation sets the maximum common mode input voltage to be less than $0.4\ \text{V}$ ($0.4\ \text{V}/50\ \Omega = 8\ \text{mA}$) while the minimum common mode input level is `GNDSXC`. For example, a clock with a 50/50 duty cycle can be driven by a current source output that ranges from $0\ \text{mA}$ to $16\ \text{mA}$ ($0\text{--}0.8\ \text{V}$). The input is AC-coupled internally, so, therefore, the exact common mode input voltage is not critical.

Note: This internal AC-couple network does not function correctly with reference clock frequencies below $90\ \text{MHz}$.

If the device driving the `SRIO_REF_CLK` inputs cannot drive $50\ \Omega$ to `GNDSXC`, or if it exceeds the maximum input current limitations, then it must use external AC-coupling. The minimum differential peak-to-peak amplitude of the input clock is $0.4\ \text{V}$ ($0.2\ \text{V}$ peak-to-peak per phase). The maximum differential peak-to-peak amplitude of the input clock is $1.6\ \text{V}$ peak-to-peak (see Figure 5). The termination to `GNDSXC` allows compatibility with HCSL type reference clocks specified for PCI-Express applications. Many other low voltage differential type outputs can be used but will probably need to be AC-coupled due to the limited common mode input range. LVPECL outputs can produce too large an amplitude and may need to be source terminated with a divider network to reduce the amplitude. The amplitude of the clock must be at least a $400\ \text{mV}$ differential peak-peak for single-ended clock. If driven differentially, each signal wire needs to drive $100\ \text{mV}$ around common mode voltage. The differential reference clock (`SRIO_REF_CLK`/`SRIO_REF_CLK`) input is HCSL-compatible DC coupled or LVDS-compatible with AC-coupling.

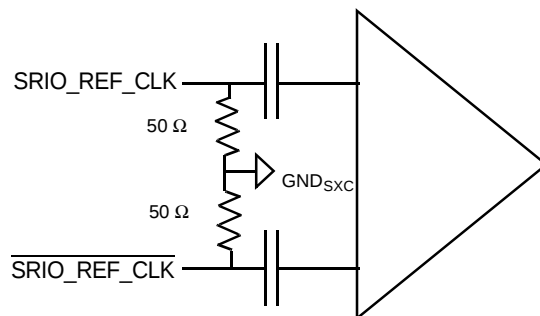


Figure 5. SerDes Reference Clocks Input Stage

2.5.5 Ethernet DC Electrical Characteristics

2.5.5.1 MII, SMII and RMII DC Electrical Characteristics

Table 11. MII, SMII and RMII DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDGE1} V_{DDGE2}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	-0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	-30	30	μ A
Signal low input current, $V_{IL} = 0.4$ V ¹	I_L	-30	30	μ A
Signal high input current, $V_{IH} = 2.4$ V ¹	I_H	-30	30	μ A
Output high voltage, $I_{OH} = -4$ mA	V_{OH}	2.4	3.465	V
Output low voltage, $I_{OL} = 4$ mA	V_{OL}	—	0.4	V
Input Pin Capacitance ¹	C_{IN}		8	pF
Note: 1. Not tested. Guaranteed by design.				

2.5.5.2 RGMII DC Electrical Characteristics

Table 12. RGMII DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 2.5 V	V_{DDGE1} V_{DDGE2}	2.375	2.625	V
Input high voltage	V_{IH}	1.7	2.625	V
Input low voltage	V_{IL}	-0.3	0.7	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	-30	30	μ A
Output high voltage, $I_{OH} = -1$ mA	V_{OH}	2.0	2.625	V
Output low voltage, $I_{OL} = 1$ mA	V_{OL}	—	0.4	V
Input Pin Capacitance ¹	C_{IN}		8	pF
Note: 1. Not tested. Guaranteed by design.				

Table 18. Reset Actions for Each Reset Source (continued)

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTEST, CLAMP, or HIGHZ
HRESET driven	Yes	Yes	No	No
IPBus modules reset (TDM, UART, SWT, DDRC, IPBus master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
SRESET driven	Yes	Yes	Yes	Depends on command
Extended cores reset	Yes	Yes	Yes	Yes
CLASS registers reset	Yes	Yes	Some registers	Some registers
Timers, Performance Monitor	Yes	Yes	No	No
QUICC Engine subsystem, PCI, DMA	Yes	Yes	Most registers	Most registers

2.6.3.1 Power-On Reset (PORESET) Pin

Asserting $\overline{\text{PORESET}}$ initiates the power-on reset flow. $\overline{\text{PORESET}}$ must be asserted externally for at least 32 CLKIN cycles after V_{DD} and V_{DDIO} are both at their nominal levels.

2.6.3.2 Reset Configuration

The MSC8144 has two mechanisms for writing the reset configuration:

- Through the I²C port
- Through external pins
- Through internal hard coded

Twenty-three signals (see **Section 1** for signal description details) are sampled during the power-on reset sequence to define the Reset Word Configuration Source and operating conditions:

- RCW_SRC[2–0]
- RC[16–0]

The RCFG_CLKIN_RNG pin must be valid during power-on or hard reset sequence. The STOP_BS pin must be always valid and is also sampled during power-on reset sequence for RCW loading from an I²C EEPROM.

2.6.3.3 Reset Timing Tables

Table 19 and Figure 7 describe the reset timing for a reset configuration.

Table 19. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Max	Min	Unit
1	Required external $\overline{\text{PORESET}}$ duration minimum • 33 MHz $\leq$ CLKIN < 44 MHz • 44 MHz $\leq$ CLKIN < 66 MHz • 66 MHz $\leq$ CLKIN < 100 MHz • 100 MHz $\leq$ CLKIN < 133 MHz	32/CLKIN	1280 728 485 320	727 484 320 241	ns ns ns ns

Table 19. Timing for a Reset Configuration Write (continued)

No.	Characteristics	Expression	Max	Min	Unit
2	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for external pins and hard coded RCW				
	• 33 MHz $\leq$ CLKIN < 66 MHz	15369/CLKIN	615	233	μs
	• 66 MHz $\leq$ CLKIN $\leq$ 133 MHz	34825/CLKIN	528	262	μs
	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for loading RCW the I ² C interface				
	• 33 MHz $\leq$ CLKIN < 44 MHz	92545/CLKIN	3702	2103	μs
3	Delay from $\overline{\text{HRESET}}$ deassertion to $\overline{\text{SRESET}}$ deassertion				
	• REFCLK = 33 MHz to 133 MHz	16/CLKIN	640	120	ns
Note: Timings are not tested, but are guaranteed by design.					

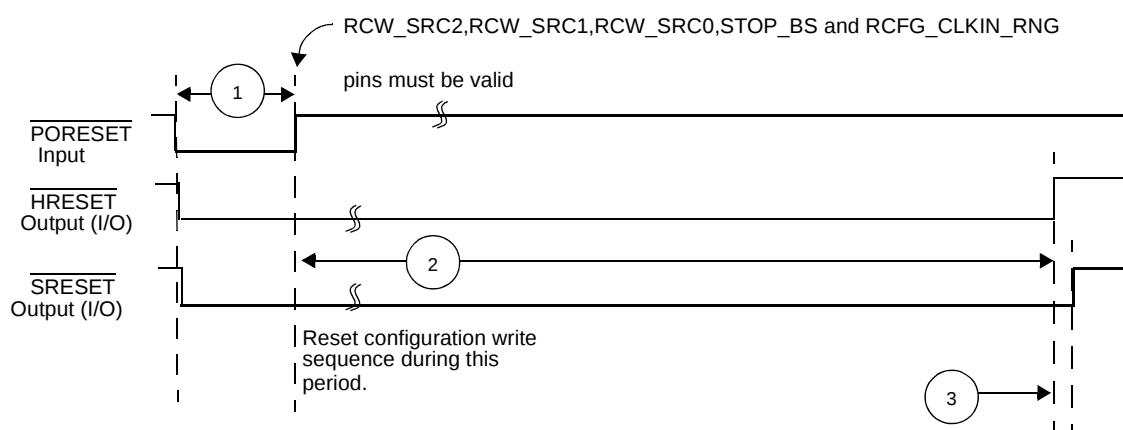


Figure 7. Timing for a Reset Configuration Write

See also Reset Errata for PLL lock and reset duration.

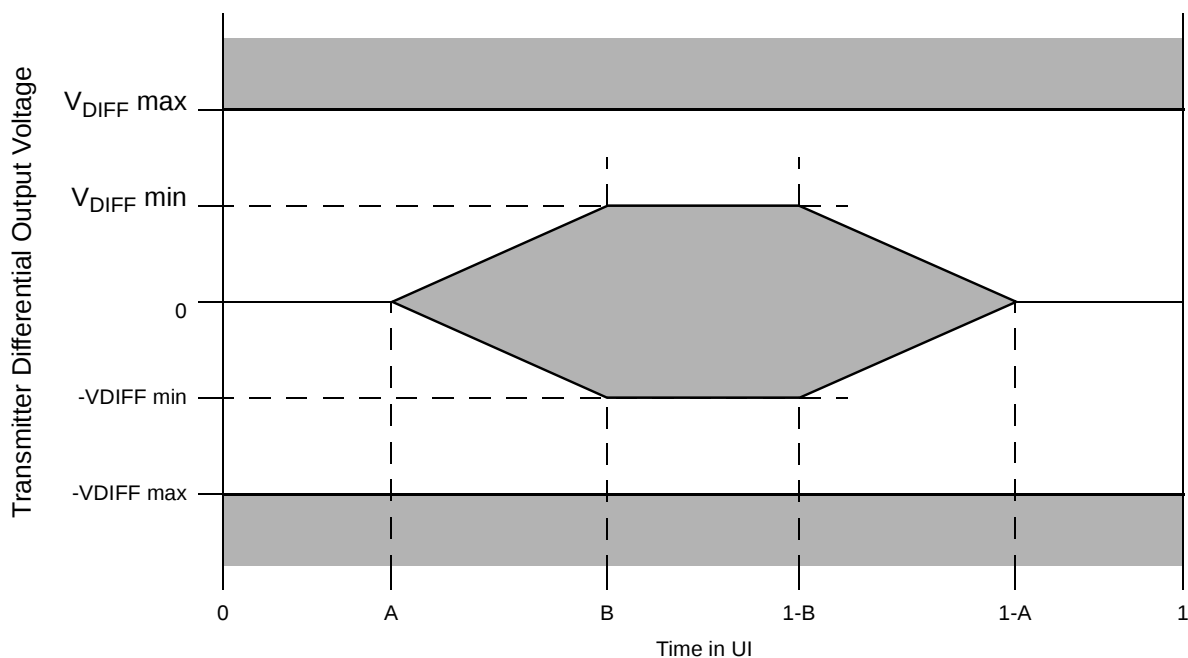


Figure 12. Transmitter Output Compliance Mask

Table 31. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

Table 36. PCI AC Timing Specifications (continued)

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
Notes: 1. See the timing measurement conditions in the <i>PCI 2.2 Local Bus Specifications</i>. 2. All PCI signals are measured from $0.5 \times V_{DDIO}$ of the rising edge of PCI_CLK_IN to $0.4 \times V_{DDIO}$ of the signal in question for 3.3-V PCI signaling levels. 3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification. 4. Input timings are measured at the pin. 5. The reset assertion timing requirement for <u>HRESET</u> is in Table 19 and Figure 7						

Figure 15 provides the AC test load for the PCI.

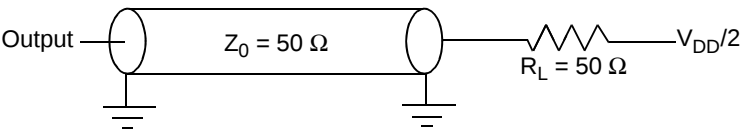


Figure 15. PCI AC Test Load

Figure 16 shows the PCI input AC timing conditions.

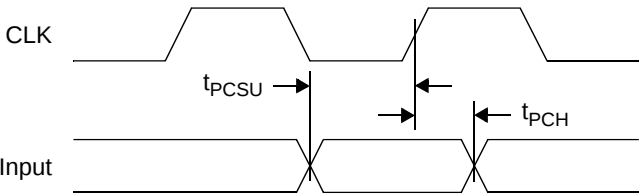


Figure 16. PCI Input AC Timing Measurement Conditions

Figure 17 shows the PCI output AC timing conditions.

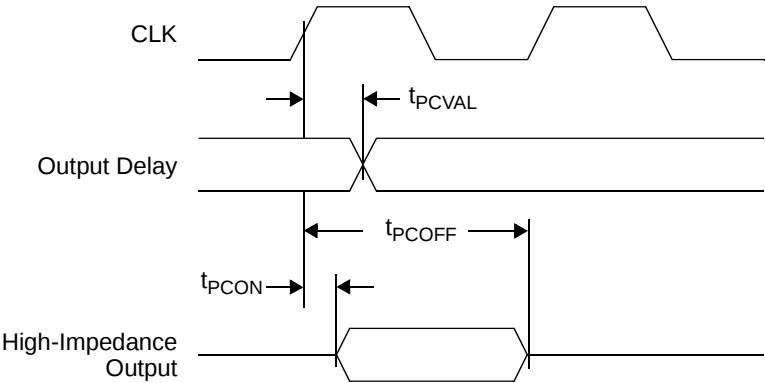


Figure 17. PCI Output AC Timing Measurement Condition

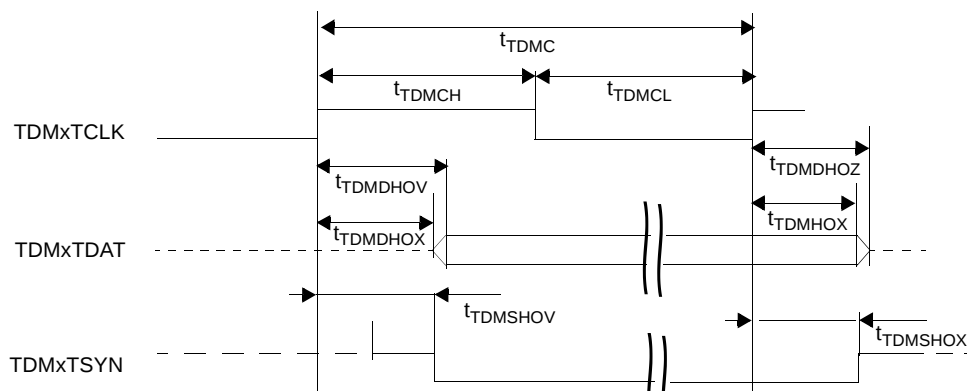


Figure 20. TDM Output Signals

Note: For some TDM modes, transmit data is output on other pins. This timing is also valid for those pins. See the *MSC8144 Reference Manual*

2.6.8 UART Timing

Table 38. UART Timing

Characteristics	Symbol	Expression	Min	Max	Unit
URXD and UTXD inputs high/low duration	$T_{UREFCLK}$	$16 \times T_{REFCLK}$	160	—	ns
Note: $T_{UREFCLK} = T_{REFCLK}$ is guaranteed by design.					

Figure 21 shows the UART input AC timing

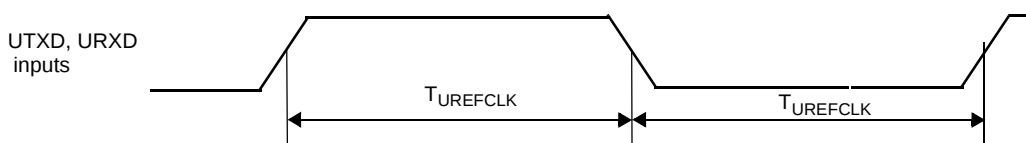


Figure 21. UART Input Timing

Figure 22 shows the UART output AC timing

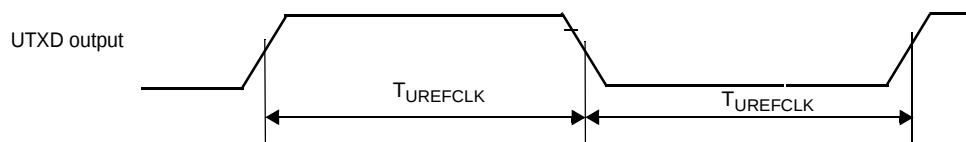


Figure 22. UART Output Timing

Figure 26 provides the AC test load.

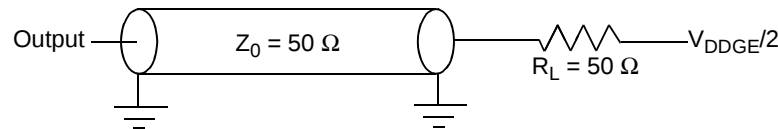


Figure 26. AC Test Load

Figure 27 shows the MII receive AC timing diagram.

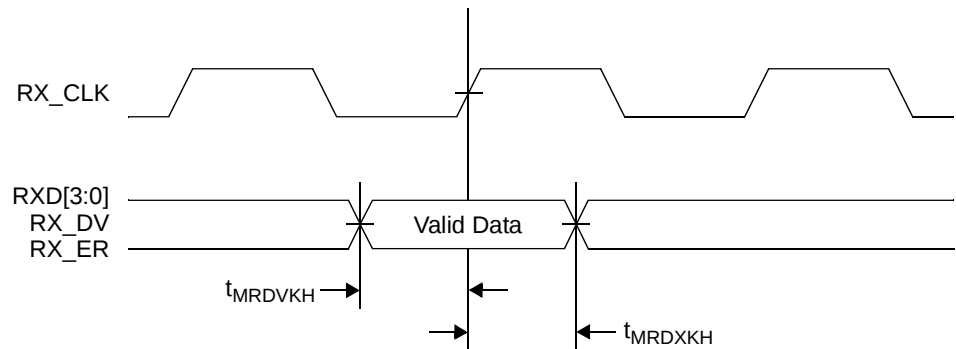


Figure 27. MII Receive AC Timing

2.6.10.4 RMII Transmit and Receive AC Timing Specifications

Table 43 provides the RMII transmit and receive AC timing specifications.

Table 43. RMII Transmit and Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Max	Unit
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	65	%
REF_CLK to RMII data TXD[1–0], TX_EN delay	$t_{RMTKHDX}$	2	10	ns
RXD[1–0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	ns
RXD[1–0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	ns
Typical REF_CLK clock period (t_{RMX}) is 20 ns				
Notes: 1. Typical REF_CLK clock period (t_{RMX}) is 20 ns 2. Program GCR4 as 0x00001405				

Table 58. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
GE1_SGMII_TX	NC
GE1_TD[0-3]	NC
GE1_TX_CLK	GND
GE1_TX_EN	NC
GE1_TX_ER	NC

3.4.4.2 Ethernet Controller 2 (GE2) Related Pins

Note: Table 59 through Table 61 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.4.4.2.1 GE2 interface Is Not Used

Table 59 assumes that the GE2 pins are not used for any purpose (including any multiplexed function) and that V_{DDGE2} is tied to GND.

Table 59. Connectivity of GE2 Related Pins When the GE2 Interface Is Not Used

Signal Name	Pin Connection
GE2_RD[0-3]	NC
GE2_RX_CLK	NC
GE2_RX_DV	NC
GE2_RX_ER	NC
GE2_SGMII_RX	GND _{SXC}
GE2_SGMII_RX	GND _{SXC}
GE2_SGMII_TX	NC
GE2_SGMII_TX	NC
GE2_TCK	Nc
GE2_TD[0-3]	Nc
GE2_TX_EN	NC

3.4.4.2.2 Subset of GE2 Pins Required

When only a subset of the whole GE2 interface is used, such as for RMII, the unused GE2 pins should be connected as described in Table 60. The table assumes that the unused GE2 pins are not used for any purpose (including any multiplexed functions) and that V_{DDGE2} is tied to either 2.5 V or 3.3 V.

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required

Signal Name	Pin Connection
GE2_RD[0-3]	GND
GE2_RX_CLK	GND
GE2_RX_DV	GND
GE2_RX_ER	GND
GE2_SGMII_RX	GND _{SXC}

3.4.6 TDM Interface Related Pins

Table 63 lists the board connections of the TDM pins when an entire specific TDM is not used. For multiplexing options that select a subset of a TDM interface, use the connections described in Table 63 for those signals that are not selected. Table 63 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 63. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDMxRCLK	GND
TDMxRDAT	GND
TDMxRSYN	GND
TDMxTCLK	GND
TDMTxDAT	GND
TDMxTSYN	GND
V _{DDIO}	3.3 V
Notes: 1. $x = \{0, 1, 2, 3, 4, 5, 6, 7\}$ 2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See Chapter 20, TDM, in the <i>MSC8144 Reference Manual</i> for details.	

3.4.7 PCI Related Pins

Table 64 lists the board connections of the pins when PCI is not used. Table 64 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 64. Connectivity of PCI Related Pins When PCI Is Not Used

Signal Name	Pin Connection
PCI_AD[0–31]	GND
PCI_CBE[0–3]	GND
PCI_CLK_IN	GND
PCI_DEVSEL	V _{DDIO}
PCI_FRAME	V _{DDIO}
PCI_GNT	V _{DDIO}
PCI_IDS	GND
PCI_IRDY	V _{DDIO}
PCI_PAR	GND
PCI_PERR	V _{DDIO}
PCI_REQ	NC
PCI_SERR	V _{DDIO}
PCI_STOP	V _{DDIO}
PCI_TRDY	V _{DDIO}
V _{DDIO}	3.3 V

3.4.8 Miscellaneous Pins

Table 65 lists the board connections for the pins if they are not required by the system design. Table 65 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 65. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[0–31]	GND
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT_OUT}}$	NC
$\overline{\text{IRQ}}[0–15]$	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V _{DDIO}
$\overline{\text{NMI_OUT}}$	NC
RC[0–16]	GND
$\overline{\text{RC_LDF}}$	NC
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[0–4]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	GND
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
V _{DDIO}	3.3 V
Note: When using I/O multiplexing mode 5 or 6, tie the TDM7TSYN/PCI_AD4 signal (ball number AC9) to GND.	

Note: For details on configuration, see the *MSC8144 Reference Manual*. For additional information, refer to the *MSC8144 Design Checklist* (AN3202).