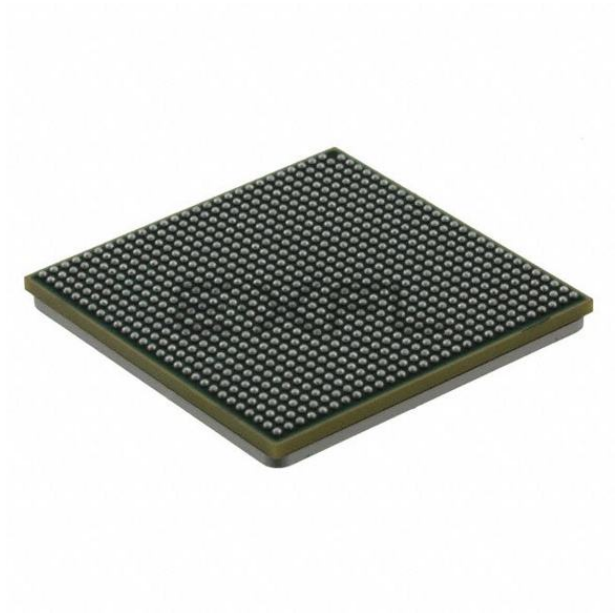

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	EBI/EMI, Ethernet, I²C, PCI, Serial RapidIO, SPI, TDM, UART, UTOPIA
Clock Rate	800MHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8144svt800a

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Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
B10	Reserved[1]										—
B11	Reserved[1]										—
B12	$\overline{\text{SRIO\_RXD0}}$										V_{DDSXC}
B13	GND_{SXC}										GND_{SXC}
B14	$\overline{\text{SRIO\_RXD1}}$										V_{DDSXC}
B15	GND_{SXC}										GND_{SXC}
B16	SRIO_REF_CLK										V_{DDSXC}
B17	Reserved[1]										—
B18	V_{DDSXC}										V_{DDSXC}
B19	$\overline{\text{SRIO\_RXD2}}$/ $\overline{\text{GE1\_SGMII\_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B20	GND_{SXC}										GND_{SXC}
B21	$\overline{\text{SRIO\_RXD3}}$/ $\overline{\text{GE2\_SGMII\_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B22	GND_{SXC}										GND_{SXC}
B23	GND_{SXP}										GND_{SXP}
B24	MDQ27										V_{DDDDR}
B25	V_{DDDDR}										V_{DDDDR}
B26	GND										GND
B27	V_{DDDDR}										V_{DDDDR}
B28	MDQS3										V_{DDDDR}
C1	Reserved[1]										—
C2	GE2_RX_CLK/PCI_AD29		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C3	V_{DDGE2}										V_{DDGE2}
C4	TDM7RSYN/GE2_TD2/ PCI_AD2/UTP_TER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C5	TDM7RCLK/GE2_RD2/ PCI_AD0/UTP_RVL		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C6	V_{DDGE2}										V_{DDGE2}
C7	GE2_RD0/PCI_AD27		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C8	Reserved[1]										—
C9	Reserved[1]										—
C10	Reserved[1]										—
C11	Reserved[1]										—
C12	V_{DDSXP}										V_{DDSXP}
C13	$\overline{\text{SRIO\_TXD0}}$										V_{DDSXP}
C14	V_{DDSXP}										V_{DDSXP}
C15	$\overline{\text{SRIO\_TXD1}}$										V_{DDSXP}
C16	GND_{SXC}										GND_{SXC}
C17	GND_{RIOPLL}										GND_{RIOPLL}
C18	Reserved[1]										—
C19	V_{DDSXP}										V_{DDSXP}
C20	$\overline{\text{SRIO\_TXD2}}$/$\overline{\text{GE1\_SGMII\_TX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
K23	MBA2										V_{DDDDR}
K24	MA10										V_{DDDDR}
K25	MA12										V_{DDDDR}
K26	MA14										V_{DDDDR}
K27	MA4										V_{DDDDR}
K28	MV_{REF}										V_{DDDDR}
L1	Reserved[1]										—
L2	CLKOUT										V_{DDIO}
L3	TMR1/UTP_IR/$\overline{\text{PCI\_CBE3}}$/ GPIO17[3, 6]		UTOPIA		TMR/ GPIO	UTOPIA	PCI	UTOPIA			V_{DDIO}
L4	TMR4/PCI_PAR/GPIO20[3, 6]/ UTP_REOP		TIMER/GPIO				PCI	TIMER/GPIO			V_{DDIO}
L5	GND										GND
L6	TMR2/$\overline{\text{PCI\_FRAME}}$/ GPIO18[3, 6]		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
L7	SCL/GPIO26[3, 4, 6]		I^2C/GPIO								V_{DDIO}
L8	UTXD/GPIO15/$\overline{\text{IRQ9}}$[3, 6]		UART/GPIO/IRQ								V_{DDIO}
L9	GND										GND
L10	V_{DD}										V_{DD}
L11	GND										GND
L12	V_{DD}										V_{DD}
L13	GND										GND
L14	V_{DD}										V_{DD}
L15	Reserved[1]										GND
L16	V_{DD}										V_{DD}
L17	GND										GND
L18	V_{DD}										V_{DD}
L19	GND										GND
L20	V_{DD}										V_{DD}
L21	GND										GND
L22	GND										GND
L23	MCKE1										V_{DDDDR}
L24	MA1										V_{DDDDR}
L25	V_{DDDDR}										V_{DDDDR}
L26	GND										GND
L27	V_{DDDDR}										V_{DDDDR}
L28	$\overline{\text{MCK1}}$										V_{DDDDR}
M1	Reserved[1]										—
M2	$\overline{\text{TRST}}$										V_{DDIO}
M3	EE0										V_{DDIO}
M4	EE1										V_{DDIO}
M5	UTP_RCLK/PCI_AD13		UTOPIA		PCI	UTOPIA					V_{DDIO}
M6	UTP_RADDR0/PCI_AD7		UTOPIA		PCI	UTOPIA					V_{DDIO}
M7	UTP_TD8/PCI_AD30		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
V8	V_{DDIO}										V_{DDIO}
V9	Reserved[1]										V_{DDIO}
V10	GND										GND
V11	V_{DDM3}										V_{DDM3}
V12	GND										GND
V13	V_{DDM3}										V_{DDM3}
V14	GND										GND
V15	V_{DDM3}										V_{DDM3}
V16	GND										GND
V17	V_{DDM3}										V_{DDM3}
V18	GND										GND
V19	V_{DDM3}										V_{DDM3}
V20	GND										GND
V21	GND										GND
V22	V_{DDDDR}										V_{DDDDR}
V23	MDQ2										V_{DDDDR}
V24	V_{DDDDR}										V_{DDDDR}
V25	MDQ6										V_{DDDDR}
V26	GND										GND
V27	V_{DDDDR}										V_{DDDDR}
V28	MDQS0										V_{DDDDR}
W1	Reserved[1]										—
W2	UTP_TD12/$\overline{\text{PCI\_CBE2}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W3	UTP_TD11/$\overline{\text{PCI\_CBE1}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W4	V_{DDIO}										V_{DDIO}
W5	GND										GND
W6	UTP_TD15/$\overline{\text{PCI\_IRDY}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W7	UTP_TD0/$\overline{\text{PCI\_SERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
W8	UTP_RSOC/PCI_AD22		UTOPIA		PCI	UTOPIA					V_{DDIO}
W9	Reserved[1]										V_{DDIO}
W10	V_{DDM3}										V_{DDM3}
W11	GND										GND
W12	V_{25M3}										V_{25M3}
W13	GND										GND
W14	V_{DDM3}										V_{DDM3}
W15	V_{25M3}										V_{25M3}
W16	V_{DDM3}										V_{DDM3}
W17	GND										GND
W18	V_{25M3}										V_{25M3}
W19	GND										GND
W20	V_{DDM3}										V_{DDM3}
W21	GND										GND
W22	GND										GND

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8144 Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8144.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{dd}	–0.3 to 1.1	V
PLL supply voltage[3]	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1	V
M3 memory Internal voltage	V_{DDM3}	–0.3 to 1.32	V
DDR memory supply voltage • DDR mode • DDR2 mode	V_{DDDDR}	 –0.3 to 2.75 –0.3 to 1.98	 V V
DDR reference voltage	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage	V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
Ethernet 1 I/O voltage	V_{DDGE1}	–0.3 to 3.465	V
Input Ethernet 1 I/O voltage	V_{INGE1}	–0.3 to V_{DDGE1} + 0.3	V
Ethernet 2 I/O voltage	V_{DDGE2}	–0.3 to 3.465	V
Input Ethernet 2I/O voltage	V_{INGE2}	–0.3 to V_{DDGE2} + 0.3	V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	–0.3 to 3.465	V
Input I/O voltage	V_{INIO}	–0.3 to V_{DDIO} + 0.3	V

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8144.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8144.

Note: DDR SDRAM uses V_{DDDDR}(typ) = 2.5 V and DDR2 SDRAM uses V_{DDDDR}(typ) = 1.8 V.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MSC8144 when V_{DDDDR}(typ) = 1.8 V.

Table 6. DDR2 SDRAM DC Electrical Characteristics for V_{DDDDR} (typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage[1]	V_{DDDDR}	1.7	1.9	V
I/O reference voltage[2]	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage[3]	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V
Output leakage current[4]	I_{OZ}	–50	50	µA
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}.
4. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

2.5.2.2 Spread Spectrum Clock

SRIO_REF_CLK/ $\overline{\text{SRIO\_REF\_CLK}}$ is designed to work with a spread spectrum clock (0 to 0.5% spreading at 3033 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

2.5.3 PCI DC Electrical Characteristics

Table 9. PCI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDPCI}	3.135	3.465	V
Input high voltage	V_{IH}	$0.5 \times V_{DDPCI}$	3.465	V
Input low voltage	V_{IL}	–0.5	$0.3 \times V_{DDPCI}$	V
Input Pull-up voltage[1]	V_{IPU}	$0.7 \times V_{DDPCI}$		
Input leakage current, $0<V_{IN}<V_{DDPCI}$	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current, $0<V_{IN}<V_{DDPCI}$	I_{OZ}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.0 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –0.5 mA, except open drain pins	V_{OH}	$0.9 \times V_{DDPCI}$	—	V
Output low voltage, I_{OL}= 1.5 mA	V_{OL}	—	$0.1 \times V_{DDPCI}$	V
Input Pin Capacitance[1]	C_{IN}		10	pF

Notes: **1.** Not tested. Guaranteed by design.

2.5.4 TDM DC Electrical Characteristics

Table 10. TDM DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDTDM}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current $0<V_{IN}<V_{DDTDM}$	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current	I_{OZ}	–30	30	µA
Output high voltage, I_{OH} = –1.6 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL}= 0.4mA	V_{OL}	—	0.4	V

2.5.6 ATM/UTOPIA/POS DC Electrical Characteristics

Table 13. ATM/UTOPIA/POS DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.4 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –4 mA	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 4 mA	V_{OL}	—	0.5	V

Notes: **1.** Not tested. Guaranteed by design.

2.5.7 SPI DC Electrical Characteristics

Table 14 provides the SPI DC electrical characteristics.

Table 14. SPI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}		30	µA
Output high voltage, I_{OH} = –4.0 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 4.0 mA	V_{OL}	—	0.5	V

2.5.8 GPIO, UART, TIMER, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, JTAG Ports DC Electrical Characteristics

Table 15. GPIO, UART, Timer, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, and JTAG Port[1] DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current, V_{IN} = supply voltage	I_{OZ}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[2]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–30	30	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0.4	V

Notes: **1.** This does not include TDI and TMS, which have internal pullup resistors.
2. Not tested. Guaranteed by design.

Table 18. Reset Actions for Each Reset Source (continued)

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTEST, CLAMP, or HIGHZ
HRESET driven	Yes	Yes	No	No
IPBus modules reset (TDM, UART, SWT, DDRC, IPBus master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
SRESET driven	Yes	Yes	Yes	Depends on command
Extended cores reset	Yes	Yes	Yes	Yes
CLASS registers reset	Yes	Yes	Some registers	Some registers
Timers, Performance Monitor	Yes	Yes	No	No
QUICC Engine subsystem, PCI, DMA	Yes	Yes	Most registers	Most registers

2.6.3.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 32 CLKIN cycles after V_{DD} and V_{DDIO} are both at their nominal levels.

2.6.3.2 Reset Configuration

The MSC8144 has two mechanisms for writing the reset configuration:

- Through the I^2C port
- Through external pins
- Through internal hard coded

Twenty-three signals (see **Section 1** for signal description details) are sampled during the power-on reset sequence to define the Reset Word Configuration Source and operating conditions:

- RCW_SRC[2–0]
- RC[16–0]

The RCFG_CLKIN_RNG pin must be valid during power-on or hard reset sequence. The STOP_BS pin must be always valid and is also sampled during power-on reset sequence for RCW loading from an I^2C EEPROM.

2.6.3.3 Reset Timing Tables

Table 19 and Figure 7 describe the reset timing for a reset configuration.

Table 19. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Max	Min	Unit
1	Required external PORESET duration minimum	32/CLKIN			
	• 33 MHz <= CLKIN < 44 MHz		1280	727	ns
	• 44 MHz <= CLKIN < 66 MHz		728	484	ns
	• 66 MHz <= CLKIN < 100 MHz		485	320	ns
	• 100 MHz <= CLKIN < 133 MHz		320	241	ns

Figure 8 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

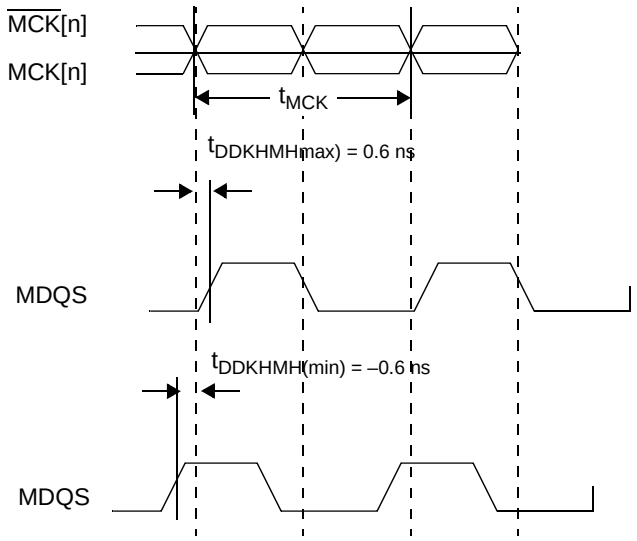


Figure 8. Timing for t_{DDKHMH}

Figure 9 shows the DDR SDRAM output timing diagram.

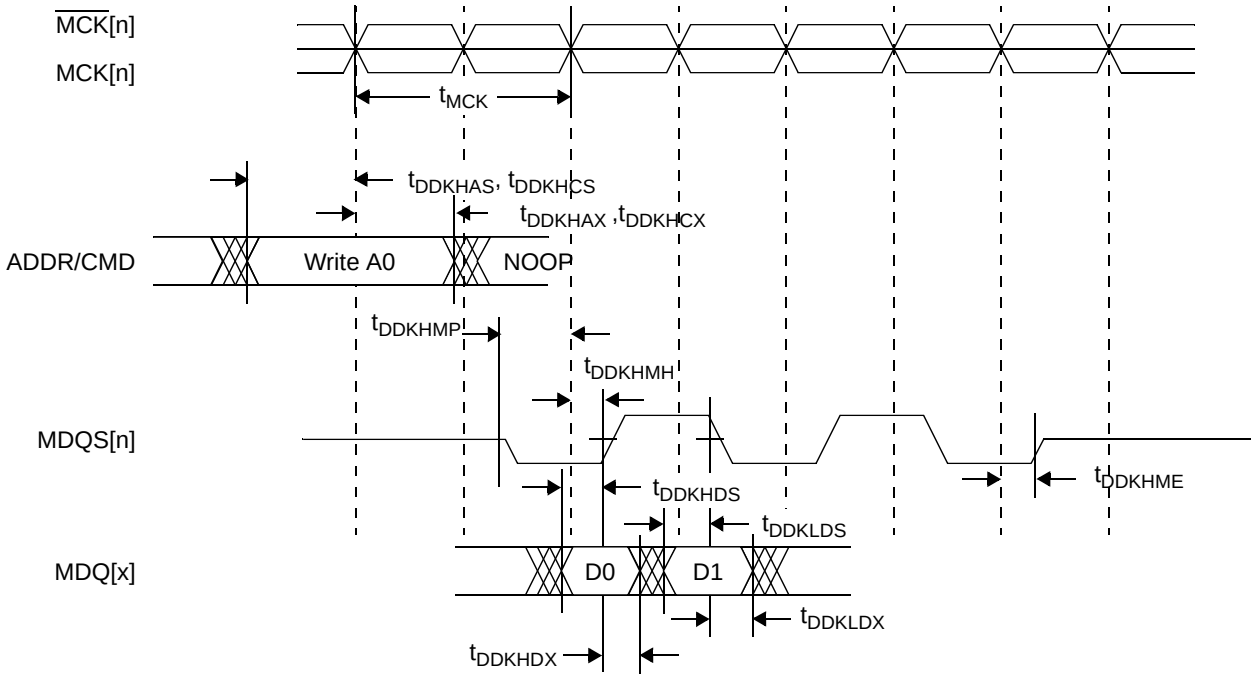


Figure 9. DDR SDRAM Output Timing

Table 34. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV_{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI_{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI_{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI_{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	±100 ppm

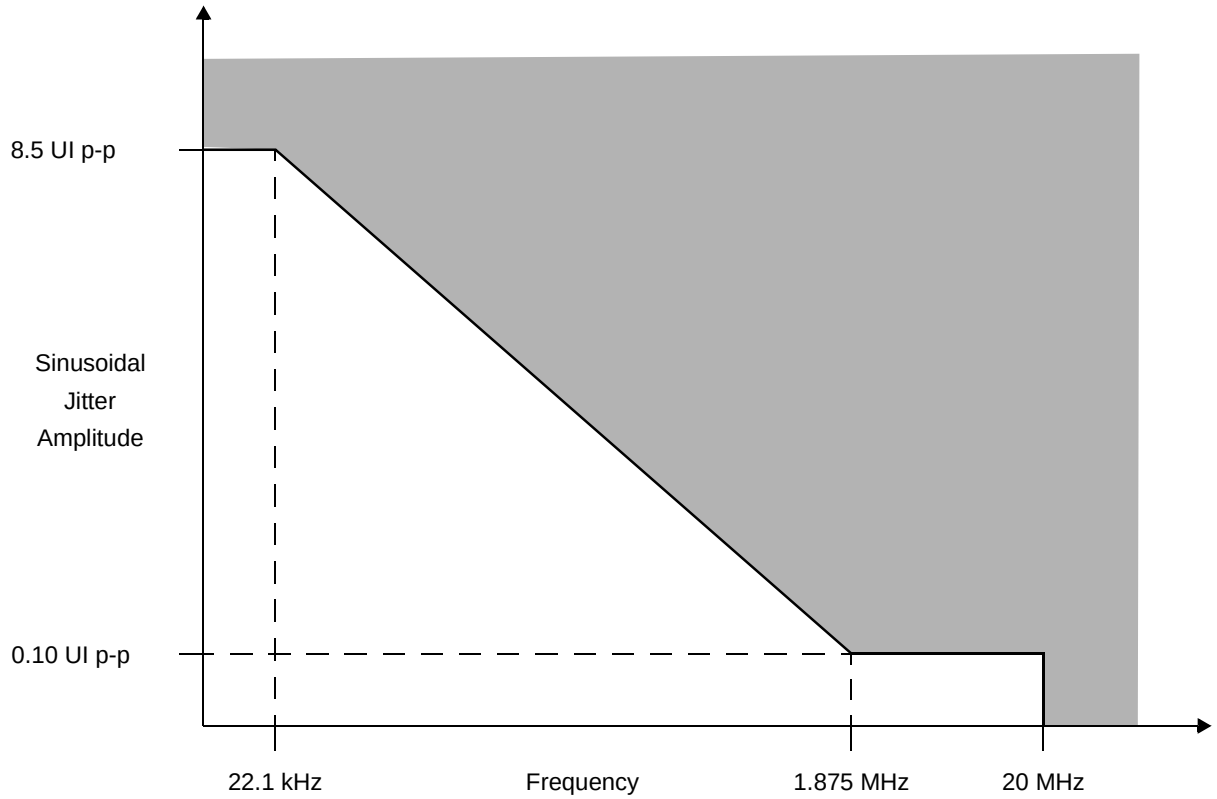


Figure 13. Single Frequency Sinusoidal Jitter Limits

Figure 28 shows the RMII transmit and receive AC timing diagram.

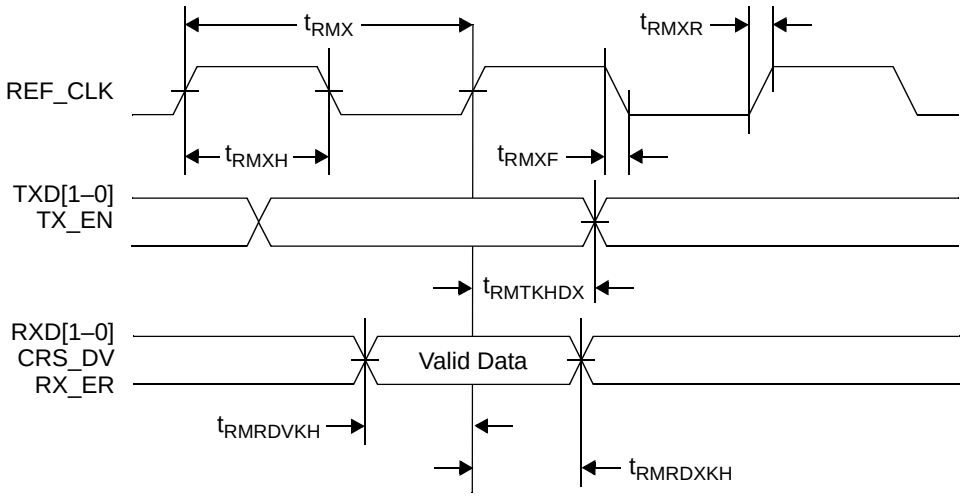


Figure 28. RMII Transmit and Receive AC Timing

Figure 29 provides the AC test load.

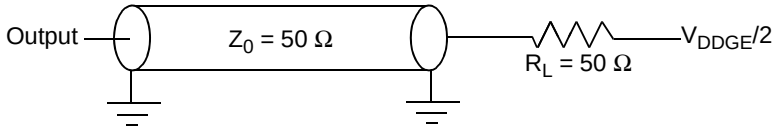


Figure 29. AC Test Load

2.6.10.5 SMII AC Timing Specification

Table 44. SMII Mode Signal Timing

Characteristics	Symbol	Min	Max	Unit
ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge setup time	t_{SMDVKH}	1.5	—	ns
ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	t_{SMDXKH}	1.0	—	ns
ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	t_{SMXR}	1.5	5.0	ns

Notes:
1. Typical REF_CLK clock period is 8ns
2. Measured using a 5 pF load.
3. Measured using a 15 pF load
4. Program GCR4 as 0x00002008

Figure 30 shows the SMII Mode signal timing.

Figure 31 shows the RGMII AC timing and multiplexing diagrams.

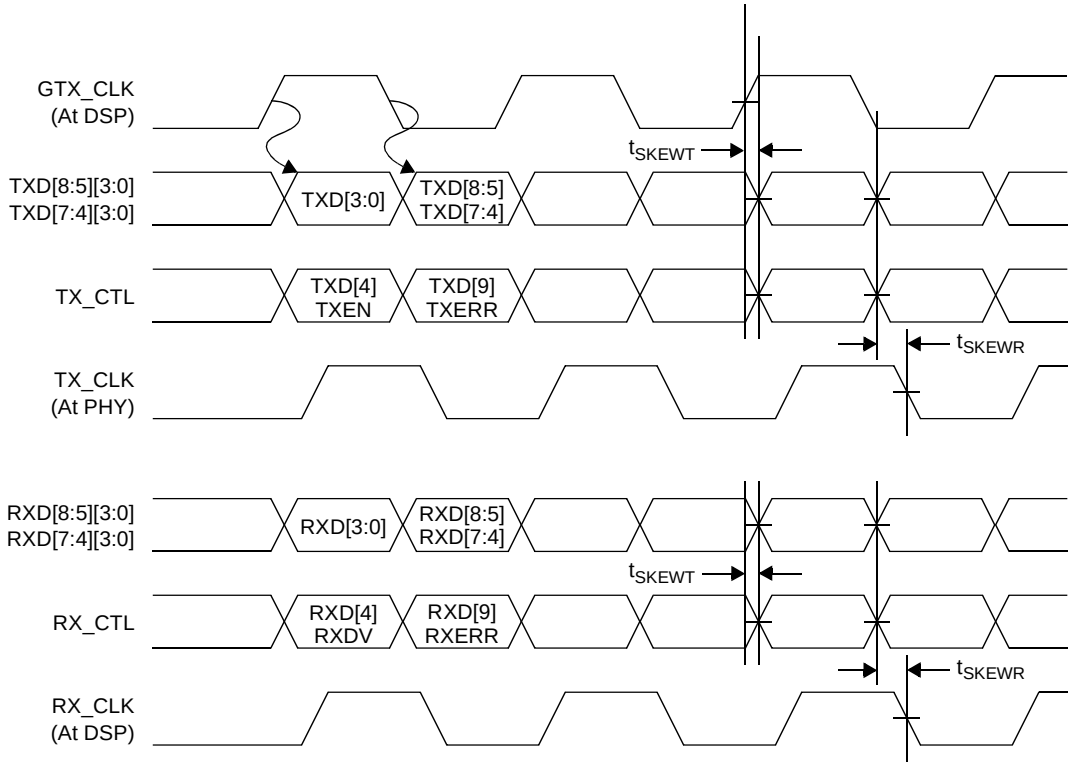


Figure 31. RGMII AC Timing and Multiplexing

2.6.14 JTAG Signals

Table 50. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at V_M = 1.6 V	t_{TCKH}	15.0	—	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
$\overline{\text{TRST}}$ assert time	t_{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 38 shows the Test Clock Input Timing Diagram

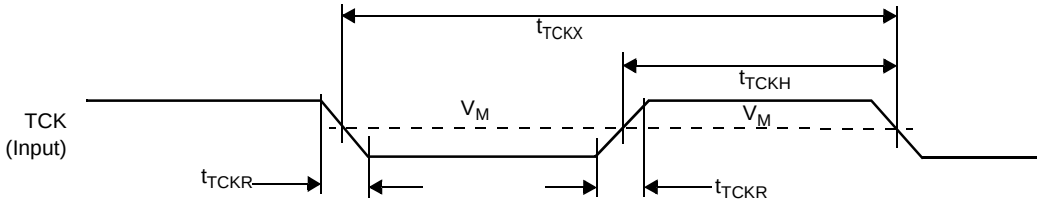


Figure 38. Test Clock Input Timing

Figure 39 shows the boundary scan (JTAG) timing diagram.

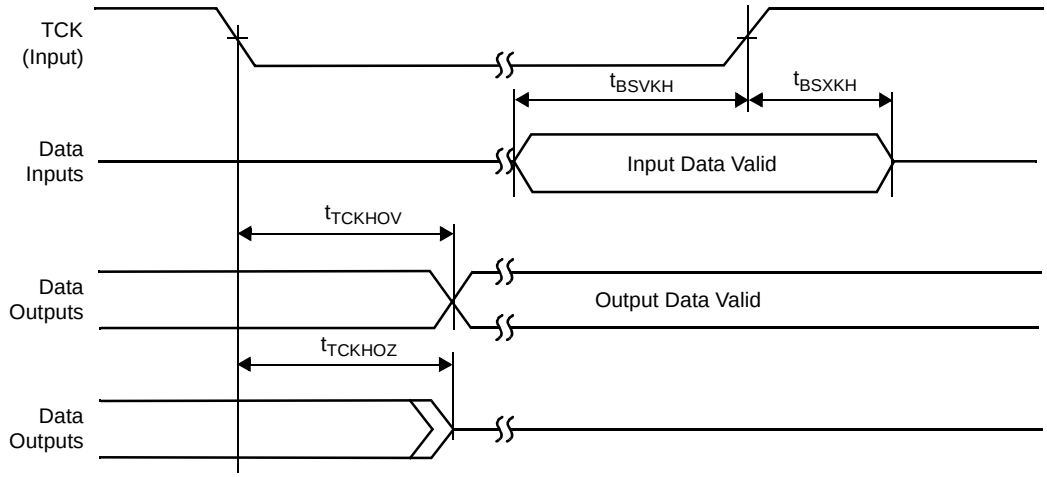


Figure 39. Boundary Scan (JTAG) Timing

Figure 40 shows the test access port timing diagram

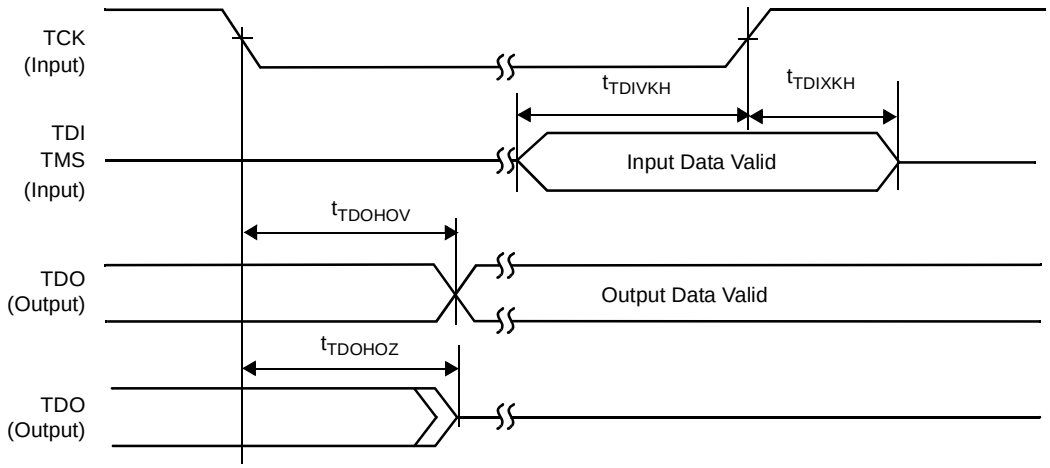


Figure 40. Test Access Port Timing

Figure 41 shows the $\overline{\text{TRST}}$ timing diagram.

Figure 41. $\overline{\text{TRST}}$ Timing

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8144 device is designed into a system.

3.1 Start-up Sequencing Recommendations

3.1.1 Power-on Sequence

Use the following guidelines for power-on sequencing:

- There are no dependencies in power-on/power-off sequence between V_{DDM3} and V_{DD} supplies.
- There are no dependencies in power-on/power-off sequence between RapidIO supplies: V_{DDSXC}, V_{DDSXP}, $V_{DDRIOPLL}$ and other MSC8144 supplies.
- V_{DDPLL} should be coupled with the V_{DD} power rail with extremely low impedance path.

External voltage applied to any input line must not exceed the related to this port I/O supply by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8144 device in the system during start-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4 V/ns.

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

  Rterm = Rim – Rbuf

  where Rim = trace characteristic impedance

  Rbuf = clock buffer internal impedance.

Note: See *MSC8144 CLKIN and PCI_CLK_IN Board Layout* (AN3440) for an example layout.

3.4 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

1. GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
2. V_{DD} indicates using a 10 kΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor it is clearly indicated as “pull-up/pull-down”.
4. NC indicates “not connected” and means do not connect anything to the pin.
5. The phrase “in use” indicates a typical pin connection for the required function.

Note: Please see recommendations #1 and #2 as mandatory pull-down or pull-up connection for unused pins in case of subset interface connection.

3.4.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with DDR1 and DDR2 memory.

Note: For information about unused differential/non-differential pins in DDR1/DDR2 modes (that is, unused negative lines of strobes in DDR1), please refer to Table 51.

3.4.1.1 DDR Interface Is Not Used

Table 51. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–31]	NC
MDQS[0–3]	NC
$\overline{\text{MDQS[0–3]}}$	NC
MA[0–15]	NC
MCK[0–2]	NC
$\overline{\text{MCK[0–2]}}$	NC
$\overline{\text{MCS[0–1]}}$	NC

Table 51. Connectivity of DDR Related Pins When the DDR Interface Is Not Used (continued)

Signal Name	Pin Connection
MDM[0–3]	NC
MBA[0–2]	NC
$\overline{\text{MCAS}}$	NC
MCKE[0–1]	NC
MODT[0–1]	NC
MDIC[0–1]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[0–7]	NC
ECC_MDM	NC
ECC_MDQS	NC
$\overline{\text{ECC\_MDQS}}$	NC
MV_{REF}	GND
V_{DDDDR}	GND
Note: If the DDR controller is not used, disable the internal DDR clock by writing a 1 to the CLK11DIS bit in the System Clock Control Register (SCCR[CLK!11DIS]). See **Chapter 7**, *Clocks*, in the ***MSC8144 Reference Manual*** for details.	

3.4.1.2 16-Bit DDR Memory Only

Table 52 lists unused pin connection when using 16-bit DDR memory. The 16 most significant data lines are not used.

Table 52. Connectivity of DDR Related Pins When Using 16-bit DDR Memory Only

Signal Name	Pin connection
MDQ[0–15]	in use
MDQ[16–31]	pull-up to V_{DDDDR}
MDQS[0–1]	in use
MDQS[2–3]	pull-down to GND
$\overline{\text{MDQS[0–1]}}$	in use
$\overline{\text{MDQS[2–3]}}$	pull-up to V_{DDDDR}
MA[0–15]	in use
MCK[0–2]	in use
$\overline{\text{MCK[0–2]}}$	in use
$\overline{\text{MCS[0–1]}}$	in use
MDM[0–1]	in use
MDM[2–3]	NC
MBA[0–2]	in use
$\overline{\text{MCAS}}$	in use
MCKE[0–1]	in use
MODT[0–1]	in use
MDIC[0–1]	in use
$\overline{\text{MRAS}}$	in use

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	NC
GE2_TD[0–3]	NC
GE2_TX_EN	NC

3.4.4.3 GE1 and GE2 Management Pins

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used (that is, V_{DDGE2} is connected to GND), Table 61 lists the recommended management pin connections.

Table 61. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

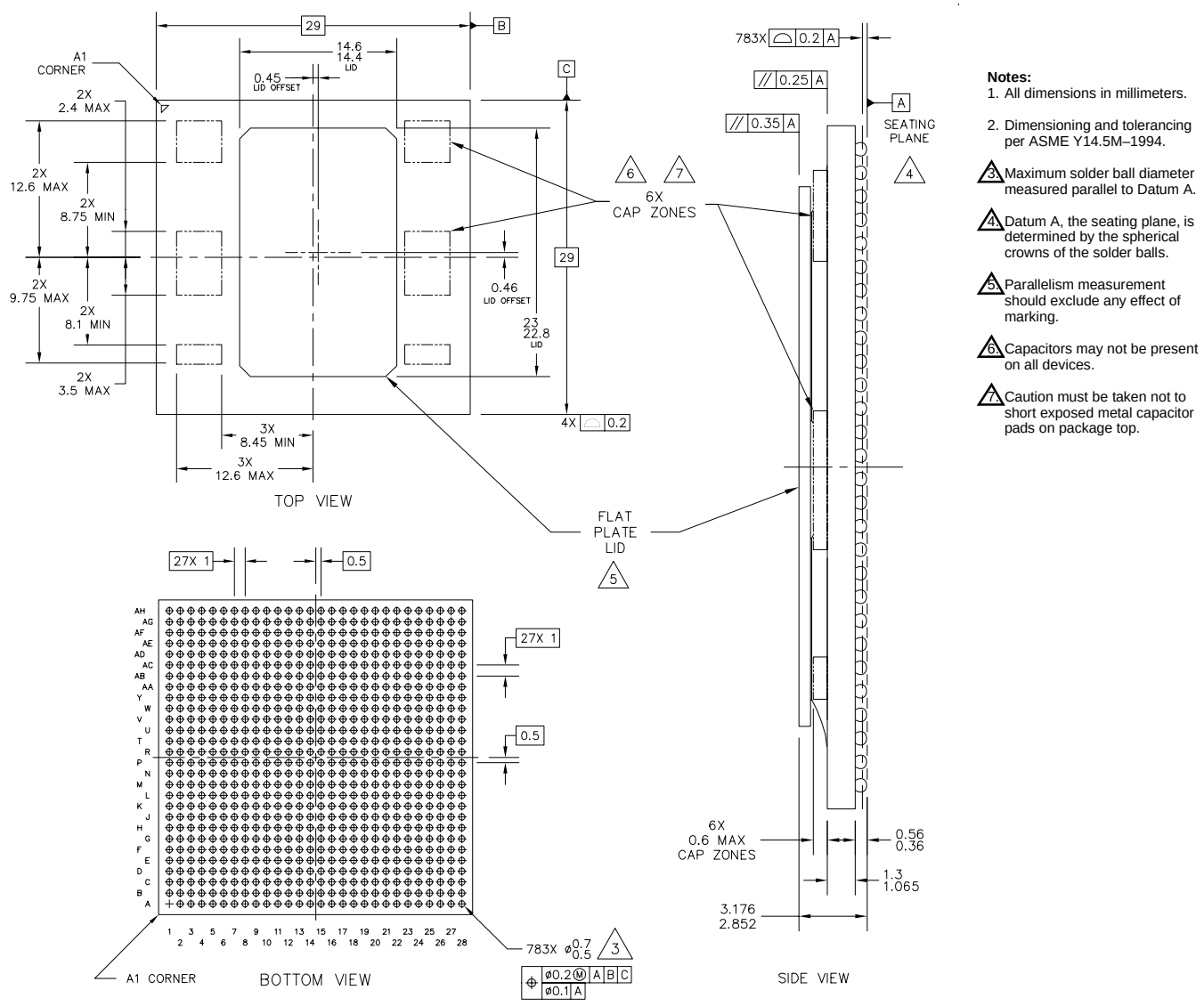
3.4.5 UTOPIA/POS Related Pins

Table 62 lists the board connections of the UTOPIA/POS pins when the entire UTOPIA/POS interface is not used or subset of UTOPIA/POS interface is used. For multiplexing options that select a subset of the UTOPIA/POS interface, use the connections described in Table 62 for those signals that are not selected. Table 62 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 62. Connectivity of UTOPIA/POS Related Pins When UTOPIA/POS Interface Is Not Used

Signal Name	Pin Connection
UTP_IR	GND
UTP_RADDR[0–4]	V_{DDIO}
UTP_RCLAV_PDRPA	NC
UTP_RCLK	GND
UTP_RD[0–15]	GND
$\overline{\text{UTP\_REN}}$	V_{DDIO}
UTP_RPRTY	GND
UTP_RSOC	GND
UTP_TADDR[0–4]	V_{DDIO}
UTP_TCLAV	NC
UTP_TCLK	GND
UTP_TD[0–15]	NC
$\overline{\text{UTP\_TEN}}$	V_{DDIO}
UTP_TPRTY	NC
UTP_TSOC	NC
V_{DDIO}	3.3 V

5 Package Information



Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement should exclude any effect of marking.
6. Capacitors may not be present on all devices.
7. Caution must be taken not to short exposed metal capacitor pads on package top.

CASE NO. 1842-04

Figure 44. MSC8144 Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

- *MSC8144 Technical Data Sheet* (MSC8144). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8144 device.
- *MSC8144 Reference Manual* (MSC8144RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes.* Cover various programming topics related to the StarCore DSP core and the MSC8144 device.
- *SC3400 DSP Core Reference Manual*. Covers the SC3400 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8144 SC3400 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

Table 66. Document Revision History (continued)

Rev.	Date	Description
7	Dec 2007	• Changed minimum voltage level for V_{DDM3} to 1.213 (1.25 – 3%) in Table 3. • Added POS to titles in **Section 2.6.6**. • Added additional signals to titles in **Section 2.6.8**. Added high and low voltage ranges to Table 19. • Added ATM and POS to headings in **Section 2.7.11**. Changed characteristics to generic input/output in Table 52, Figure 33, and Figure 34. • Replaced **Sections 2.7.13** and **2.7.14** with new **Section 2.7.13**, *Asynchronous Signal Timing*. Renumbered subsequent sections, tables, and figures. • Added POS to all UTOPIA references in **Section 3.4.5**.
8	Dec 2007	• Changed GCR4 program value to 0x0004C130 in Note 7 in Table 51.
9	Mar 2008	• Changed description of Table 20 in **Section 2.7.2**.
10	Apr 2008	• Added [3] to the PLL supply voltage row in **Table 2**. • Changed the first sentence in **Section 3.4.8** to reflect that **Table 70** indicates what to do with pins if they are "not" required by the design. Changed the Pin Connection for GPIO[0–31] to GND. • Updated ordering information in **Section 4**. • Multiple corrections of minor punctuation errors.
11	Aug 2008	• Removed the comment about preliminary estimates before Table 4 and removed non-DDR rows in the table. • Table 9 and Table 11 for DDR and DDR2 SDRAM capacitance removed and subsequent tables renumbered. • Changed units for I_{OH} and I_{OL} to mA in Table 9. • Removed signal low and high input current from Table 12. • Added a note to Table 15 to exclude TDM and TMS. Removed reference to overshoot and undershoot and associated figure. • Changed minimum clock frequency to 33 MHz and maximum clock frequency to 133 MHz in Table 16. • Deleted old Table 17 Clock Parameters. • Changed minimum input clock frequency to 33 MHz in Table 19. • Changed the t_{DDKHAX} minimum value in Table 23 to 1.85 ns. • Removed t_{REFPJ} and t_{REFCJ} from Table 24 because the specifications are not required or tested. • Removed $t_{PCRSTCLK}$, $t_{PCRSTOFF}$, t_{PCRST}, and t_{PCRHFA} from Table 36 because the specifications are not required or tested. • Removed t_{UAVKH} and t_{UAVXH} from Table 38 because the specifications are not required or tested. • The parameters t_{MDCH}, t_{MDCR}, and t_{MDHF} were removed from Table 40 because the specifications are not required or tested. • The parameters t_{MTXH}/t_{MTX}, t_{MTXR}, and t_{MTXF} were removed from Table 41 because the specifications are not required or tested. • The parameters t_{MRXH}/t_{MRX}, t_{MRXR}, and t_{MRXF} were removed from Table 42 because the specifications are not required or tested. • The parameters t_{RMXH}/t_{RMX}, t_{RMXR}, and t_{RMXF} were removed from Table 43 because the specifications are not required or tested. • Removed the parameters t_{RGT}, t_{RGTH}/t_{RGT} (1000Base-T), t_{RGTH}/t_{RGT} (10Base-T), t_{RGTR}, t_{RGTF}, t_{G12}, and t_{G125H}/t_{G125} were removed from Table 45 and Table 46 because the specifications are not required or tested. • Changed t_{UEKHOX} to guaranteed by design in Table 47. • Updated Figure 35 and Figure 36 SPI timing diagrams. • Removed TCK rise and fall time from Table 50. • Updated orderable part numbers in **Section 4**.
12	Aug 2008	• Changed b8t to bit in the M3 memory description on the first page. • Changed maximum input high voltage (VIH) for SPI to 3.465 in the first row of Table 14. • Changed packet processor to QUICC Engine Subsystem in the last row of Table 18.
13	Feb 2009	• In Figure 31, for GTX_CLK, changed (at transmitter) to (at DSP) and for RX_CLK, changed (at PHY) to (at DSP). • Updated package drawing to the latest revision, Case No. 1842-04 in Figure 44.
14	Jul 2009	• Updated MV_{REF} equations and temperature ranges in Table 3. • Updated orderable part numbers to **Section 4**.
15	Nov 2009	• Updated Core and PLL input voltage tolerance in Table 3.
16	May 2010	• Corrected typo in Table 23. Changed MCLK minimum time to 5 ns.