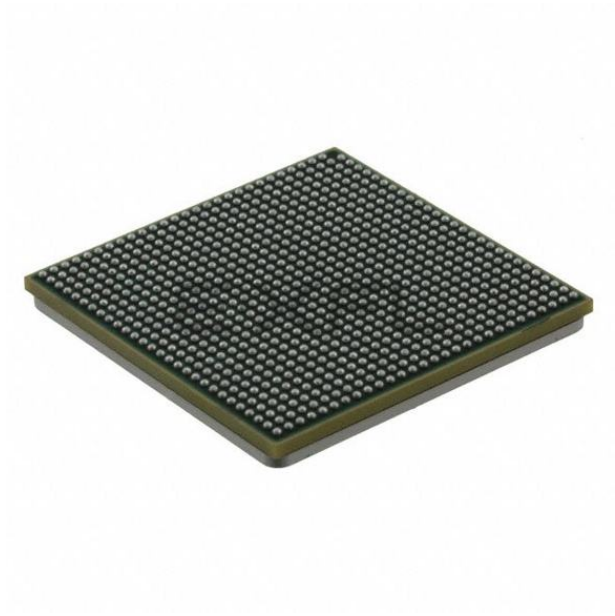


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	EBI/EMI, Ethernet, I²C, PCI, Serial RapidIO, SPI, TDM, UART, UTOPIA
Clock Rate	800MHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8144tvt800a

Table of Contents

List of Figures

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
C21	V_{DDSXP}										V_{DDSXP}
C22	$\overline{SRIO\_TXD3/GE2\_SGMII\_TX}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
C23	V_{DDSXP}										V_{DDSXP}
C24	MDQ26										V_{DDDDR}
C25	MDQ25										V_{DDDDR}
C26	MDM3										V_{DDDDR}
C27	GND										GND
C28	MDQ24										V_{DDDDR}
D1	Reserved[1]										—
D2	GE2_RD1/PCI_AD28		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
D3	GND										GND
D4	TDM7TDAT/GE2_TD3/ PCI_AD3/UTP_TMD		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D5	TDM7RDAT/GE2_RD3/ PCI_AD1/UTP_STA		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D6	$\overline{GE1\_RD0}$/UTP_RD2/ $\overline{PCI\_CBE2}$		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
D7	TDM7TCLK/GE2_TCK/ PCI_IDS/UTP_RER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D8	Reserved[1]										—
D9	Reserved[1]										—
D10	Reserved[1]										—
D11	Reserved[1]										—
D12	GND_{SXP}										GND_{SXP}
D13	SRIO_TXD0										V_{DDSXP}
D14	GND_{SXP}										GND_{SXP}
D15	SRIO_TXD1										V_{DDSXP}
D16	V_{DDSXC}										V_{DDSXC}
D17	Reserved[1]										—
D18	Reserved[1]										—
D19	GND_{SXP}										GND_{SXP}
D20	SRIO_TXD2/GE1_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D21	GND_{SXP}										GND_{SXP}
D22	SRIO_TXD3/GE2_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D23	GND_{SXP}										GND_{SXP}
D24	MDQ23										V_{DDDDR}
D25	V_{DDDDR}										V_{DDDDR}
D26	MDQ22										V_{DDDDR}
D27	MDQ21										V_{DDDDR}
D28	$\overline{MDQS2}$										V_{DDDDR}
E1	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E6	V_{DDGE1}										V_{DDGE1}
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E8	Reserved[1]										—
E9	Reserved[1]										—
E10	GND										GND
E11	V_{DD}										V_{DD}
E12	GND										GND
E13	V_{DD}										V_{DD}
E14	GND										GND
E15	V_{DD}										V_{DD}
E16	GND										GND
E17	V_{DD}										V_{DD}
E18	GND										GND
E19	V_{DD}										V_{DD}
E20	GND										GND
E21	V_{DD}										V_{DD}
E22	GND										GND
E23	V_{DDDDR}										V_{DDDDR}
E24	MDQ20										V_{DDDDR}
E25	GND										GND
E26	V_{DDDDR}										V_{DDDDR}
E27	GND										GND
E28	MDQS2										V_{DDDDR}
F1	Reserved[1]										—
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F3	V_{DDGE1}										V_{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F6	GND										GND
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F8	V_{DDGE1}										V_{DDGE1}
F9	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AB19	V_{DDM3}										V_{DDM3}
AB20	GND										GND
AB21	GND										GND
AB22	V_{DDDDR}										V_{DDDDR}
AB23	MECC7										V_{DDDDR}
AB24	MECC1										V_{DDDDR}
AB25	MECC4										V_{DDDDR}
AB26	MECC5										V_{DDDDR}
AB27	MECC2										V_{DDDDR}
AB28	ECC_MDQS										V_{DDDDR}
AC1	Reserved[1]										—
AC2	UTP_RD9/RC13	RC13	UTOPIA								V_{DDIO}
AC3	UTP_RD8/RC12	RC12	UTOPIA								V_{DDIO}
AC4	TDM6TCLK/PCI_AD22		TDM			PCI		TDM			V_{DDIO}
AC5	TDM6RSYN/PCI_AD21/ GPIO6/ $\overline{IRQ12}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AC6	V_{DDIO}										V_{DDIO}
AC7	TDM3TSYN/RC11	RC11	TDM								V_{DDIO}
AC8	PCI_AD23/GPIO7/$\overline{IRQ13}$/ TDM6TDAT[3, 6]/UTP_RMOD		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ		UTOPIA	V_{DDIO}
AC9	TDM7TSYN/ PCI_AD4		TDM		PCI			reserved			V_{DDIO}
AC10	V_{DDM3IO}										V_{DDM3IO}
AC11	GND										GND
AC12	V_{DDM3}										V_{DDM3}
AC13	GND										GND
AC14	V_{DDM3}										V_{DDM3}
AC15	GND										GND
AC16	V_{DDM3}										V_{DDM3}
AC17	GND										GND
AC18	V_{DDM3}										V_{DDM3}
AC19	GND										GND
AC20	V_{DDM3IO}										V_{DDM3IO}
AC21	Reserved[1]										—
AC22	MECC6										V_{DDDDR}
AC23	MECC3										V_{DDDDR}
AC24	ECC_MDM										V_{DDDDR}
AC25	V_{DDDDR}										V_{DDDDR}
AC26	MECC0										V_{DDDDR}
AC27	V_{DDDDR}										V_{DDDDR}
AC28	$\overline{ECC\_MDQS}$										V_{DDDDR}
AD1	Reserved[1]										—
AD2	GPIO1[3, 6]		GPIO								V_{DDIO}
AD3	TMR0/GPIO13		TIMER/GPIO								V_{DDIO}

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
M3 memory I/O and M3 memory charge pump voltage	V_{DDM3IO} V_{25M3}	–0.3 to 2.75	V
Input M3 memory I/O voltage	V_{INM3IO}	–0.3 to V_{DDM3IO} + 0.3	V
Rapid I/O C voltage	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O P voltage	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	–0.3 to 1.21	V
Operating temperature	T_J	–40 to 105	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8144 (see Figure 43)

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage • 800 MHz (VT, SVT, TVT) and 1000 MHz (VT) • 1000 MHz (SVT, TVT)	V_{DD}	 0.97 0.97	 1.0 1.0	 1.05 1.03	 V V
PLL supply voltage • 800 MHz (VT, SVT, TVT) and 1000 MHz (VT) • 1000 MHz (SVT, TVT)	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	 0.97 0.97	 1.0 1.0	 1.05 1.03	 V V
M3 memory Internal voltage	V_{DDM3}	1.213	1.25	1.313	V
DDR memory supply voltage • DDR mode • DDR2 mode DDR reference voltage	V_{DDDDR} MV_{REF}	 2.375 1.71 0.49 × V_{DDDDR} (nom)	 2.5 1.8 0.5 × V_{DDDDR} (nom)	 2.625 1.89 0.51 × V_{DDDDR} (nom)	 V V V
Ethernet 1 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE1}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
Ethernet 2 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE2}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	3.135	3.3	3.465	V
M3 memory I/O and M3 charge pump voltage	V_{DDM3IO} V_{25M3}	2.375	2.5	2.625	V
Rapid I/O C voltage	V_{DDSXC}	0.97	1.0	1.05	V
Rapid I/O P voltage • Short run (haul) mode • Long run (haul) mode	V_{DDSXP}	 0.97 1.14	 1.0 1.2	 1.05 1.26	 V V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	0.97	1.0	1.05	V
Operating temperature range: • Standard (VT) • Intermediate (SVT) • Extended (TVT)	 T_J T_J T_A T_J	 0 0 –40 —		 90 105 — 105	 °C °C °C °C

Note: PLL supply voltage is specified at input of the filter and not at pin of the MSC8144 (see Figure 43).

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8144.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8144.

Note: DDR SDRAM uses V_{DDDDR}(typ) = 2.5 V and DDR2 SDRAM uses V_{DDDDR}(typ) = 1.8 V.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MSC8144 when V_{DDDDR}(typ) = 1.8 V.

Table 6. DDR2 SDRAM DC Electrical Characteristics for V_{DDDDR} (typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage[1]	V_{DDDDR}	1.7	1.9	V
I/O reference voltage[2]	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage[3]	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V
Output leakage current[4]	I_{OZ}	–50	50	µA
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}.
4. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

2.6 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs.

2.6.1 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.6.2** describes the clocking characteristics. **Section 2.6.3** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8144 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence using the V_{DDIO} (3.3 V) supply. See Table 19 for timing. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. During functional operation when JTAG is not used, $\overline{\text{TRST}}$ can be asserted and remain asserted after the power ramp.

Note: For applications that use M3 memory, $\overline{\text{M3\_RESET}}$ should replicate the $\overline{\text{PORESET}}$ sequence timing, but using the V_{DDM3IO} (2.5 V) supply. See **Section 3.1.1**, *Power-on Sequence* for additional design information.

- CLKIN should start toggling at least 32 cycles before the $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see Figure 6). 32 cycles should be accounted only after V_{DDIO} reaches its nominal value.
- CLKIN and PCI_CLK_IN should either be stable low during the power-up of V_{DDIO} supply and start their swings after power-up or should swing within V_{DDIO} range during V_{DDIO} power-up., so their amplitude grows as V_{DDIO} grows during power-up.

Figure 6 shows a sequence in which V_{DDIO} is raised after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

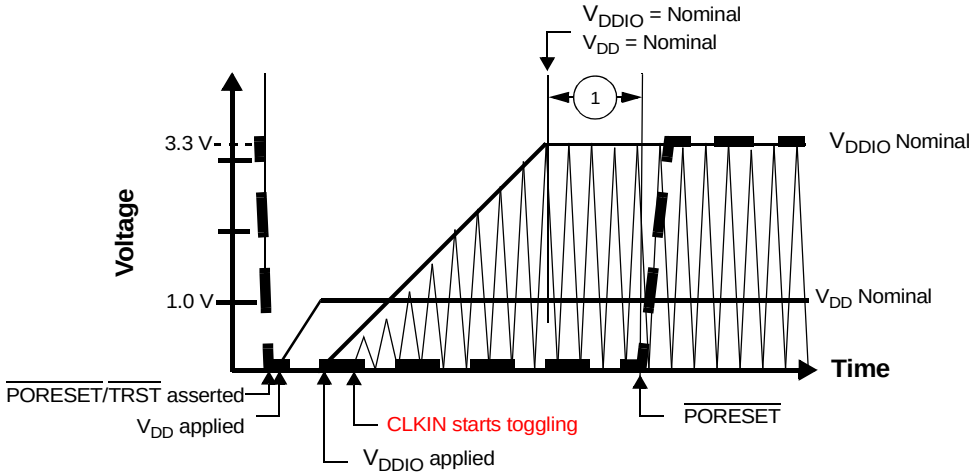


Figure 6. Start-Up Sequence with V_{DD} Raised Before V_{DDIO} with CLKIN Started with V_{DDIO}

2.6.2 Clock and Timing Signals

The following sections include a description of clock signal characteristics. Table 16 shows the maximum frequency values for CLKIN and PCI_CLK_IN. The user must ensure that maximum frequency values are not exceeded.

Table 16. Clock Frequencies

Characteristic	Symbol	Min	Max	Unit
CLKIN frequency	F_{CLKIN}	33	133	MHz
PCI_CLK_IN frequency	$F_{PCI\_CLK\_IN}$	33	133	MHz
CLKIN duty cycle	D_{CLKIN}	40	60	%
PCI_CLK_IN duty cycle	$D_{PCI\_CLK\_IN}$	40	60	%

2.6.4 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.4.1 DDR SDRAM Input Timings

Table 20 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 2.5 V.

Table 20. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V
Note: At recommended operating conditions with V_{DDDDR} of 2.5 ± 5%.				

Table 21 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 21. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.8 ± 5%.				

Table 22 provides the input AC timing specifications for the DDR SDRAM interface.

Table 22. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit
Controller Skew for MDQS—MDQ/MECC/MDM[1]	t_{CISKEW}			
• 400 MHz		–365	365	ps
• 333 MHz		–390	390	ps
• 266 MHz		–428	428	ps
• 200 MHz		–490	490	ps

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) ± 5%

2.6.4.2 DDR SDRAM Output AC Timing Specifications

Table 23 provides the output AC timing specifications for the DDR SDRAM interface.

Table 23. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)[2]	t_{MCK}	5	10	ns
ADDR/CMD output setup with respect to MCK[3]	t_{DDKHAS}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
ADDR/CMD output hold with respect to MCK[3]	t_{DDKHAX}			
• 400 MHz		1.85	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
$\overline{\text{MCS}}$n output setup with respect to MCK[3]	t_{DDKHCS}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
$\overline{\text{MCS}}$n output hold with respect to MCK[3]	t_{DDKHCX}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
MCK to MDQS Skew[4]	t_{DDKHMH}	–0.6	0.6	ns
MDQ/MECC/MDM output setup with respect to MDQS[5]	t_{DDKHDS}, t_{DDKLDS}			
• 400 MHz		700	—	ps
• 333 MHz		900	—	ps
• 266 MHz		1100	—	ps
• 200 MHz		1200	—	ps
MDQ/MECC/MDM output hold with respect to MDQS[5]	t_{DDKHDX}, t_{DDKLDX}			
• 400 MHz		700	—	ps
• 333 MHz		900	—	ps
• 266 MHz		1100	—	ps
• 200 MHz		1200	—	ps
MDQS preamble start[6]	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns
MDQS epilogue end[6]	t_{DDKHME}	–0.6	0.6	ns

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MSC8144 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) ± 5%.

Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD and $\overline{RD}$ each have a peak-to-peak voltage (V_{PP}) swing of A – B.
2. The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$.
3. The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B).
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B.
6. The value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A - B)$ V_{PP}.

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV_{PP}. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV_{PP}.

Note: AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described. The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of **IEEE™** Std 802.3ae-2002™. XAUI has similar application goals to serial RapidIO. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

2.6.5.3 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

2.6.5.4 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section. The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (baud frequency)/10 < freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ freq(f) ≤ baud frequency

The reference impedance for the differential return loss measurements is 100 Ω resistive. Differential return loss includes contributions from internal circuitry, packaging, and any external components related to the driver. The output impedance requirement applies to all valid output levels. It is recommended that the 20–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case. It is also recommended that the timing skew at the output of an LP-Serial transmitter between the two signals comprising a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Table 25. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	

Table 34. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV_{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI_{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI_{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI_{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	±100 ppm

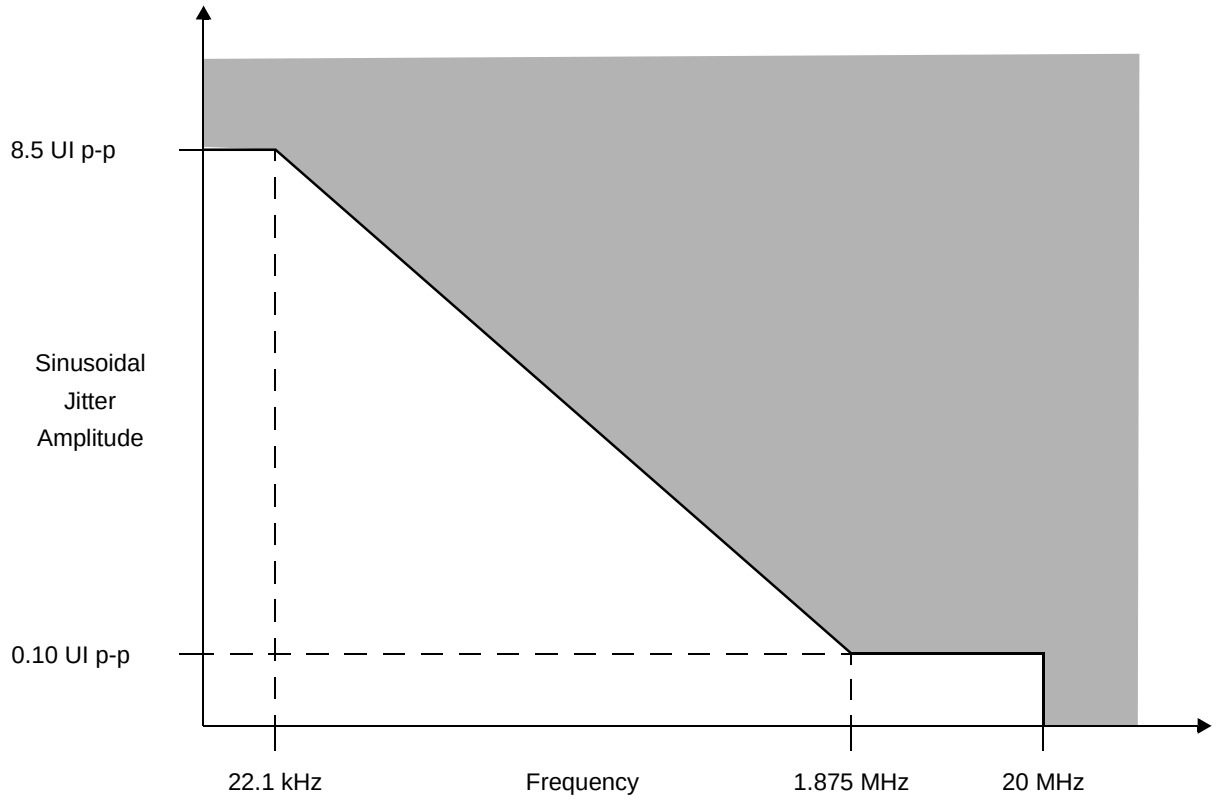


Figure 13. Single Frequency Sinusoidal Jitter Limits

2.6.5.8 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.9 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of **IEEE** Std. 802.3ae.

2.6.5.10 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.11 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in **Section 2.6.5.9** and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 14 and Table 35. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

2.6.6 PCI Timing

This section describes the general AC timing parameters of the PCI bus. Table 36 provides the PCI AC timing specifications.

Table 36. PCI AC Timing Specifications

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
Output delay	t_{PCVAL}	2.0	11.0	1.0	6.0	ns
High-Z to Valid Output delay	t_{PCON}	2.0	—	1.0	—	ns
Valid to High-Z Output delay	t_{PCOFF}	—	28	—	14	ns
Input setup	t_{PCSU}	7.0	—	3.0	—	ns
Input hold	t_{PCH}	0	—	0	—	ns

2.6.9 Timer Timing

Table 39. Timer Timing

Characteristics	Symbol	Min	Unit
TIMERx frequency	$T_{TMREFCLK}$	10.0	ns
TIMERx Input high phase	T_{TMCH}	4.0	ns
TIMERx Output low phase	T_{TMCL}	4.0	ns

Figure 23 shows the timer input AC timing

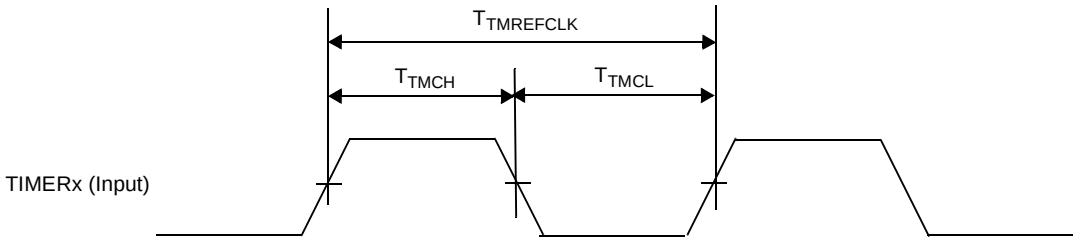


Figure 23. Timer Timing

2.6.10 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each Interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the *MSC8144 Reference Manual*.

2.6.10.1 Management Interface Timing

Table 40. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
ETHMDC to ETHMDIO delay[2]	t_{MDKHDX}	10	70	ns
ETHMDIO to ETHMDC rising edge setup time	t_{MDDVKH}	7	—	ns
ETHMDC rising edge to ETHMDIO hold time	t_{MDDXKH}	0	—	ns

Notes:
1. Program the ETHMDC frequency (f_{MDC}) to a maximum value of 2.5 MHz (400 ns period for t_{MDC}). The value depends on the source clock and configuration of MIIMCFG[MCS] and UPSMR[MDCP]. For example, for a source clock of 400 MHz, to achieve f_{MDC} = 2.5 MHz, program MIIMCFG[MCS] = 0x4 and UPSMR[MDCP] = 0. See the *MSC8144 Reference Manual* for configuration details.
2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns.

2.6.11 ATM/UTOPIA/POS Timing

Table 47 provides the ATM/UTOPIA/POS input and output AC timing specifications.

Table 47. ATM/UTOPIA/POS AC Timing (External Clock) Specifications

Characteristic	Symbol	Min	Max	Unit
Outputs—External clock delay	t_{UEKHOV}	1	9	ns
Outputs—External clock High Impedance[1]	t_{UEKHOX}	1	9	ns
Inputs—External clock input setup time	t_{UEIVKH}	4		ns
Inputs—External clock input hold time	t_{UEIXKH}	1		ns

Notes:
1. Not tested. Guaranteed by design.
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. Although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 32 provides the AC test load for the ATM/UTOPIA/POS.

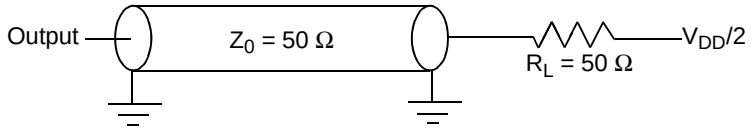


Figure 32. ATM/UTOPIA/POS AC Test Load

Figure 33 shows the ATM/UTOPIA/UTOPIA timing with external clock.

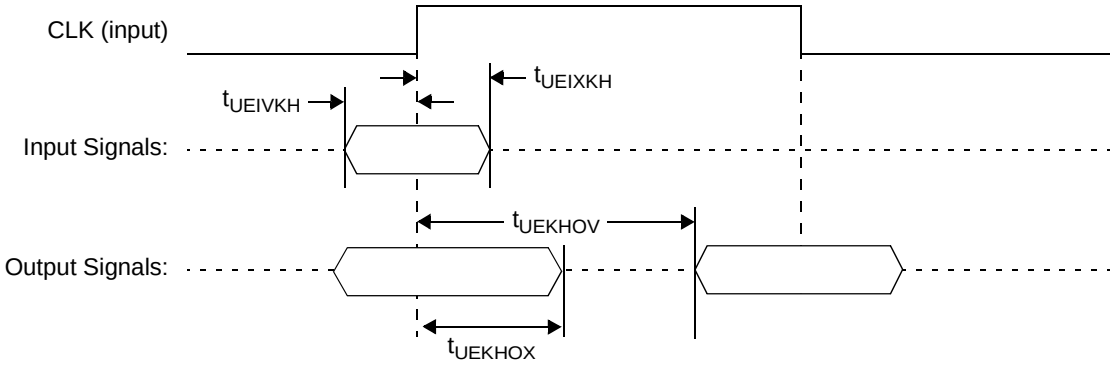


Figure 33. ATM/UTOPIAPOS AC Timing (External Clock)

2.6.14 JTAG Signals

Table 50. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at V_M = 1.6 V	t_{TCKH}	15.0	—	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
$\overline{\text{TRST}}$ assert time	t_{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 38 shows the Test Clock Input Timing Diagram

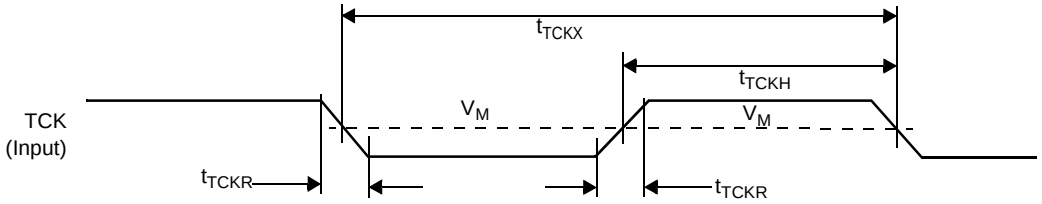


Figure 38. Test Clock Input Timing

Figure 39 shows the boundary scan (JTAG) timing diagram.

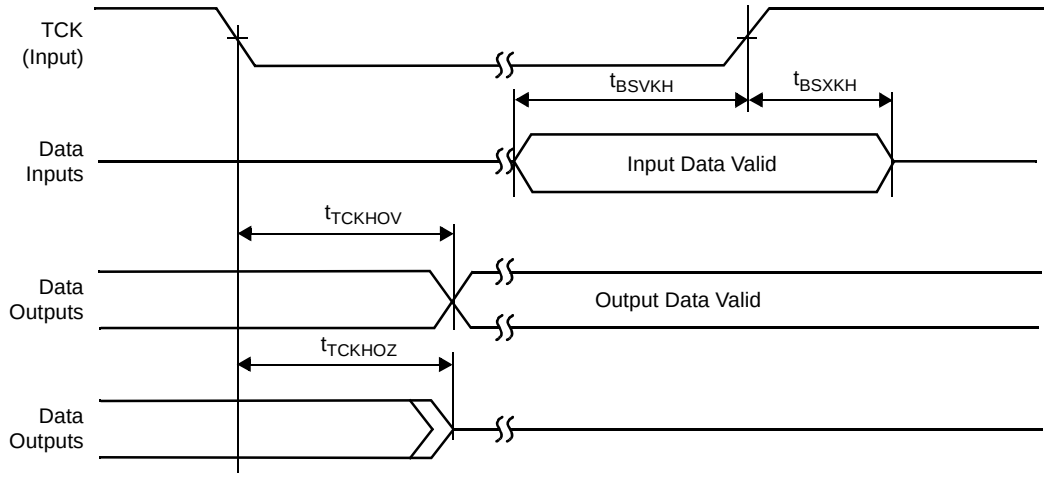


Figure 39. Boundary Scan (JTAG) Timing

The following supplies should rise before any other supplies in any sequence

- V_{DD} and V_{DDPLL} coupled together
- V_{DDM3}

After the above supplies rise to 90% of their nominal value the following I/O supplies may rise in any sequence (see Figure 42):

- V_{DDGE1}
- V_{DDGE2}
- V_{DDIO}
- V_{DDDDR} and MV_{REF} coupled one to another. MV_{REF} should be either at same time or after V_{DDDDR}.
- V_{DDM3IO}
- V_{25M3}

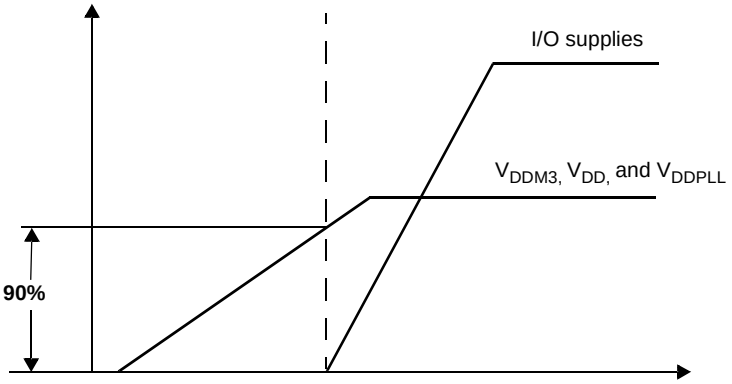


Figure 42. V_{DDM3}, V_{DDM3IO} and V_{25M3} Power-on Sequence

Note:
1. This recommended power sequencing is different from the MSC8122/MSC8126.
2. If no pins that require V_{DDGE1} as a reference supply are used (see Table 1), V_{DDGE1} can be tied to GND.
3. If no pins that require V_{DDGE2} as a reference supply are used (see Table 1), V_{DDGE2} can be tied to GND.
4. If the DDR interface is not used, V_{DDDDR} and MV_{REF} can be tied to GND.
5. If the M3 memory is not used, V_{DDM3}, V_{DDM3IO}, and V_{25M3} can be tied to GND.
6. If the RapidIO interface is not used, V_{DDSX}, V_{DDSXP}, and $V_{DDRIOPLL}$ can be tied to GND.

3.1.2 Start-Up Timing

Section 2.6.1 describes the start-up timing.

Table 58. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
GE1_SGMII_TX	NC
GE1_TD[0-3]	NC
GE1_TX_CLK	GND
GE1_TX_EN	NC
GE1_TX_ER	NC

3.4.4.2 Ethernet Controller 2 (GE2) Related Pins

Note: Table 59 through Table 61 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.4.4.2.1 GE2 interface Is Not Used

Table 59 assumes that the GE2 pins are not used for any purpose (including any multiplexed function) and that V_{DDGE2} is tied to GND.

Table 59. Connectivity of GE2 Related Pins When the GE2 Interface Is Not Used

Signal Name	Pin Connection
GE2_RD[0-3]	NC
GE2_RX_CLK	NC
GE2_RX_DV	NC
GE2_RX_ER	NC
GE2_SGMII_RX	GND_{SXC}
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	Nc
GE2_TD[0–3]	Nc
GE2_TX_EN	NC

3.4.4.2.2 Subset of GE2 Pins Required

When only a subset of the whole GE2 interface is used, such as for RMII, the unused GE2 pins should be connected as described in Table 60. The table assumes that the unused GE2 pins are not used for any purpose (including any multiplexed functions) and that V_{DDGE2} is tied to either 2.5 V or 3.3 V.

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required

Signal Name	Pin Connection
GE2_RD[0-3]	GND
GE2_RX_CLK	GND
GE2_RX_DV	GND
GE2_RX_ER	GND
GE2_SGMII_RX	GND_{SXC}

3.4.8 Miscellaneous Pins

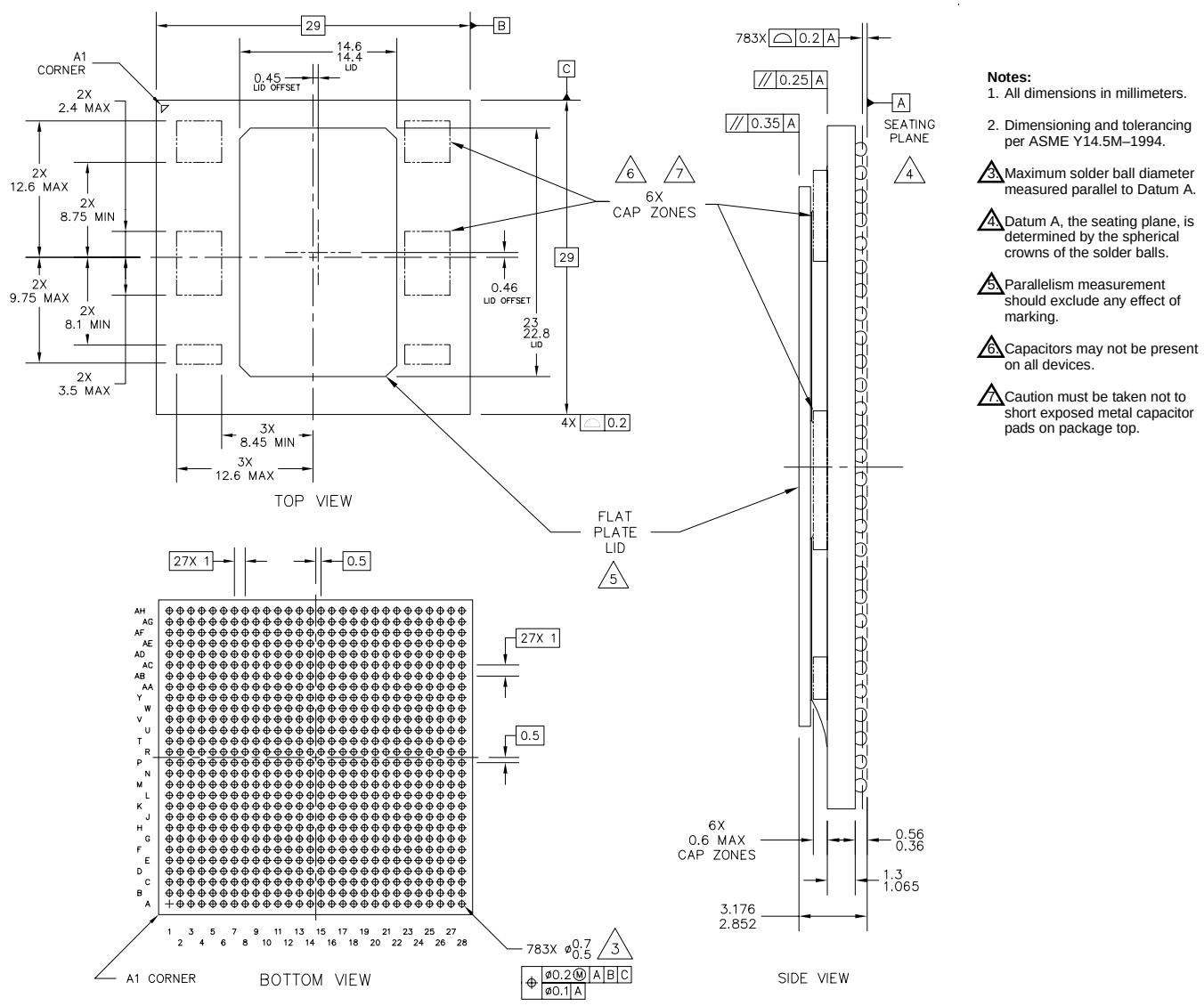
Table 65 lists the board connections for the pins if they are not required by the system design. Table 65 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 65. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[0–31]	GND
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ}}$[0–15]	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[0–16]	GND
$\overline{\text{RC\_LDF}}$	NC
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[0–4]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	GND
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
V_{DDIO}	3.3 V
Note: When using I/O multiplexing mode 5 or 6, tie the TDM7TSYN/PCI_AD4 signal (ball number AC9) to GND.	

Note: For details on configuration, see the *MSC8144 Reference Manual*. For additional information, refer to the *MSC8144 Design Checklist* (AN3202).

5 Package Information



Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement should exclude any effect of marking.
6. Capacitors may not be present on all devices.
7. Caution must be taken not to short exposed metal capacitor pads on package top.

CASE NO. 1842-04

Figure 44. MSC8144 Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

- *MSC8144 Technical Data Sheet* (MSC8144). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8144 device.
- *MSC8144 Reference Manual* (MSC8144RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes.* Cover various programming topics related to the StarCore DSP core and the MSC8144 device.
- *SC3400 DSP Core Reference Manual*. Covers the SC3400 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8144 SC3400 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.