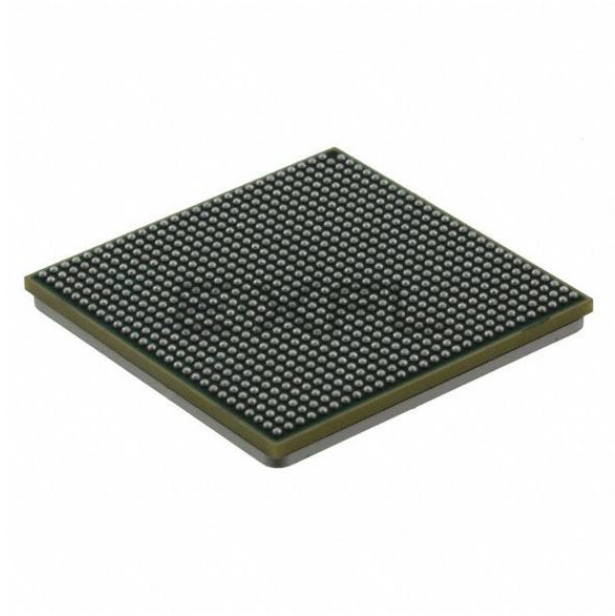

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	EBI/EMI, Ethernet, I²C, PCI, Serial RapidIO, SPI, TDM, UART, UTOPIA
Clock Rate	800MHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8144vt800a

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A4	V_{DDGE2}										V_{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A6	GE2_TD0/$\overline{\text{PCI\_CBE0}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A7	SRIO_IMP_CAL_RX										V_{DDSXC}
A8	Reserved[1]										—
A9	Reserved[1]										—
A10	Reserved[1]										—
A11	Reserved[1]										—
A12	SRIO_RXD0										V_{DDSXC}
A13	V_{DDSXC}										V_{DDSXC}
A14	SRIO_RXD1										V_{DDSXC}
A15	V_{DDSXC}										V_{DDSXC}
A16	$\overline{\text{SRIO\_REF\_CLK}}$										V_{DDSXC}
A17	$V_{DDRIOPLL}$										GND_{RIOPLL}
A18	GND_{SXC}										GND_{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A20	V_{DDSXC}										V_{DDSXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A22	V_{DDSXC}										V_{DDSXC}
A23	SRIO_IMP_CAL_TX										V_{DDSXP}
A24	MDQ28										V_{DDDDR}
A25	MDQ29										V_{DDDDR}
A26	MDQ30										V_{DDDDR}
A27	MDQ31										V_{DDDDR}
A28	$\overline{\text{MDQS3}}$										V_{DDDDR}
B1	Reserved[1]										—
B2	GE2_TD1/$\overline{\text{PCI\_CBE1}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B3	GE2_TX_EN/$\overline{\text{PCI\_CBE2}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B4	GE_MDIO		Ethernet								V_{DDGE2}
B5	GND										GND
B6	GE_MDC		Ethernet								V_{DDGE2}
B7	GND_{SXC}										GND_{SXC}
B8	Reserved[1]										—
B9	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E6	V_{DDGE1}										V_{DDGE1}
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E8	Reserved[1]										—
E9	Reserved[1]										—
E10	GND										GND
E11	V_{DD}										V_{DD}
E12	GND										GND
E13	V_{DD}										V_{DD}
E14	GND										GND
E15	V_{DD}										V_{DD}
E16	GND										GND
E17	V_{DD}										V_{DD}
E18	GND										GND
E19	V_{DD}										V_{DD}
E20	GND										GND
E21	V_{DD}										V_{DD}
E22	GND										GND
E23	V_{DDDDR}										V_{DDDDR}
E24	MDQ20										V_{DDDDR}
E25	GND										GND
E26	V_{DDDDR}										V_{DDDDR}
E27	GND										GND
E28	MDQS2										V_{DDDDR}
F1	Reserved[1]										—
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F3	V_{DDGE1}										V_{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F6	GND										GND
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F8	V_{DDGE1}										V_{DDGE1}
F9	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
G23	MBA1										V_{DDDDR}
G24	MA3										V_{DDDDR}
G25	MA8										V_{DDDDR}
G26	V_{DDDDR}										V_{DDDDR}
G27	GND										GND
G28	$\overline{\text{MCK0}}$										V_{DDDDR}
H1	Reserved[1]										—
H2	CLKIN										V_{DDIO}
H3	$\overline{\text{HRESET}}$										V_{DDIO}
H4	PCI_CLK_IN										V_{DDIO}
H5	$\overline{\text{NMI}}$										V_{DDIO}
H6	URXD/GPIO14/$\overline{\text{IRQ8}}$/ $\overline{\text{RC\_LDF}}$[3, 6]	$\overline{\text{RC\_LDF}}$	UART/GPIO/IRQ								V_{DDIO}
H7	GE1_RX_ER/PCI_AD6/ GPIO25/$\overline{\text{IRQ15}}$[3, 6]		GPIO/ IRQ	Ethernet 1	PCI			GPIO/ IRQ	Ethernet 1		V_{DDIO}
H8	GE1_CRS/PCI_AD5		PCI	Ethernet 1	PCI				Ethernet 1		V_{DDIO}
H9	GND										GND
H10	V_{DD}										V_{DD}
H11	GND										GND
H12	V_{DD}										V_{DD}
H13	GND										GND
H14	V_{DD}										V_{DD}
H15	V_{DD}										V_{DD}
H16	V_{DD}										V_{DD}
H17	GND										GND
H18	V_{DD}										V_{DD}
H19	GND										GND
H20	V_{DD}										V_{DD}
H21	V_{DD}										V_{DD}
H22	V_{DDDDR}										V_{DDDDR}
H23	MBA0										V_{DDDDR}
H24	MA15										V_{DDDDR}
H25	V_{DDDDR}										V_{DDDDR}
H26	MA9										V_{DDDDR}
H27	MA7										V_{DDDDR}
H28	MCK0										V_{DDDDR}
J1	Reserved[1]										—
J2	GND										GND
J3	V_{DDIO}										V_{DDIO}
J4	STOP_BS										V_{DDIO}
J5	$\overline{\text{NMI\_OUT}}$[4]										V_{DDIO}
J6	$\overline{\text{INT\_OUT}}$[4]										V_{DDIO}
J7	SDA/GPIO27[3, 4, 6]		I2C/GPIO								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
V8	V_{DDIO}										V_{DDIO}
V9	Reserved[1]										V_{DDIO}
V10	GND										GND
V11	V_{DDM3}										V_{DDM3}
V12	GND										GND
V13	V_{DDM3}										V_{DDM3}
V14	GND										GND
V15	V_{DDM3}										V_{DDM3}
V16	GND										GND
V17	V_{DDM3}										V_{DDM3}
V18	GND										GND
V19	V_{DDM3}										V_{DDM3}
V20	GND										GND
V21	GND										GND
V22	V_{DDDDR}										V_{DDDDR}
V23	MDQ2										V_{DDDDR}
V24	V_{DDDDR}										V_{DDDDR}
V25	MDQ6										V_{DDDDR}
V26	GND										GND
V27	V_{DDDDR}										V_{DDDDR}
V28	MDQS0										V_{DDDDR}
W1	Reserved[1]										—
W2	UTP_TD12/$\overline{\text{PCI\_CBE2}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W3	UTP_TD11/$\overline{\text{PCI\_CBE1}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W4	V_{DDIO}										V_{DDIO}
W5	GND										GND
W6	UTP_TD15/$\overline{\text{PCI\_IRDY}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W7	UTP_TD0/$\overline{\text{PCI\_SERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
W8	UTP_RSOC/PCI_AD22		UTOPIA		PCI	UTOPIA					V_{DDIO}
W9	Reserved[1]										V_{DDIO}
W10	V_{DDM3}										V_{DDM3}
W11	GND										GND
W12	V_{25M3}										V_{25M3}
W13	GND										GND
W14	V_{DDM3}										V_{DDM3}
W15	V_{25M3}										V_{25M3}
W16	V_{DDM3}										V_{DDM3}
W17	GND										GND
W18	V_{25M3}										V_{25M3}
W19	GND										GND
W20	V_{DDM3}										V_{DDM3}
W21	GND										GND
W22	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AA7	TDM4TCLK/PCI_AD10		TDM			PCI		TDM			V_{DDIO}
AA8	TDM4TDAT/PCI_AD11		TDM			PCI		TDM			V_{DDIO}
AA9	V_{DDIO}										V_{DDIO}
AA10	V_{DDM3}										V_{DDM3}
AA11	GND										GND
AA12	V_{DDM3}										V_{DDM3}
AA13	GND										GND
AA14	V_{DDM3}										V_{DDM3}
AA15	GND										GND
AA16	V_{DDM3}										V_{DDM3}
AA17	GND										GND
AA18	V_{DDM3}										V_{DDM3}
AA19	GND										GND
AA20	V_{DDM3}										V_{DDM3}
AA21	GND										GND
AA22	GND										GND
AA23	MDQ15										V_{DDDDR}
AA24	MDQ14										V_{DDDDR}
AA25	MDM1										V_{DDDDR}
AA26	MDQ12										V_{DDDDR}
AA27	$\overline{\text{MDQS1}}$										V_{DDDDR}
AA28	MDQS1										V_{DDDDR}
AB1	Reserved[1]										-
AB2	UTP_TSOC/RC15	RC15	UTOPIA								V_{DDIO}
AB3	V_{DDIO}										V_{DDIO}
AB4	TDM6RDAT/PCI_AD20/ GPIO5/$\overline{\text{IRQ11}}$[3, 6]		TDM/GPIO/ IRQ			PCI		TDM/GPIO/ IRQ			V_{DDIO}
AB5	TDM5RDAT/PCI_AD14/ GPIO9[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AB6	TDM6TSYN/PCI_AD24/ GPIO8/ $\overline{\text{IRQ14}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB7	TDM6RCLK/PCI_AD19/ GPIO4/$\overline{\text{IRQ10}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB8	TDM4RSYN/PCI_AD9		TDM			PCI		TDM			V_{DDIO}
AB9	TDM4RDAT/PCI_AD8		TDM			PCI		TDM			V_{DDIO}
AB10	GND										GND
AB11	V_{DDM3}										V_{DDM3}
AB12	GND										GND
AB13	V_{DDM3}										V_{DDM3}
AB14	GND										GND
AB15	V_{DDM3}										V_{DDM3}
AB16	GND										GND
AB17	V_{DDM3}										V_{DDM3}
AB18	GND										GND

2.3 Default Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths.

Table 4. Output Drive Impedance

Driver Type	Output Impedance (Ω)
DDR signal	18
DDR2 signal	18 35 (half strength mode)

2.4 Thermal Characteristics

Table 5 describes thermal characteristics of the MSC8144 for the FC-PBGA packages.

Table 5. Thermal Characteristics for the MSC8144

Characteristic	Symbol	FC-PBGA 29 × 29 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	20	15	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	15	12	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	7		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.8		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature.

2.5.2 Serial RapidIO DC Electrical Characteristics

DC receiver logic levels are not defined since the receiver is AC-coupled.

2.5.2.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$ are AC-coupled differential inputs. Each differential clock input has an internal 50 Ω termination to GND_{SXC}. The reference clock must be able to drive this termination. The recommended minimum operating voltage is –0.4 V; the recommended maximum operating voltage is 1.32 V; and the maximum absolute voltage is 1.72 V.

The maximum average current allowed in each input is 8 mA. This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 Ω = 8 mA) while the minimum common mode input level is GND_{SXC}. For example, a clock with a 50/50 duty cycle can be driven by a current source output that ranges from 0 mA to 16 mA (0–0.8 V). The input is AC-coupled internally, so, therefore, the exact common mode input voltage is not critical.

Note: This internal AC-couple network does not function correctly with reference clock frequencies below 90 MHz.

If the device driving the $\overline{\text{SRIO\_REF\_CLK}}$ inputs cannot drive 50 Ω to GND_{SXC}, or if it exceeds the maximum input current limitations, then it must use external AC-coupling. The minimum differential peak-to-peak amplitude of the input clock is 0.4 V (0.2 V peak-to-peak per phase). The maximum differential peak-to-peak amplitude of the input clock is 1.6 V peak-to-peak (see Figure 5. The termination to GND_{SXC} allows compatibility with HCSL type reference clocks specified for PCI-Express applications. Many other low voltage differential type outputs can be used but will probably need to be AC-coupled due to the limited common mode input range. LVPECL outputs can produce too large an amplitude and may need to be source terminated with a divider network to reduce the amplitude. The amplitude of the clock must be at least a 400 mV differential peak-peak for single-ended clock. If driven differentially, each signal wire needs to drive 100 mV around common mode voltage. The differential reference clock (SRIO_REF_CLK/ $\overline{\text{SRIO\_REF\_CLK}}$) input is HCSL-compatible DC coupled or LVDS-compatible with AC-coupling.

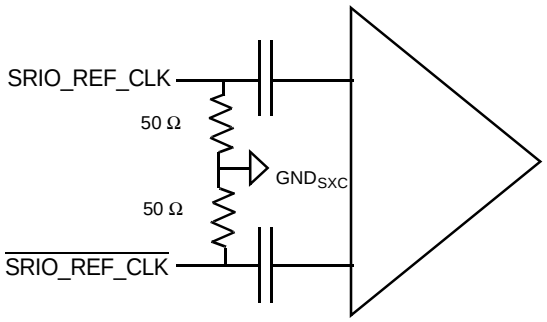

Figure 5. SerDes Reference Clocks Input Stage

2.6 AC Timings

The following sections include illustrations and tables of clock diagrams, signals, and parallel I/O outputs and inputs.

2.6.1 Start-Up Timing

Starting the device requires coordination among several input sequences including clocking, reset, and power. **Section 2.6.2** describes the clocking characteristics. **Section 2.6.3** describes the reset and power-up characteristics. You must use the following guidelines when starting up an MSC8144 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the power-up sequence using the V_{DDIO} (3.3 V) supply. See Table 19 for timing. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. During functional operation when JTAG is not used, $\overline{\text{TRST}}$ can be asserted and remain asserted after the power ramp.

Note: For applications that use M3 memory, $\overline{\text{M3\_RESET}}$ should replicate the $\overline{\text{PORESET}}$ sequence timing, but using the V_{DDM3IO} (2.5 V) supply. See **Section 3.1.1**, *Power-on Sequence* for additional design information.

- CLKIN should start toggling at least 32 cycles before the $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation (see Figure 6). 32 cycles should be accounted only after V_{DDIO} reaches its nominal value.
- CLKIN and PCI_CLK_IN should either be stable low during the power-up of V_{DDIO} supply and start their swings after power-up or should swing within V_{DDIO} range during V_{DDIO} power-up., so their amplitude grows as V_{DDIO} grows during power-up.

Figure 6 shows a sequence in which V_{DDIO} is raised after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

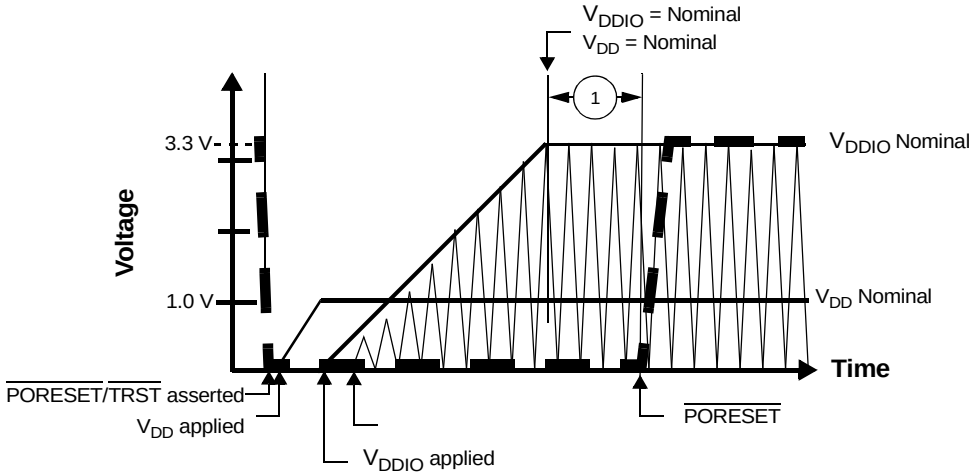

Figure 6. Start-Up Sequence with V_{DD} Raised Before V_{DDIO} with CLKIN Started with V_{DDIO}

2.6.2 Clock and Timing Signals

The following sections include a description of clock signal characteristics. Table 16 shows the maximum frequency values for CLKIN and PCI_CLK_IN. The user must ensure that maximum frequency values are not exceeded.

Table 16. Clock Frequencies

Characteristic	Symbol	Min	Max	Unit
CLKIN frequency	F_{CLKIN}	33	133	MHz
PCI_CLK_IN frequency	$F_{PCI\_CLK\_IN}$	33	133	MHz
CLKIN duty cycle	D_{CLKIN}	40	60	%
PCI_CLK_IN duty cycle	$D_{PCI\_CLK\_IN}$	40	60	%

2.6.3 Reset Timing

The MSC8144 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- JTAG reset
- RapidIO reset
- Software hard reset
- Software soft reset

All MSC8144 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. Table 17 describes the reset sources.

Table 17. Reset Sources

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	Initiates the power-on reset flow that resets the MSC8144 and configures various attributes of the MSC8144. On $\overline{\text{PORESET}}$, the entire MSC8144 device is reset. All PLLs states is reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the extended cores are reset, and system configuration is sampled. The reset source and word are configured only when $\overline{\text{PORESET}}$ is asserted.
External hard reset ($\overline{\text{HRESET}}$)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8144. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the extended cores are reset, and system configuration is sampled. Note that the RCW (reset Configuration Word) is not reloaded during $\overline{\text{HRESET}}$ assertion after out of power on reset sequence. The reset configuration word is described in the Reset chapter in the *MSC8144 Reference Manual*.
External soft reset ($\overline{\text{SRESET}}$)	Input/ Output	Initiates the soft reset flow. The MSC8144 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8144 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the extended cores are reset, and system configuration is maintained.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.
Software watchdog reset	Internal	When the MSC8144 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
RapidIO reset	Internal	When the RapidIO logic asserts the RapidIO hard reset signal, it generates an internal hard reset sequence.
Software hard reset	Internal	A hard reset sequence can be initialized by writing to a memory mapped register (RCR)
Software soft reset	Internal	A soft reset sequence can be initialized by writing to a memory mapped register (RCR)

Table 18 summarizes the reset actions that occur as a result of the different reset sources.

Table 18. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset ($\overline{\text{PORESET}}$)	Hard Reset ($\overline{\text{HRESET}}$)	Soft Reset ($\overline{\text{SRESET}}$)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (Refer to **Section 2.6.3.2** for details).	Yes	No	No	No
PLL state reset	Yes	No	No	No
Select reset configuration source	Yes	No	No	No
System reset configuration write	Yes	No	No	No

Table 19. Timing for a Reset Configuration Write (continued)

No.	Characteristics	Expression	Max	Min	Unit
2	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for external pins and hard coded RCW				
	• 33 MHz <= CLKIN < 66 MHz	15369/CLKIN	615	233	µs
	• 66 MHz <= CLKIN <= 133 MHz	34825/CLKIN	528	262	µs
	Delay from de-assertion of external $\overline{\text{PORESET}}$ to $\overline{\text{HRESET}}$ deassertion for loading RCW the I^2C interface				
	• 33 MHz <= CLKIN < 44 MHz	92545/CLKIN	3702	2103	µs
	• 44 MHz <= CLKIN < 66 MHz	107435/CLKIN	2441	1627	µs
	• 66 MHz <= CLKIN < 100 MHz	124208/CLKIN	1882	1242	µs
	• 100 MHz <= CLKIN < 133 MHz	157880/CLKIN	1579	1187	µs
3	Delay from $\overline{\text{HRESET}}$ deassertion to $\overline{\text{SRESET}}$ deassertion				
	• REFCLK = 33 MHz to 133 MHz	16/CLKIN	640	120	ns
Note:	Timings are not tested, but are guaranteed by design.				

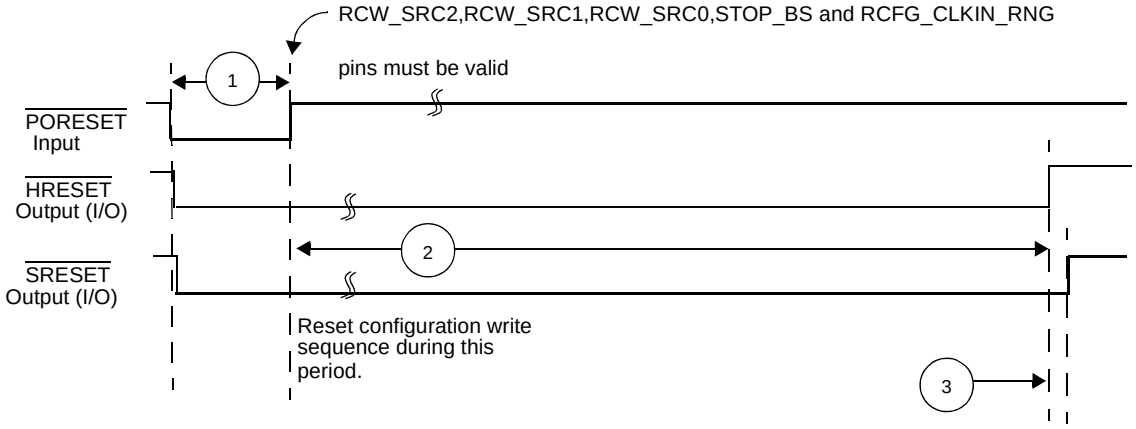

Figure 7. Timing for a Reset Configuration Write

See also Reset Errata for PLL lock and reset duration.

2.6.4.2 DDR SDRAM Output AC Timing Specifications

Table 23 provides the output AC timing specifications for the DDR SDRAM interface.

Table 23. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)[2]	t_{MCK}	5	10	ns
ADDR/CMD output setup with respect to MCK[3]	t_{DDKHAS}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
ADDR/CMD output hold with respect to MCK[3]	t_{DDKHAX}			
• 400 MHz		1.85	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
$\overline{\text{MCS}}$n output setup with respect to MCK[3]	t_{DDKHCS}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
$\overline{\text{MCS}}$n output hold with respect to MCK[3]	t_{DDKHCX}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
MCK to MDQS Skew[4]	t_{DDKHMH}	–0.6	0.6	ns
MDQ/MECC/MDM output setup with respect to MDQS[5]	t_{DDKHDS}, t_{DDKLDS}			
• 400 MHz		700	—	ps
• 333 MHz		900	—	ps
• 266 MHz		1100	—	ps
• 200 MHz		1200	—	ps
MDQ/MECC/MDM output hold with respect to MDQS[5]	t_{DDKHDX}, t_{DDKLDX}			
• 400 MHz		700	—	ps
• 333 MHz		900	—	ps
• 266 MHz		1100	—	ps
• 200 MHz		1200	—	ps
MDQS preamble start[6]	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns
MDQS epilogue end[6]	t_{DDKHME}	–0.6	0.6	ns

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MSC8144 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) ± 5%.

Figure 10 provides the AC test load for the DDR bus.

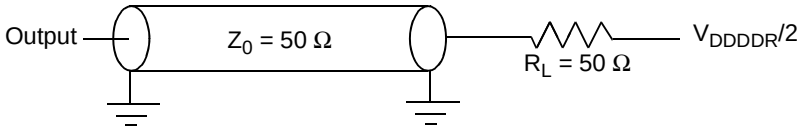

Figure 10. DDR AC Test Load

2.6.5 Serial RapidIO Timing and SGMII Timing

2.6.5.1 AC Requirements for SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$

Table 24 lists AC signal specifications.

Table 24. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Signal Specifications

Parameter Description	Symbol	Min	Typical	Max	Units	Comments
REFCLK cycle time	t_{REF}	—	10 (8, 6.4)	—	ns	8 ns applies only to serial RapidIO system with 125-MHz reference clock. 6.4 ns applies only to serial RapidIO systems with a 156.25 MHz reference clock. **Note:** SGMII uses the 8 ns (125 MHz) value only.

2.6.5.2 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 11 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between voltage levels A and B, where A > B.

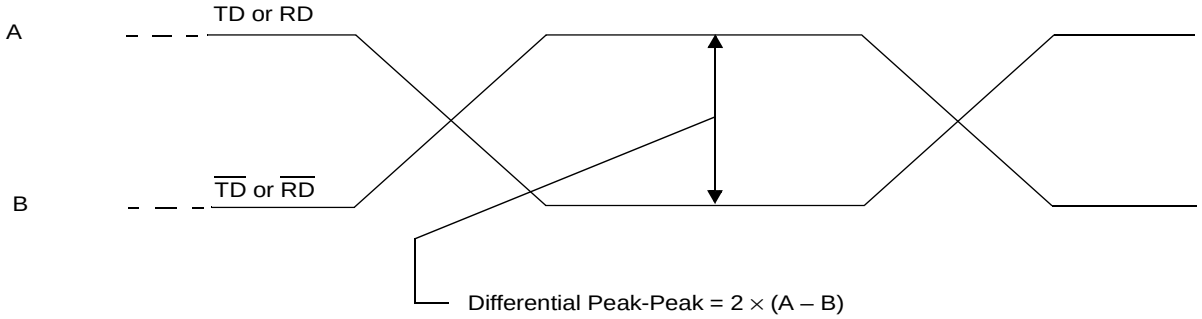

Figure 11. Differential V_{PP} of Transmitter or Receiver

Note: This explanation uses generic TD/$\overline{\text{TD}}$/RD/$\overline{\text{RD}}$ signal names. These correspond to SRIO_TXD/$\overline{\text{SRIO\_TXD}}$/ SRIO_RXD/$\overline{\text{SRIO\_RXD}}$ respectively.

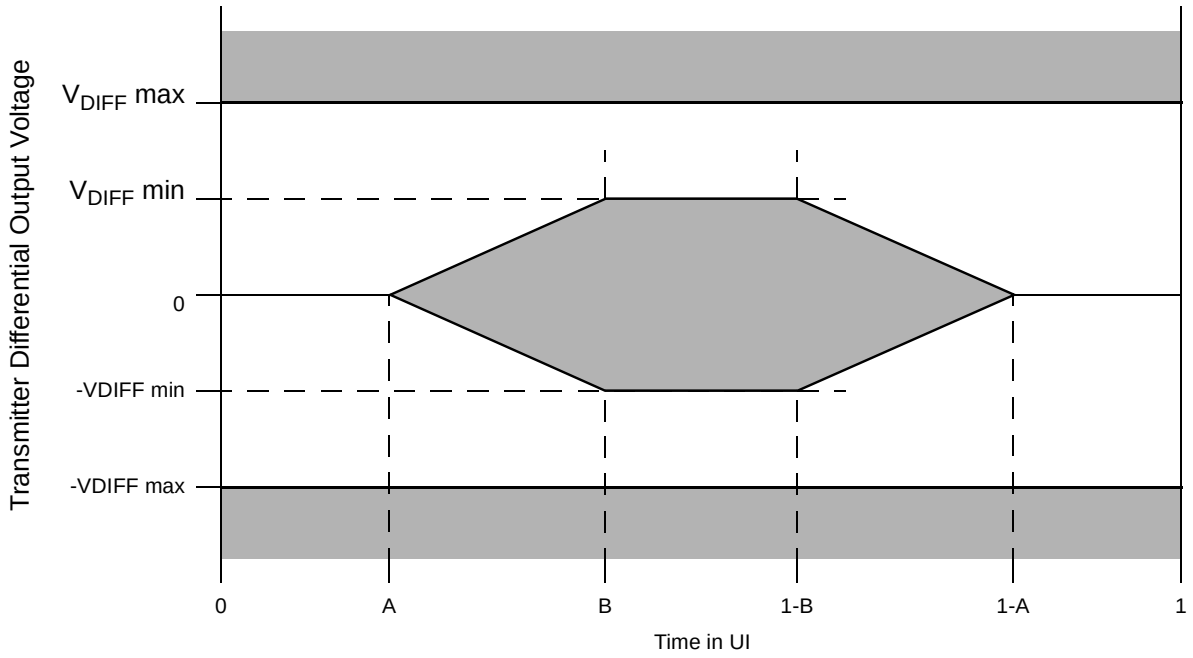

Figure 12. Transmitter Output Compliance Mask

Table 31. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

2.6.5.6 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 32, Table 33, and Table 34) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 14 with the parameters specified in Table 35. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω ±5% differential resistive load.

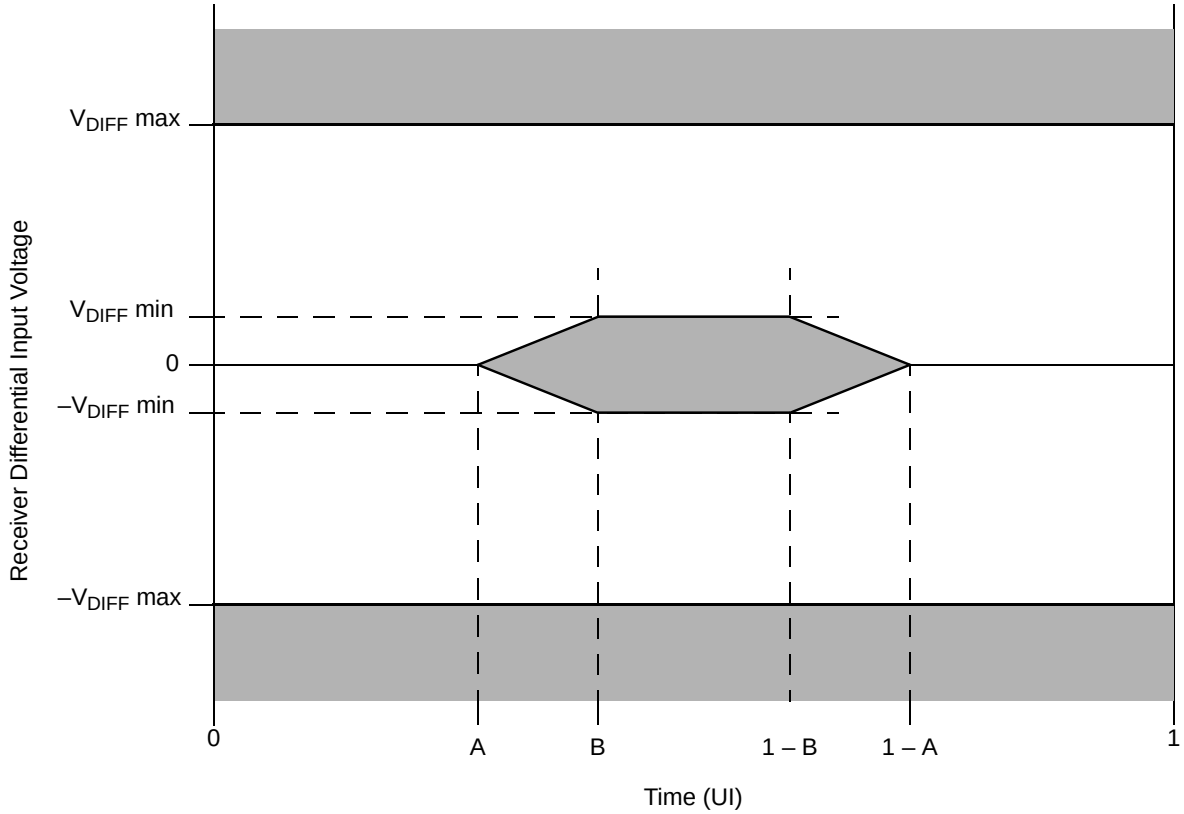

Figure 14. Receiver Input Compliance Mask

Table 35. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

2.6.5.7 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of **IEEE** Std. 802.3ae-2002™, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of **IEEE** Std. 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of **IEEE** Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

2.6.5.8 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.9 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of **IEEE** Std. 802.3ae.

2.6.5.10 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.11 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in **Section 2.6.5.9** and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 14 and Table 35. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

2.6.6 PCI Timing

This section describes the general AC timing parameters of the PCI bus. Table 36 provides the PCI AC timing specifications.

Table 36. PCI AC Timing Specifications

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
Output delay	t_{PCVAL}	2.0	11.0	1.0	6.0	ns
High-Z to Valid Output delay	t_{PCON}	2.0	—	1.0	—	ns
Valid to High-Z Output delay	t_{PCOFF}	—	28	—	14	ns
Input setup	t_{PCSU}	7.0	—	3.0	—	ns
Input hold	t_{PCH}	0	—	0	—	ns

Table 36. PCI AC Timing Specifications (continued)

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	

Notes:
1. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
2. All PCI signals are measured from $0.5 \times V_{DDIO}$ of the rising edge of PCI_CLK_IN to $0.4 \times V_{DDIO}$ of the signal in question for 3.3-V PCI signaling levels.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is in Table 19 and Figure 7

Figure 15 provides the AC test load for the PCI.

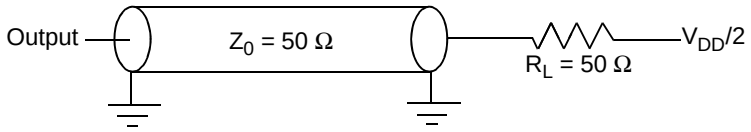

Figure 15. PCI AC Test Load

Figure 16 shows the PCI input AC timing conditions.

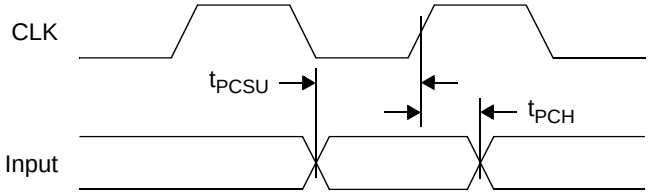

Figure 16. PCI Input AC Timing Measurement Conditions

Figure 17 shows the PCI output AC timing conditions.

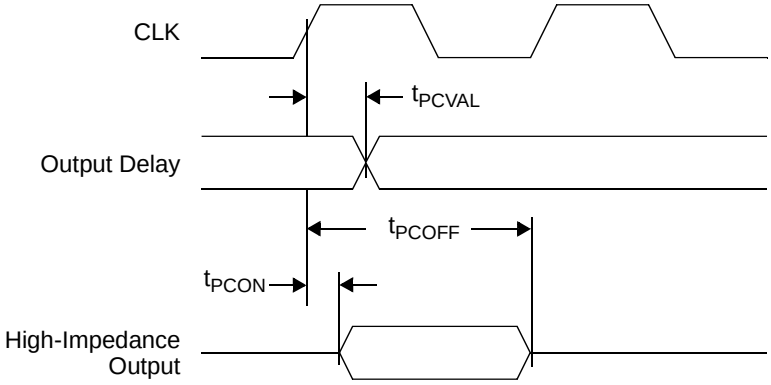

Figure 17. PCI Output AC Timing Measurement Condition

2.6.9 Timer Timing

Table 39. Timer Timing

Characteristics	Symbol	Min	Unit
TIMERx frequency	$T_{TMREFCLK}$	10.0	ns
TIMERx Input high phase	T_{TMCH}	4.0	ns
TIMERx Output low phase	T_{TMCL}	4.0	ns

Figure 23 shows the timer input AC timing

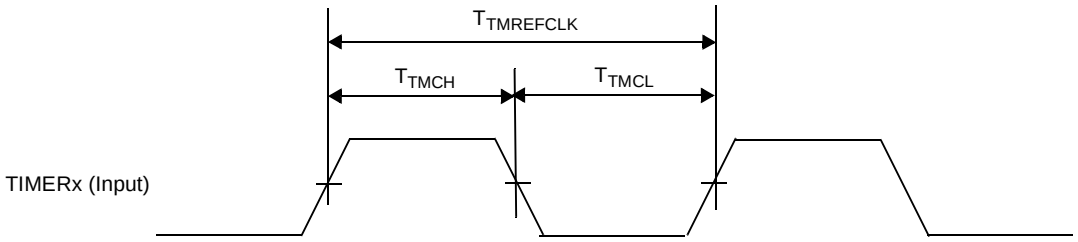

Figure 23. Timer Timing

2.6.10 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each Interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the *MSC8144 Reference Manual*.

2.6.10.1 Management Interface Timing

Table 40. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
ETHMDC to ETHMDIO delay[2]	t_{MDKHDX}	10	70	ns
ETHMDIO to ETHMDC rising edge setup time	t_{MDDVKH}	7	—	ns
ETHMDC rising edge to ETHMDIO hold time	t_{MDDXKH}	0	—	ns

Notes:
1. Program the ETHMDC frequency (f_{MDC}) to a maximum value of 2.5 MHz (400 ns period for t_{MDC}). The value depends on the source clock and configuration of MIIMCFG[MCS] and UPSMR[MDCP]. For example, for a source clock of 400 MHz, to achieve f_{MDC} = 2.5 MHz, program MIIMCFG[MCS] = 0x4 and UPSMR[MDCP] = 0. See the *MSC8144 Reference Manual* for configuration details.
2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns.

The following supplies should rise before any other supplies in any sequence

- V_{DD} and V_{DDPLL} coupled together
- V_{DDM3}

After the above supplies rise to 90% of their nominal value the following I/O supplies may rise in any sequence (see Figure 42):

- V_{DDGE1}
- V_{DDGE2}
- V_{DDIO}
- V_{DDDDR} and MV_{REF} coupled one to another. MV_{REF} should be either at same time or after V_{DDDDR}.
- V_{DDM3IO}
- V_{25M3}

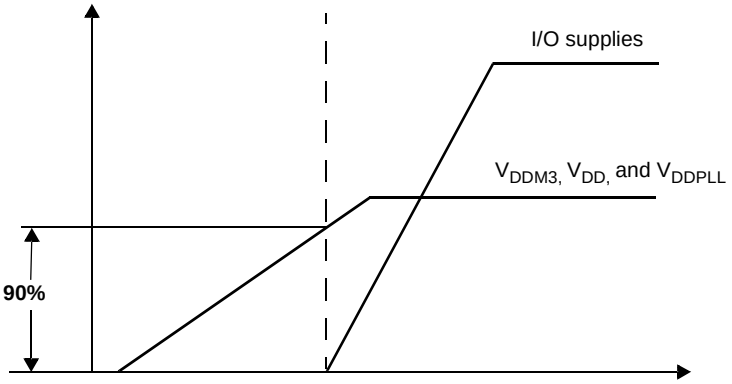

Figure 42. V_{DDM3}, V_{DDM3IO} and V_{25M3} Power-on Sequence

Note:
1. This recommended power sequencing is different from the MSC8122/MSC8126.
2. If no pins that require V_{DDGE1} as a reference supply are used (see Table 1), V_{DDGE1} can be tied to GND.
3. If no pins that require V_{DDGE2} as a reference supply are used (see Table 1), V_{DDGE2} can be tied to GND.
4. If the DDR interface is not used, V_{DDDDR} and MV_{REF} can be tied to GND.
5. If the M3 memory is not used, V_{DDM3}, V_{DDM3IO}, and V_{25M3} can be tied to GND.
6. If the RapidIO interface is not used, V_{DDSX}, V_{DDSXP}, and $V_{DDRIOPLL}$ can be tied to GND.

3.1.2 Start-Up Timing

Section 2.6.1 describes the start-up timing.

3.4.4 Ethernet Related Pins

3.4.4.1 Ethernet Controller 1 (GE1) Related Pins

Note: Table 57 and Table 58 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.4.4.1.1 GE1 Interface Is Not Used

Table 57 assumes that the GE1 signals are not used for any purpose (including any multiplexed functions) and that V_{DDGE1} is tied to GND.

Table 57. Connectivity of GE1 Related Pins When the GE1 Interface Is Not Used

Signal Name	Pin Connection
GE1_COL	NC
GE1_CRS	NC
GE1_RD[0–4]	NC
GE1_RX_ER	NC
GE1_RX_CLK	NC
GE1_RX_DV	NC
GE1_SGMII_RX	GND_{SXC}
$\overline{\text{GE1\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE1\_SGMII\_TX}}$	NC
GE1_SGMII_TX	NC
GE1_TD[0–4]	NC
GE1_TX_CLK	NC
GE1_TX_EN	NC
GE1_TX_ER	NC

3.4.4.1.2 Subset of GE1 Pins Required

When only a subset of the whole GE1 interface is used, such as for RMII, the unused GE1 pins should be connected as described in Table 58. This table assumes that the unused GE1 pins are not used for any purpose (including any multiplexed function) and that V_{DDGE1} is tied to either 2.5 V or 3.3 V.

Table 58. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required

Signal Name	Pin Connection
GE1_COL	GND
GE1_CRS	GND
GE1_RD[0–3]	GND
GE1_RX_ER	GND
GE1_RX_CLK	GND
GE1_RX_DV	GND
GE1_SGMII_RX	GND_{SXC}
$\overline{\text{GE1\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE1\_SGMII\_TX}}$	NC

Table 66. Document Revision History (continued)

Rev.	Date	Description
7	Dec 2007	• Changed minimum voltage level for V_{DDM3} to 1.213 (1.25 – 3%) in Table 3. • Added POS to titles in **Section 2.6.6**. • Added additional signals to titles in **Section 2.6.8**. Added high and low voltage ranges to Table 19. • Added ATM and POS to headings in **Section 2.7.11**. Changed characteristics to generic input/output in Table 52, Figure 33, and Figure 34. • Replaced **Sections 2.7.13** and **2.7.14** with new **Section 2.7.13**, *Asynchronous Signal Timing*. Renumbered subsequent sections, tables, and figures. • Added POS to all UTOPIA references in **Section 3.4.5**.
8	Dec 2007	• Changed GCR4 program value to 0x0004C130 in Note 7 in Table 51.
9	Mar 2008	• Changed description of Table 20 in **Section 2.7.2**.
10	Apr 2008	• Added [3] to the PLL supply voltage row in **Table 2**. • Changed the first sentence in **Section 3.4.8** to reflect that **Table 70** indicates what to do with pins if they are "not" required by the design. Changed the Pin Connection for GPIO[0–31] to GND. • Updated ordering information in **Section 4**. • Multiple corrections of minor punctuation errors.
11	Aug 2008	• Removed the comment about preliminary estimates before Table 4 and removed non-DDR rows in the table. • Table 9 and Table 11 for DDR and DDR2 SDRAM capacitance removed and subsequent tables renumbered. • Changed units for I_{OH} and I_{OL} to mA in Table 9. • Removed signal low and high input current from Table 12. • Added a note to Table 15 to exclude TDM and TMS. Removed reference to overshoot and undershoot and associated figure. • Changed minimum clock frequency to 33 MHz and maximum clock frequency to 133 MHz in Table 16. • Deleted old Table 17 Clock Parameters. • Changed minimum input clock frequency to 33 MHz in Table 19. • Changed the t_{DDKHAX} minimum value in Table 23 to 1.85 ns. • Removed t_{REFPJ} and t_{REFCJ} from Table 24 because the specifications are not required or tested. • Removed $t_{PCRSTCLK}$, $t_{PCRSTOFF}$, t_{PCRST}, and t_{PCRHFA} from Table 36 because the specifications are not required or tested. • Removed t_{UAVKH} and t_{UAVXH} from Table 38 because the specifications are not required or tested. • The parameters t_{MDCH}, t_{MDCR}, and t_{MDHF} were removed from Table 40 because the specifications are not required or tested. • The parameters t_{MTXH}/t_{MTX}, t_{MTXR}, and t_{MTXF} were removed from Table 41 because the specifications are not required or tested. • The parameters t_{MRXH}/t_{MRX}, t_{MRXR}, and t_{MRXF} were removed from Table 42 because the specifications are not required or tested. • The parameters t_{RMXH}/t_{RMX}, t_{RMXR}, and t_{RMXF} were removed from Table 43 because the specifications are not required or tested. • Removed the parameters t_{RGT}, t_{RGTH}/t_{RGT} (1000Base-T), t_{RGTH}/t_{RGT} (10Base-T), t_{RGTR}, t_{RGTF}, t_{G12}, and t_{G125H}/t_{G125} were removed from Table 45 and Table 46 because the specifications are not required or tested. • Changed t_{UEKHOX} to guaranteed by design in Table 47. • Updated Figure 35 and Figure 36 SPI timing diagrams. • Removed TCK rise and fall time from Table 50. • Updated orderable part numbers in **Section 4**.
12	Aug 2008	• Changed b8t to bit in the M3 memory description on the first page. • Changed maximum input high voltage (VIH) for SPI to 3.465 in the first row of Table 14. • Changed packet processor to QUICC Engine Subsystem in the last row of Table 18.
13	Feb 2009	• In Figure 31, for GTX_CLK, changed (at transmitter) to (at DSP) and for RX_CLK, changed (at PHY) to (at DSP). • Updated package drawing to the latest revision, Case No. 1842-04 in Figure 44.
14	Jul 2009	• Updated MV_{REF} equations and temperature ranges in Table 3. • Updated orderable part numbers to **Section 4**.
15	Nov 2009	• Updated Core and PLL input voltage tolerance in Table 3.
16	May 2010	• Corrected typo in Table 23. Changed MCLK minimum time to 5 ns.