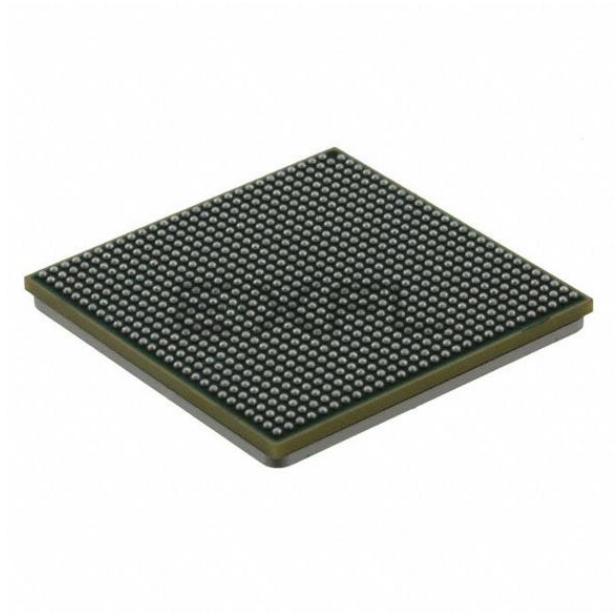


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	EBI/EMI, Ethernet, I²C, PCI, Serial RapidIO, SPI, TDM, UART, UTOPIA
Clock Rate	800MHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmc8144vt800b

1 Pin Assignments and Reset States

This section includes diagrams of the MSC8144 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in Figure 3 and Figure 4 with their ball location index numbers.

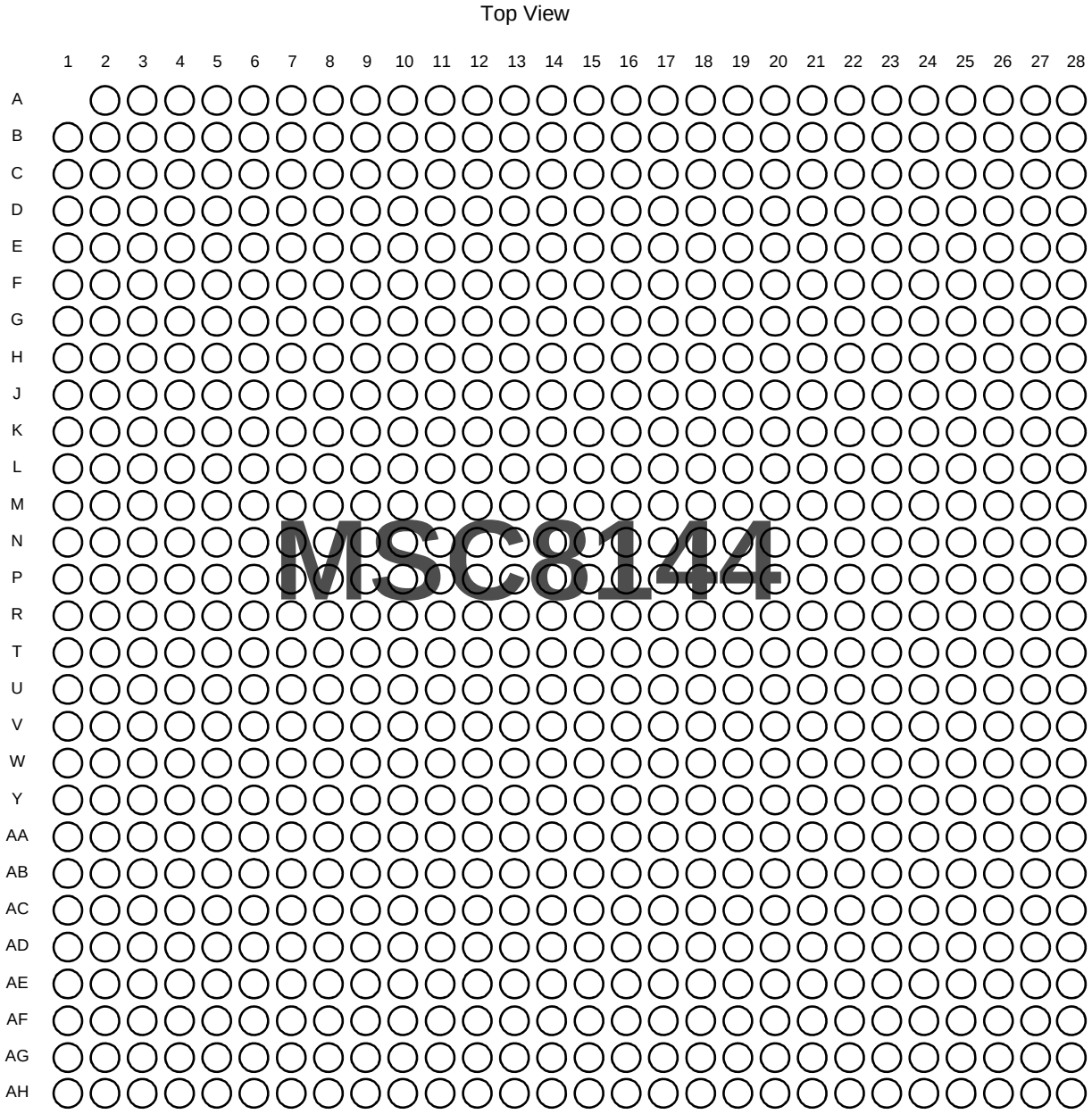


Figure 3. MSC8144 FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
B10	Reserved[1]										—
B11	Reserved[1]										—
B12	$\overline{\text{SRIO\_RXD0}}$										V_{DDSXC}
B13	GND_{SXC}										GND_{SXC}
B14	$\overline{\text{SRIO\_RXD1}}$										V_{DDSXC}
B15	GND_{SXC}										GND_{SXC}
B16	SRIO_REF_CLK										V_{DDSXC}
B17	Reserved[1]										—
B18	V_{DDSXC}										V_{DDSXC}
B19	$\overline{\text{SRIO\_RXD2}}$/ $\overline{\text{GE1\_SGMII\_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B20	GND_{SXC}										GND_{SXC}
B21	$\overline{\text{SRIO\_RXD3}}$/ $\overline{\text{GE2\_SGMII\_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B22	GND_{SXC}										GND_{SXC}
B23	GND_{SXP}										GND_{SXP}
B24	MDQ27										V_{DDDDR}
B25	V_{DDDDR}										V_{DDDDR}
B26	GND										GND
B27	V_{DDDDR}										V_{DDDDR}
B28	MDQS3										V_{DDDDR}
C1	Reserved[1]										—
C2	GE2_RX_CLK/PCI_AD29		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C3	V_{DDGE2}										V_{DDGE2}
C4	TDM7RSYN/GE2_TD2/ PCI_AD2/UTP_TER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C5	TDM7RCLK/GE2_RD2/ PCI_AD0/UTP_RVL		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C6	V_{DDGE2}										V_{DDGE2}
C7	GE2_RD0/PCI_AD27		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C8	Reserved[1]										—
C9	Reserved[1]										—
C10	Reserved[1]										—
C11	Reserved[1]										—
C12	V_{DDSXP}										V_{DDSXP}
C13	$\overline{\text{SRIO\_TXD0}}$										V_{DDSXP}
C14	V_{DDSXP}										V_{DDSXP}
C15	$\overline{\text{SRIO\_TXD1}}$										V_{DDSXP}
C16	GND_{SXC}										GND_{SXC}
C17	GND_{RIOPLL}										GND_{RIOPLL}
C18	Reserved[1]										—
C19	V_{DDSXP}										V_{DDSXP}
C20	$\overline{\text{SRIO\_TXD2}}$/$\overline{\text{GE1\_SGMII\_TX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
C21	V_{DDSXP}										V_{DDSXP}
C22	$\overline{SRIO\_TXD3/GE2\_SGMII\_TX}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
C23	V_{DDSXP}										V_{DDSXP}
C24	MDQ26										V_{DDDDR}
C25	MDQ25										V_{DDDDR}
C26	MDM3										V_{DDDDR}
C27	GND										GND
C28	MDQ24										V_{DDDDR}
D1	Reserved[1]										—
D2	GE2_RD1/PCI_AD28		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
D3	GND										GND
D4	TDM7TDAT/GE2_TD3/ PCI_AD3/UTP_TMD		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D5	TDM7RDAT/GE2_RD3/ PCI_AD1/UTP_STA		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D6	$\overline{GE1\_RD0}$/UTP_RD2/ $\overline{PCI\_CBE2}$		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
D7	TDM7TCLK/GE2_TCK/ PCI_IDS/UTP_RER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D8	Reserved[1]										—
D9	Reserved[1]										—
D10	Reserved[1]										—
D11	Reserved[1]										—
D12	GND_{SXP}										GND_{SXP}
D13	SRIO_TXD0										V_{DDSXP}
D14	GND_{SXP}										GND_{SXP}
D15	SRIO_TXD1										V_{DDSXP}
D16	V_{DDSXC}										V_{DDSXC}
D17	Reserved[1]										—
D18	Reserved[1]										—
D19	GND_{SXP}										GND_{SXP}
D20	SRIO_TXD2/GE1_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D21	GND_{SXP}										GND_{SXP}
D22	SRIO_TXD3/GE2_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D23	GND_{SXP}										GND_{SXP}
D24	MDQ23										V_{DDDDR}
D25	V_{DDDDR}										V_{DDDDR}
D26	MDQ22										V_{DDDDR}
D27	MDQ21										V_{DDDDR}
D28	$\overline{MDQS2}$										V_{DDDDR}
E1	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
R7	V_{DDIO}										V_{DDIO}
R8	$\overline{\text{PCI\_REQ}}$		PCI								V_{DDIO}
R9	GND										GND
R10	GND										GND
R11	GND										GND
R12	GND										GND
R13	GND										GND
R14	GND										GND
R15	GND										GND
R16	GND										GND
R17	GND										GND
R18	GND										GND
R19	GND										GND
R20	GND										GND
R21	GND										GND
R22	GND										GND
R23	MODT0										V_{DDDDR}
R24	MDIC1										V_{DDDDR}
R25	MDIC0										V_{DDDDR}
R26	$\overline{\text{MCAS}}$										V_{DDDDR}
R27	$\overline{\text{MWE}}$										V_{DDDDR}
R28	MCK2										V_{DDDDR}
T1	Reserved[1]										—
T2	UTP_RPRTY/PCI_AD21		UTOPIA		PCI	UTOPIA					V_{DDIO}
T3	UTP_RD13/PCI_AD17		UTOPIA		PCI	UTOPIA					V_{DDIO}
T4	V_{DDIO}										V_{DDIO}
T5	UTP_RD14/PCI_AD18		UTOPIA		PCI	UTOPIA					V_{DDIO}
T6	UTP_RD15/PCI_AD19		UTOPIA		PCI	UTOPIA					V_{DDIO}
T7	$\overline{\text{PCI\_TRDY}}$		PCI								V_{DDIO}
T8	$\overline{\text{PCI\_DEVSEL}}$/GPIO31/ $\overline{\text{IRQ3}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
T9	GND										GND
T10	GND										GND
T11	GND										GND
T12	GND										GND
T13	GND										GND
T14	GND										GND
T15	GND										GND
T16	GND										GND
T17	GND										GND
T18	GND										GND
T19	GND										GND
T20	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AE19	GND										GND
AE20	V_{DDM3IO}										V_{DDM3IO}
AE21	Reserved[1]										—
AE22	GND										GND
AE23	GND										GND
AE24	GND										GND
AE25	V_{DDDDR}										V_{DDDDR}
AE26	GND										GND
AE27	V_{DDDDR}										V_{DDDDR}
AE28	GND										GND
AF1	Reserved[1]										—
AF2	V_{DDIO}										V_{DDIO}
AF3	GND										GND
AF4	TDM0RDAT/ RCFG_CLKIN_RNG	RCFG_ CLKIN_ RNG	TDM								V_{DDIO}
AF5	TDM0TSYN/RCW_SRC2	RCW_ SRC2	TDM								V_{DDIO}
AF6	TDM1RDAT/RC0	RC0	TDM								V_{DDIO}
AF7	V_{DDIO}										V_{DDIO}
AF8	GND										GND
AF9	TDM2RDAT/RC4	RC4	TDM								V_{DDIO}
AF10	TDM2TCLK		TDM								V_{DDIO}
AF11	GPIO22/$\overline{IRQ4}$[3, 6]/SPIMOSI		GPIO/IRQ/SPI								V_{DDIO}
AF12	GND										GND
AF13	GND										GND
AF14	V_{DDM3IO}										V_{DDM3IO}
AF15	GND										GND
AF16	GND										GND
AF17	Reserved[1]										—
AF18	V_{DDM3IO}										V_{DDM3IO}
AF19	GND										GND
AF20	Reserved[1]										—
AF21	Reserved[1]										—
AF22	$\overline{M3\_RESET}$										V_{DDM3IO}
AF23	GND										GND
AF24	V_{DDDDR}										V_{DDDDR}
AF25	GND										GND
AF26	V_{DDDDR}										V_{DDDDR}
AF27	GND										GND
AF28	V_{DDDDR}										V_{DDDDR}
AG1	Reserved[1]										—
AG2	GPIO16/$\overline{IRQ0}$[3, 6]		GPIO/IRQ								V_{DDIO}
AG3	TDM0TCLK		TDM								V_{DDIO}

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
M3 memory I/O and M3 memory charge pump voltage	V_{DDM3IO} V_{25M3}	–0.3 to 2.75	V
Input M3 memory I/O voltage	V_{INM3IO}	–0.3 to V_{DDM3IO} + 0.3	V
Rapid I/O C voltage	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O P voltage	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	–0.3 to 1.21	V
Operating temperature	T_J	–40 to 105	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8144 (see Figure 43)

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage • 800 MHz (VT, SVT, TVT) and 1000 MHz (VT) • 1000 MHz (SVT, TVT)	V_{DD}	 0.97 0.97	 1.0 1.0	 1.05 1.03	 V V
PLL supply voltage • 800 MHz (VT, SVT, TVT) and 1000 MHz (VT) • 1000 MHz (SVT, TVT)	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	 0.97 0.97	 1.0 1.0	 1.05 1.03	 V V
M3 memory Internal voltage	V_{DDM3}	1.213	1.25	1.313	V
DDR memory supply voltage • DDR mode • DDR2 mode DDR reference voltage	V_{DDDDR} MV_{REF}	 2.375 1.71 0.49 × V_{DDDDR} (nom)	 2.5 1.8 0.5 × V_{DDDDR} (nom)	 2.625 1.89 0.51 × V_{DDDDR} (nom)	 V V V
Ethernet 1 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE1}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
Ethernet 2 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE2}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	3.135	3.3	3.465	V
M3 memory I/O and M3 charge pump voltage	V_{DDM3IO} V_{25M3}	2.375	2.5	2.625	V
Rapid I/O C voltage	V_{DDSXC}	0.97	1.0	1.05	V
Rapid I/O P voltage • Short run (haul) mode • Long run (haul) mode	V_{DDSXP}	 0.97 1.14	 1.0 1.2	 1.05 1.26	 V V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	0.97	1.0	1.05	V
Operating temperature range: • Standard (VT) • Intermediate (SVT) • Extended (TVT)	 T_J T_J T_A T_J	 0 0 –40 —		 90 105 — 105	 °C °C °C °C

Note: PLL supply voltage is specified at input of the filter and not at pin of the MSC8144 (see Figure 43).

2.3 Default Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths.

Table 4. Output Drive Impedance

Driver Type	Output Impedance (Ω)
DDR signal	18
DDR2 signal	18 35 (half strength mode)

2.4 Thermal Characteristics

Table 5 describes thermal characteristics of the MSC8144 for the FC-PBGA packages.

Table 5. Thermal Characteristics for the MSC8144

Characteristic	Symbol	FC-PBGA 29 × 29 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	20	15	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	15	12	°C/W
Junction-to-board (bottom)[4]	$R_{\theta JB}$	7		°C/W
Junction-to-case[5]	$R_{\theta JC}$	0.8		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature.

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8144.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8144.

Note: DDR SDRAM uses V_{DDDDR}(typ) = 2.5 V and DDR2 SDRAM uses V_{DDDDR}(typ) = 1.8 V.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MSC8144 when V_{DDDDR}(typ) = 1.8 V.

Table 6. DDR2 SDRAM DC Electrical Characteristics for V_{DDDDR} (typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage[1]	V_{DDDDR}	1.7	1.9	V
I/O reference voltage[2]	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage[3]	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V
Output leakage current[4]	I_{OZ}	–50	50	µA
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}.
4. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

2.5.1.2 DDR (2.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM component(s) of the MSC8144 when V_{DDDDR}(typ) = 2.5 V.

Table 7. DDR SDRAM DC Electrical Characteristics for V_{DDDDR} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage[1]	V_{DDDDR}	2.3	2.7	V
I/O reference voltage[2]	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage[3]	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.15$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.15$	V
Output leakage current[4]	I_{OZ}	–50	50	µA
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}.
4. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

Table 8 lists the current draw characteristics for MV_{REF}.

Table 8. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REF}	I_{MVREF}	—	500	µA

Note: The voltage regulator for MV_{REF} must be able to supply up to 500 µA current.

2.6.3 Reset Timing

The MSC8144 has several inputs to the reset logic:

- Power-on reset ($\overline{\text{PORESET}}$)
- External hard reset ($\overline{\text{HRESET}}$)
- External soft reset ($\overline{\text{SRESET}}$)
- Software watchdog reset
- JTAG reset
- RapidIO reset
- Software hard reset
- Software soft reset

All MSC8144 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. Table 17 describes the reset sources.

Table 17. Reset Sources

Name	Direction	Description
Power-on reset ($\overline{\text{PORESET}}$)	Input	Initiates the power-on reset flow that resets the MSC8144 and configures various attributes of the MSC8144. On $\overline{\text{PORESET}}$, the entire MSC8144 device is reset. All PLLs states is reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the extended cores are reset, and system configuration is sampled. The reset source and word are configured only when $\overline{\text{PORESET}}$ is asserted.
External hard reset ($\overline{\text{HRESET}}$)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8144. While $\overline{\text{HRESET}}$ is asserted, $\overline{\text{SRESET}}$ is also asserted. $\overline{\text{HRESET}}$ is an open-drain pin. Upon hard reset, $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are driven, the extended cores are reset, and system configuration is sampled. Note that the RCW (reset Configuration Word) is not reloaded during $\overline{\text{HRESET}}$ assertion after out of power on reset sequence. The reset configuration word is described in the Reset chapter in the *MSC8144 Reference Manual*.
External soft reset ($\overline{\text{SRESET}}$)	Input/ Output	Initiates the soft reset flow. The MSC8144 detects an external assertion of $\overline{\text{SRESET}}$ only if it occurs while the MSC8144 is not asserting reset. $\overline{\text{SRESET}}$ is an open-drain pin. Upon soft reset, $\overline{\text{SRESET}}$ is driven, the extended cores are reset, and system configuration is maintained.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.
Software watchdog reset	Internal	When the MSC8144 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
RapidIO reset	Internal	When the RapidIO logic asserts the RapidIO hard reset signal, it generates an internal hard reset sequence.
Software hard reset	Internal	A hard reset sequence can be initialized by writing to a memory mapped register (RCR)
Software soft reset	Internal	A soft reset sequence can be initialized by writing to a memory mapped register (RCR)

Table 18 summarizes the reset actions that occur as a result of the different reset sources.

Table 18. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset ($\overline{\text{PORESET}}$)	Hard Reset ($\overline{\text{HRESET}}$)	Soft Reset ($\overline{\text{SRESET}}$)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (Refer to **Section 2.6.3.2** for details).	Yes	No	No	No
PLL state reset	Yes	No	No	No
Select reset configuration source	Yes	No	No	No
System reset configuration write	Yes	No	No	No

2.6.5.8 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for template measurements is the continuous jitter test pattern (CJPAT) defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.9 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (baud frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of **IEEE** Std. 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 V differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of **IEEE** Std. 802.3ae.

2.6.5.10 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ω resistive ±5% differential to 2.5 GHz.

2.6.5.11 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in **Section 2.6.5.9** and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in Figure 14 and Table 35. Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in Section 8.6 is then added to the signal and the test load is replaced by the receiver being tested.

2.6.6 PCI Timing

This section describes the general AC timing parameters of the PCI bus. Table 36 provides the PCI AC timing specifications.

Table 36. PCI AC Timing Specifications

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	
Output delay	t_{PCVAL}	2.0	11.0	1.0	6.0	ns
High-Z to Valid Output delay	t_{PCON}	2.0	—	1.0	—	ns
Valid to High-Z Output delay	t_{PCOFF}	—	28	—	14	ns
Input setup	t_{PCSU}	7.0	—	3.0	—	ns
Input hold	t_{PCH}	0	—	0	—	ns

2.6.7 TDM Timing

Table 37. TDM Timing

Characteristic	Symbol	Expression	Min	Max	Units
TDMxRCLK/TDMxTCLK	t_{TDMC}	TC[1]	16	—	ns
TDMxRCLK/TDMxTCLK high pulse width	t_{TDMCH}	(0.5 ± 0.1) × TC[4]	7	—	ns
TDMxRCLK/TDMxTCLK low pulse width	t_{TDMCL}	(0.5 ± 0.1) × TC[4]	7	—	ns
TDM receive all input setup time related to TDMxRCLK TDMxTSYN input setup time related to TDMxTCLK in TSO=0 mode	t_{TDMVKH}		3.6	—	ns
TDM receive all input hold time related to TDMxRCLK TDMxTSYN input hold time related to TDMxTCLK in TSO=0 mode	t_{TDMXKH}		1.9	—	ns
TDMxTCLK high to TDMxTDAT output active[2]	$t_{TDMDHOX}$		2.5	—	ns
TDMxTCLK high to TDMxTDAT output valid[2]	$t_{TDMDHOV}$		—	9.8	ns
All output hold time (except TDMxTSYN) [3]	t_{TDMHOX}		2.5	—	ns
TDMxTCLK high to TDMxTDAT output high impedance[2]	$t_{TDMDHOZ}$		—	9.8	ns
TDMxTCLK high to TDMxTSYN output valid[2]	$t_{TDMSHOV}$		—	9.25	ns
TDMxTSYN output hold time[3]	$t_{TDMSHOX}$		2.0	—	ns

Notes:
1. Values are based on a a maximum frequency of 62.5 MHz. The TDM interface supports any frequency below 62.5 MHz.
2. Values are based on 20 pF capacitive load.
3. Values are based on 10 pF capacitive load.
4. The expression is for common calculations only.

Figure 18 shows the TDM input AC timing.

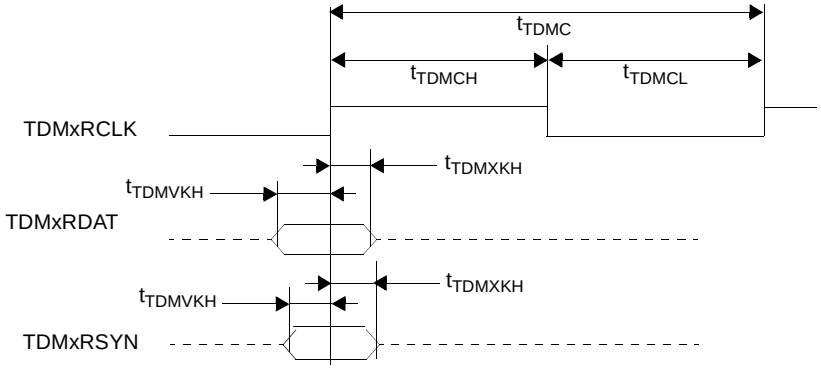


Figure 18. TDM Inputs Signals

Note: For some TDM modes, receive data and receive sync are input on other pins. This timing is also valid for them. See the *MSC8144 Reference Manual*.

Figure 19 shows TDMxTSYN AC timing in TSO=0 mode.

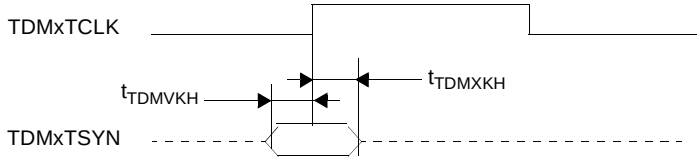
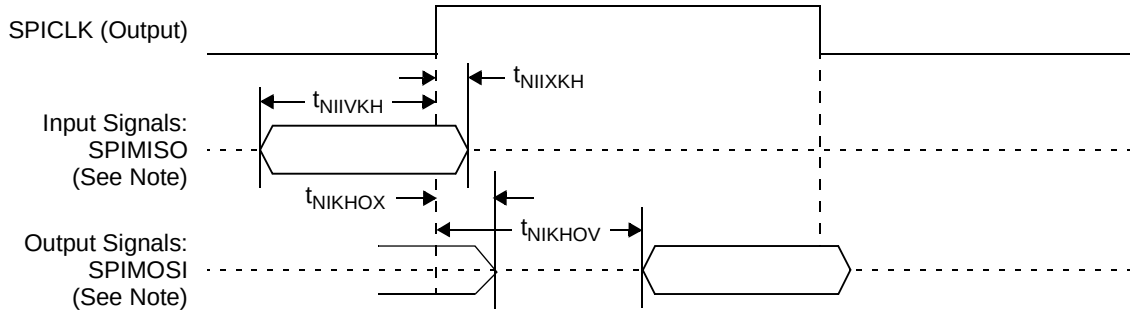


Figure 19. TDMxTSYN in TSO=0 mode

Figure 20 shows the TDM Output AC timing



Note: The clock edge is selectable on SPI.

Figure 36. SPI AC Timing in Master Mode (Internal Clock)

2.6.13 Asynchronous Signal Timing

Table 49. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN cycle[1]
Output	t_{OUT}	Asynchronous	Application dependent
Note: 1. Relevant for EE0, $\overline{\text{IRQ}}$[15–0], and $\overline{\text{NMI}}$ only.			

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a GPI, the input should be driven until it is acknowledged by the device; the GPIO input status is read from a register.

- *EE port.* Signals EE0, EE1, EE2_0, EE2_1, EE2_2, and EE2_3.
- *Boot function*. Signal STOP_BS.
- *I^2C interface*. Signals I2C_SCL and I2C_SDA.
- *Interrupt inputs*. Signals $\overline{\text{IRQ}}$[15–0] and $\overline{\text{NMI}}$.
- *Interrupt outputs*. Signals $\overline{\text{INT\_OUT}}$ and $\overline{\text{NMI\_OUT}}$ (pulse width is 10 ns).

Figure 37 shows the behavior of the asynchronous signals.

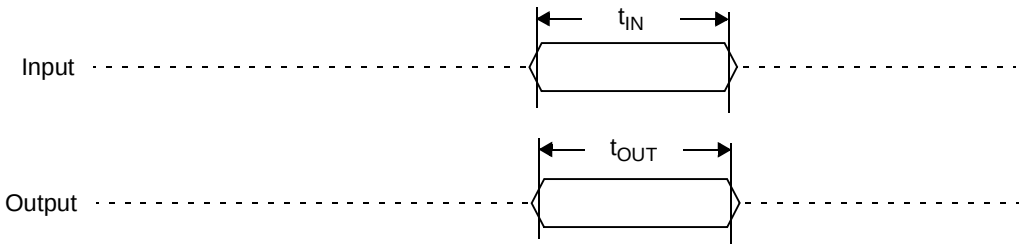


Figure 37. Asynchronous Signal Timing

Table 52. Connectivity of DDR Related Pins When Using 16-bit DDR Memory Only (continued)

Signal Name	Pin connection
$\overline{\text{MWE}}$	in use
MV_{REF}	$1/2*V_{DDDDR}$
V_{DDDDR}	2.5 V or 1.8 V

3.4.1.3 ECC Unused Pin Connections

When the error code corrected mechanism is not used in any 32- or 16-bit DDR configuration, refer to Table 53 to determine the correct pin connections.

Table 53. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[0–7]	pull-up to V_{DDDDR}
ECC_MDM	NC
ECC_MDQS	pull-down to GND
$\overline{\text{ECC\_MDQS}}$	pull-up to V_{DDDDR}

3.4.2 Serial RapidIO Interface Related Pins

3.4.2.1 Serial RapidIO interface Is Not Used

Table 54. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	GND
SRIO_IMP_CAL_TX	GND
$\overline{\text{SRIO\_REF\_CLK}}$	GND
SRIO_REF_CLK	GND
SRIO_RXD[0–3]	GND
$\overline{\text{SRIO\_RXD[0–3]}}$	GND
$\overline{\text{SRIO\_TXD[0–3]}}$	NC
SRIO_TXD[0–3]	NC
$V_{DDRIOPLL}$	GND
GND_{RIOPLL}	GND
GND_{SXP}	GND
GND_{SXC}	GND
V_{DDSXP}	GND
V_{DDSXC}	GND

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	NC
GE2_TD[0–3]	NC
GE2_TX_EN	NC

3.4.4.3 GE1 and GE2 Management Pins

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used (that is, V_{DDGE2} is connected to GND), Table 61 lists the recommended management pin connections.

Table 61. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

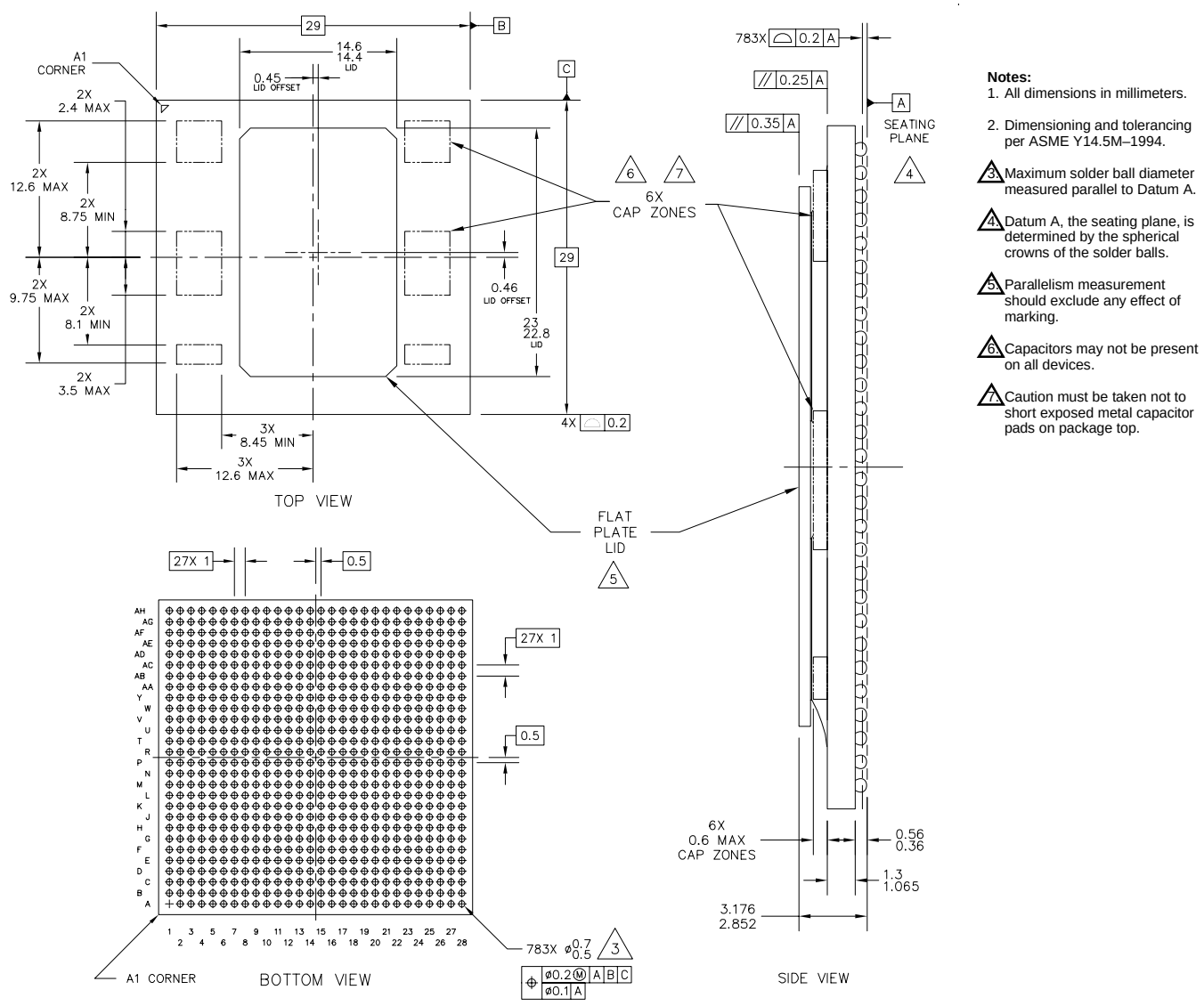
3.4.5 UTOPIA/POS Related Pins

Table 62 lists the board connections of the UTOPIA/POS pins when the entire UTOPIA/POS interface is not used or subset of UTOPIA/POS interface is used. For multiplexing options that select a subset of the UTOPIA/POS interface, use the connections described in Table 62 for those signals that are not selected. Table 62 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 62. Connectivity of UTOPIA/POS Related Pins When UTOPIA/POS Interface Is Not Used

Signal Name	Pin Connection
UTP_IR	GND
UTP_RADDR[0–4]	V_{DDIO}
UTP_RCLAV_PDRPA	NC
UTP_RCLK	GND
UTP_RD[0–15]	GND
$\overline{\text{UTP\_REN}}$	V_{DDIO}
UTP_RPRTY	GND
UTP_RSOC	GND
UTP_TADDR[0–4]	V_{DDIO}
UTP_TCLAV	NC
UTP_TCLK	GND
UTP_TD[0–15]	NC
$\overline{\text{UTP\_TEN}}$	V_{DDIO}
UTP_TPRTY	NC
UTP_TSOC	NC
V_{DDIO}	3.3 V

5 Package Information



Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement should exclude any effect of marking.
6. Capacitors may not be present on all devices.
7. Caution must be taken not to short exposed metal capacitor pads on package top.

CASE NO. 1842-04

Figure 44. MSC8144 Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

- *MSC8144 Technical Data Sheet* (MSC8144). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8144 device.
- *MSC8144 Reference Manual* (MSC8144RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes.* Cover various programming topics related to the StarCore DSP core and the MSC8144 device.
- *SC3400 DSP Core Reference Manual*. Covers the SC3400 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8144 SC3400 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

Table 66 provides a revision history for this data sheet.

Table 66. Document Revision History

Rev.	Date	Description
0	Feb. 2007	• Initial public release.
1	Apr. 2007	• Adds new I/O multiplexing mode 7 that supports POS functionality. • Updates reference voltage supply for pins G5, H7, and H8 in Table 1. • Updates start-up timing recommendations with regard to $\overline{\text{TRST}}$ and $\overline{\text{M3\_RESET}}$ in Section 2.7.1. • Adds input clock duty cycles in Table 20. • Updates PCI AC timings in Table 41. • Removes UTOPIA internal clock specifications in Table 52. • Updates JTAG timings in Table 56. • Clarifies connectivity guidelines for Ethernet pins in Section 3.3.4. • Miscellaneous pin connectivity guidelines were updated in Table 71. • Updates name of core subsystem reference manual.
2	June 2007	• Corrected AA4 definition in Table 1. Changed TDM5TD3 to correct name TDM5TDAT. • Removed Figure 35 because the device does not support UTOPIA using an internal clock. Renumbered subsequent figures. • Removed Section 3.5 *Thermal Considerations*. To be replaced with an application note.
3	Sep 2007	• Updated M3 voltage range in Table 3. • Changed note in Table 7 for PLL power supplies. • DDR voltage designator changed from V_{DD} to V_{DDDDR} in Table 8, Table 10, **Section 2.7.4.1**, **Section 2.7.4.2**, and Figure 11. Changed range on I_{OZ} in Table 8 and Table 10. • Deleted text before Table 13 and added note 2 to input pin capacitance. • Deleted text before Table 14, added a 1 to the note, and added note 1 to input pin capacitance. • Deleted **Section 2.6.5** on page 32 and renumbered subsequent subsections. • Deleted text before new **Section 2.6.5.1**. • Added a 1 to the note in Table 15 and added note 1 to input pin capacitance. • Deleted ac voltage rows from Table 16. Added note 1 to input pin capacitance. • Changed output high and low voltage levels in Table 17 and Table 18. • Deleted text before Table 19. • Added clock skew ranges in percent in Table 21. • Changed V_{REF} to MV_{REF} in Table 26. • Changed V_{DD} to V_{DDIO} in Table 41 Updated note 2. • Added note 4 to Table 42. Changed $t_{TDMSHOX}$ value. • Changed V_{DD} to V_{DDGE} in Figure 27 and Figure 30. • Changed the value of the data to clock out skew in Table 51. • Changed EE pin timing in Table 55. • Changed the head for the JTAG timing section, now **Section 2.7.15**. • Updated JTAG timing for TCK cycle time, TCK high phase, and boundary scan input data hold time in Table 56. • Added new **Section 3.3** with guidelines for board layout for clock and timing signals. Renumbered subsequent sections.
4	Sep 2007	• Changed leakage current values in Table 13, Table 14, Table 11, Table 16, Table 17, Table 18, and Table 19 from –10 and 10 µa to –30 and 30 µa. • Change the minimum value of t_{MDDVKH} in Table 45 from 5 ns to 7 ns. • Updated note 1 in Table 45.
5	Oct 2007	• Corrected column numbering in Figure 3 and Figure 4. • Updated SPI signal names in Table 1.
6	Oct 2007	• Updated SPI signal names in Table 1.

Table 66. Document Revision History (continued)

Rev.	Date	Description
7	Dec 2007	• Changed minimum voltage level for V_{DDM3} to 1.213 (1.25 – 3%) in Table 3. • Added POS to titles in **Section 2.6.6**. • Added additional signals to titles in **Section 2.6.8**. Added high and low voltage ranges to Table 19. • Added ATM and POS to headings in **Section 2.7.11**. Changed characteristics to generic input/output in Table 52, Figure 33, and Figure 34. • Replaced **Sections 2.7.13** and **2.7.14** with new **Section 2.7.13**, *Asynchronous Signal Timing*. Renumbered subsequent sections, tables, and figures. • Added POS to all UTOPIA references in **Section 3.4.5**.
8	Dec 2007	• Changed GCR4 program value to 0x0004C130 in Note 7 in Table 51.
9	Mar 2008	• Changed description of Table 20 in **Section 2.7.2**.
10	Apr 2008	• Added [3] to the PLL supply voltage row in **Table 2**. • Changed the first sentence in **Section 3.4.8** to reflect that **Table 70** indicates what to do with pins if they are "not" required by the design. Changed the Pin Connection for GPIO[0–31] to GND. • Updated ordering information in **Section 4**. • Multiple corrections of minor punctuation errors.
11	Aug 2008	• Removed the comment about preliminary estimates before Table 4 and removed non-DDR rows in the table. • Table 9 and Table 11 for DDR and DDR2 SDRAM capacitance removed and subsequent tables renumbered. • Changed units for I_{OH} and I_{OL} to mA in Table 9. • Removed signal low and high input current from Table 12. • Added a note to Table 15 to exclude TDM and TMS. Removed reference to overshoot and undershoot and associated figure. • Changed minimum clock frequency to 33 MHz and maximum clock frequency to 133 MHz in Table 16. • Deleted old Table 17 Clock Parameters. • Changed minimum input clock frequency to 33 MHz in Table 19. • Changed the t_{DDKHAX} minimum value in Table 23 to 1.85 ns. • Removed t_{REFPJ} and t_{REFCJ} from Table 24 because the specifications are not required or tested. • Removed $t_{PCRSTCLK}$, $t_{PCRSTOFF}$, t_{PCRST}, and t_{PCRHFA} from Table 36 because the specifications are not required or tested. • Removed t_{UAVKH} and t_{UAVXH} from Table 38 because the specifications are not required or tested. • The parameters t_{MDCH}, t_{MDCR}, and t_{MDHF} were removed from Table 40 because the specifications are not required or tested. • The parameters t_{MTXH}/t_{MTX}, t_{MTXR}, and t_{MTXF} were removed from Table 41 because the specifications are not required or tested. • The parameters t_{MRXH}/t_{MRX}, t_{MRXR}, and t_{MRXF} were removed from Table 42 because the specifications are not required or tested. • The parameters t_{RMXH}/t_{RMX}, t_{RMXR}, and t_{RMXF} were removed from Table 43 because the specifications are not required or tested. • Removed the parameters t_{RGT}, t_{RGTH}/t_{RGT} (1000Base-T), t_{RGTH}/t_{RGT} (10Base-T), t_{RGTR}, t_{RGTF}, t_{G12}, and t_{G125H}/t_{G125} were removed from Table 45 and Table 46 because the specifications are not required or tested. • Changed t_{UEKHOX} to guaranteed by design in Table 47. • Updated Figure 35 and Figure 36 SPI timing diagrams. • Removed TCK rise and fall time from Table 50. • Updated orderable part numbers in **Section 4**.
12	Aug 2008	• Changed b8t to bit in the M3 memory description on the first page. • Changed maximum input high voltage (VIH) for SPI to 3.465 in the first row of Table 14. • Changed packet processor to QUICC Engine Subsystem in the last row of Table 18.
13	Feb 2009	• In Figure 31, for GTX_CLK, changed (at transmitter) to (at DSP) and for RX_CLK, changed (at PHY) to (at DSP). • Updated package drawing to the latest revision, Case No. 1842-04 in Figure 44.
14	Jul 2009	• Updated MV_{REF} equations and temperature ranges in Table 3. • Updated orderable part numbers to **Section 4**.
15	Nov 2009	• Updated Core and PLL input voltage tolerance in Table 3.
16	May 2010	• Corrected typo in Table 23. Changed MCLK minimum time to 5 ns.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 010 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: MSC8144
Rev. 16
5/2010

freescale™
semiconductor