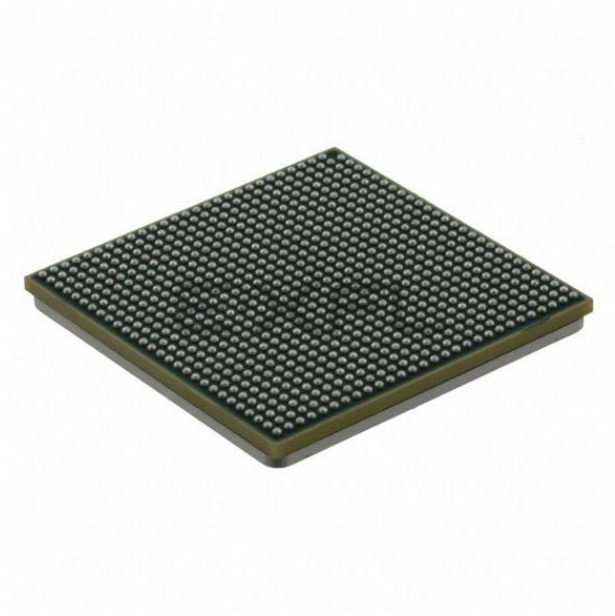

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	Ethernet, I²C, SPI, TDM, UART, UTOPIA
Clock Rate	1GHz
Non-Volatile Memory	External
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8144svt1000a

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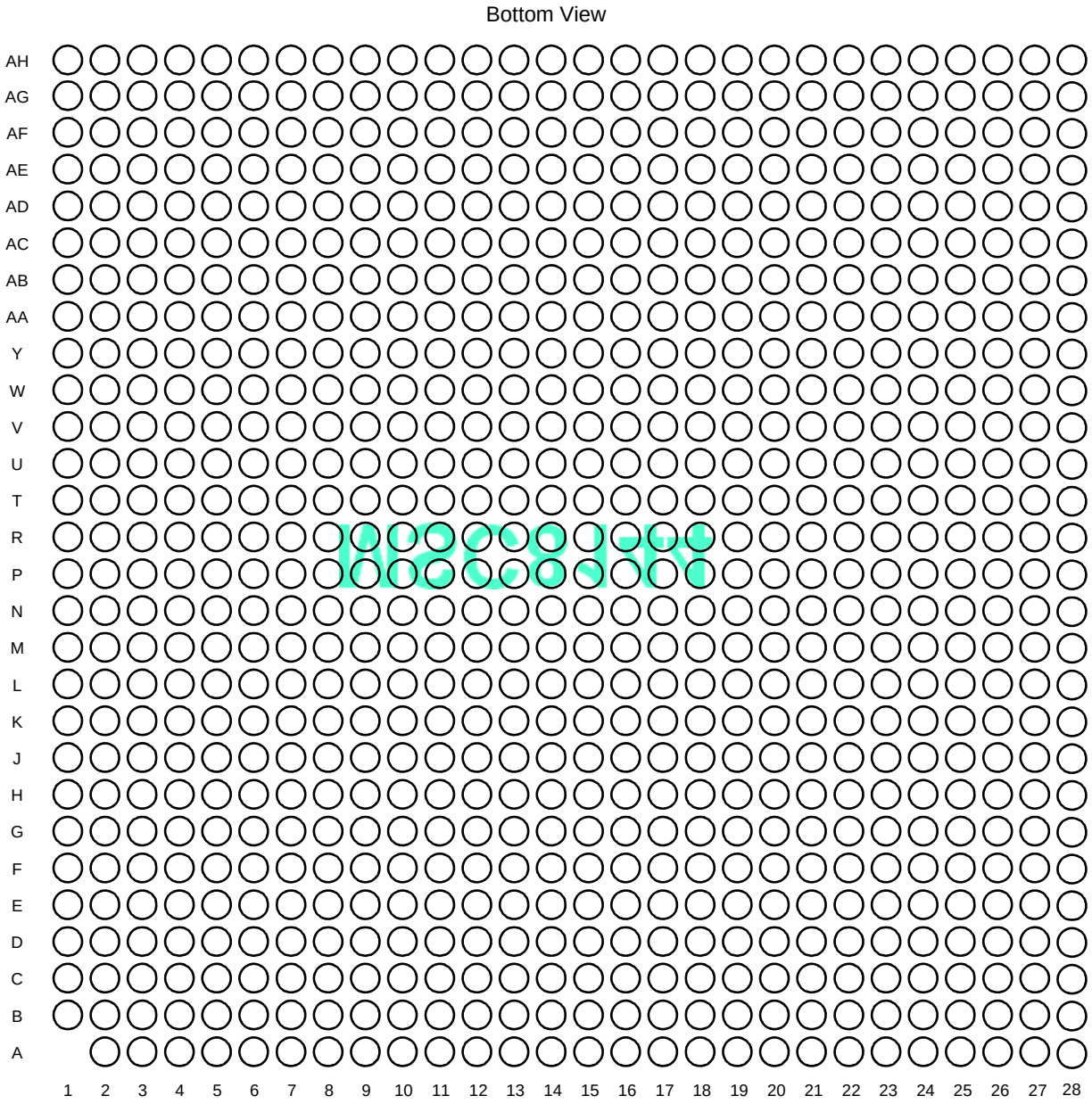


Figure 4. MSC8144 FC-PBGA Package, Bottom View

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A4	V_{DDGE2}										V_{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A6	GE2_TD0/$\overline{\text{PCI\_CBE0}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A7	SRIO_IMP_CAL_RX										V_{DDSXC}
A8	Reserved[1]										—
A9	Reserved[1]										—
A10	Reserved[1]										—
A11	Reserved[1]										—
A12	SRIO_RXD0										V_{DDSXC}
A13	V_{DDSXC}										V_{DDSXC}
A14	SRIO_RXD1										V_{DDSXC}
A15	V_{DDSXC}										V_{DDSXC}
A16	$\overline{\text{SRIO\_REF\_CLK}}$										V_{DDSXC}
A17	$V_{DDRIOPLL}$										GND_{RIOPLL}
A18	GND_{SXC}										GND_{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A20	V_{DDSXC}										V_{DDSXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A22	V_{DDSXC}										V_{DDSXC}
A23	SRIO_IMP_CAL_TX										V_{DDSXP}
A24	MDQ28										V_{DDDDR}
A25	MDQ29										V_{DDDDR}
A26	MDQ30										V_{DDDDR}
A27	MDQ31										V_{DDDDR}
A28	$\overline{\text{MDQS3}}$										V_{DDDDR}
B1	Reserved[1]										—
B2	GE2_TD1/$\overline{\text{PCI\_CBE1}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B3	GE2_TX_EN/$\overline{\text{PCI\_CBE2}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B4	GE_MDIO		Ethernet								V_{DDGE2}
B5	GND										GND
B6	GE_MDC		Ethernet								V_{DDGE2}
B7	GND_{SXC}										GND_{SXC}
B8	Reserved[1]										—
B9	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
T21	GND										GND
T22	V_{DDDDR}										V_{DDDDR}
T23	GND										GND
T24	V_{DDDDR}										V_{DDDDR}
T25	GND										GND
T26	V_{DDDDR}										V_{DDDDR}
T27	GND										GND
T28	V_{DDDDR}										V_{DDDDR}
U1	Reserved[1]										—
U2	UTP_TCLK/PCI_AD29		UTOPIA		PCI	UTOPIA					V_{DDIO}
U3	UTP_TADDR4/PCI_AD27		UTOPIA		PCI	UTOPIA					V_{DDIO}
U4	UTP_TADDR2		UTOPIA								V_{DDIO}
U5	GND										GND
U6	$\overline{\text{UTP\_REN}}$/PCI_AD20		UTOPIA		PCI	UTOPIA					V_{DDIO}
U7	PCI_AD26		PCI								V_{DDIO}
U8	PCI_AD25		PCI								V_{DDIO}
U9	Reserved[1]										V_{DDIO}
U10	V_{DDM3}										V_{DDM3}
U11	GND										GND
U12	V_{DDM3}										V_{DDM3}
U13	GND										GND
U14	V_{DDM3}										V_{DDM3}
U15	GND										GND
U16	V_{DDM3}										V_{DDM3}
U17	GND										GND
U18	V_{DDM3}										V_{DDM3}
U19	GND										GND
U20	V_{DDM3}										V_{DDM3}
U21	GND										GND
U22	GND										GND
U23	MDQ7										V_{DDDDR}
U24	MDQ3										V_{DDDDR}
U25	MDQ4										V_{DDDDR}
U26	MDQ5										V_{DDDDR}
U27	MDQ1										V_{DDDDR}
U28	MDQ0										V_{DDDDR}
V1	Reserved[1]										—
V2	UTP_TD10/$\overline{\text{PCI\_CBE0}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
V3	UTP_TADDR3		UTOPIA								V_{DDIO}
V4	UTP_TD1/$\overline{\text{PCI\_PERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
V5	UTP_TADDR0/PCI_AD23		UTOPIA		PCI	UTOPIA					V_{DDIO}
V6	UTP_TADDR1/PCI_AD24		UTOPIA		PCI	UTOPIA					V_{DDIO}
V7	UTP_TCLAV/PCI_AD28		UTOPIA		PCI	UTOPIA					V_{DDIO}

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8144.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8144.

Note: DDR SDRAM uses V_{DDDDR}(typ) = 2.5 V and DDR2 SDRAM uses V_{DDDDR}(typ) = 1.8 V.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MSC8144 when V_{DDDDR}(typ) = 1.8 V.

Table 6. DDR2 SDRAM DC Electrical Characteristics for V_{DDDDR} (typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit
I/O supply voltage[1]	V_{DDDDR}	1.7	1.9	V
I/O reference voltage[2]	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V
I/O termination voltage[3]	V_{TT}	$MV_{REF} - 0.04$	$MV_{REF} + 0.04$	V
Input high voltage	V_{IH}	$MV_{REF} + 0.125$	$V_{DDDDR} + 0.3$	V
Input low voltage	V_{IL}	–0.3	$MV_{REF} - 0.125$	V
Output leakage current[4]	I_{OZ}	–50	50	µA
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times.
2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of V_{DDDDR}.
4. Output leakage is measured with all outputs are disabled, $0 V \le V_{OUT} \le V_{DDDDR}$.

2.6.3 Reset Timing

The MSC8144 has several inputs to the reset logic:

- Power-on reset (PORESET)
- External hard reset (HRESET)
- External soft reset (SRESET)
- Software watchdog reset
- JTAG reset
- RapidIO reset
- Software hard reset
- Software soft reset

All MSC8144 reset sources are fed into the reset controller, which takes different actions depending on the source of the reset. The reset status register indicates the most recent sources to cause a reset. Table 17 describes the reset sources.

Table 17. Reset Sources

Name	Direction	Description
Power-on reset (PORESET)	Input	Initiates the power-on reset flow that resets the MSC8144 and configures various attributes of the MSC8144. On PORESET, the entire MSC8144 device is reset. All PLLs states is reset, HRESET and SRESET are driven, the extended cores are reset, and system configuration is sampled. The reset source and word are configured only when PORESET is asserted.
External hard reset (HRESET)	Input/ Output	Initiates the hard reset flow that configures various attributes of the MSC8144. While HRESET is asserted, SRESET is also asserted. HRESET is an open-drain pin. Upon hard reset, HRESET and SRESET are driven, the extended cores are reset, and system configuration is sampled. Note that the RCW (reset Configuration Word) is not reloaded during HRESET assertion after out of power on reset sequence. The reset configuration word is described in the Reset chapter in the *MSC8144 Reference Manual*.
External soft reset (SRESET)	Input/ Output	Initiates the soft reset flow. The MSC8144 detects an external assertion of SRESET only if it occurs while the MSC8144 is not asserting reset. SRESET is an open-drain pin. Upon soft reset, SRESET is driven, the extended cores are reset, and system configuration is maintained.
Host reset command through the TAP	Internal	When a host reset command is written through the Test Access Port (TAP), the TAP logic asserts the soft reset signal and an internal soft reset sequence is generated.
Software watchdog reset	Internal	When the MSC8144 watchdog count reaches zero, a software watchdog reset is signalled. The enabled software watchdog event then generates an internal hard reset sequence.
RapidIO reset	Internal	When the RapidIO logic asserts the RapidIO hard reset signal, it generates an internal hard reset sequence.
Software hard reset	Internal	A hard reset sequence can be initialized by writing to a memory mapped register (RCR)
Software soft reset	Internal	A soft reset sequence can be initialized by writing to a memory mapped register (RCR)

Table 18 summarizes the reset actions that occur as a result of the different reset sources.

Table 18. Reset Actions for Each Reset Source

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTEST, CLAMP, or HIGHZ
Configuration pins sampled (Refer to **Section 2.6.3.2** for details).	Yes	No	No	No
PLL state reset	Yes	No	No	No
Select reset configuration source	Yes	No	No	No
System reset configuration write	Yes	No	No	No

2.6.4 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.4.1 DDR SDRAM Input Timings

Table 20 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 2.5 V.

Table 20. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V
Note: At recommended operating conditions with V_{DDDDR} of 2.5 ± 5%.				

Table 21 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 21. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.8 ± 5%.				

Table 22 provides the input AC timing specifications for the DDR SDRAM interface.

Table 22. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit
Controller Skew for MDQS—MDQ/MECC/MDM[1]	t_{CISKEW}			
• 400 MHz		–365	365	ps
• 333 MHz		–390	390	ps
• 266 MHz		–428	428	ps
• 200 MHz		–490	490	ps

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) ± 5%

Figure 8 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

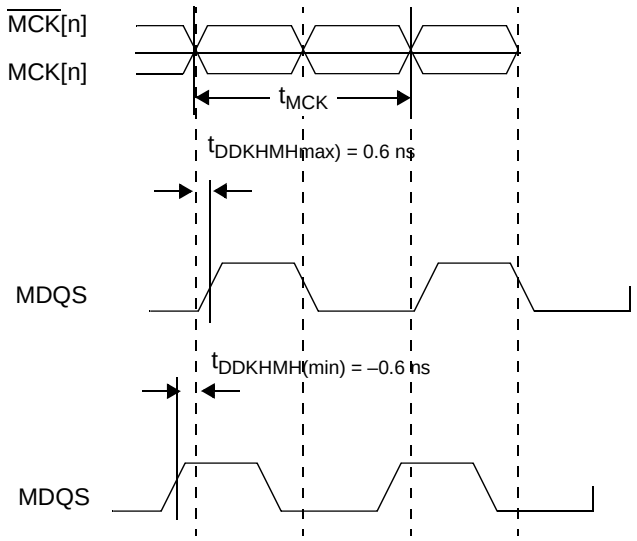


Figure 8. Timing for t_{DDKHMH}

Figure 9 shows the DDR SDRAM output timing diagram.

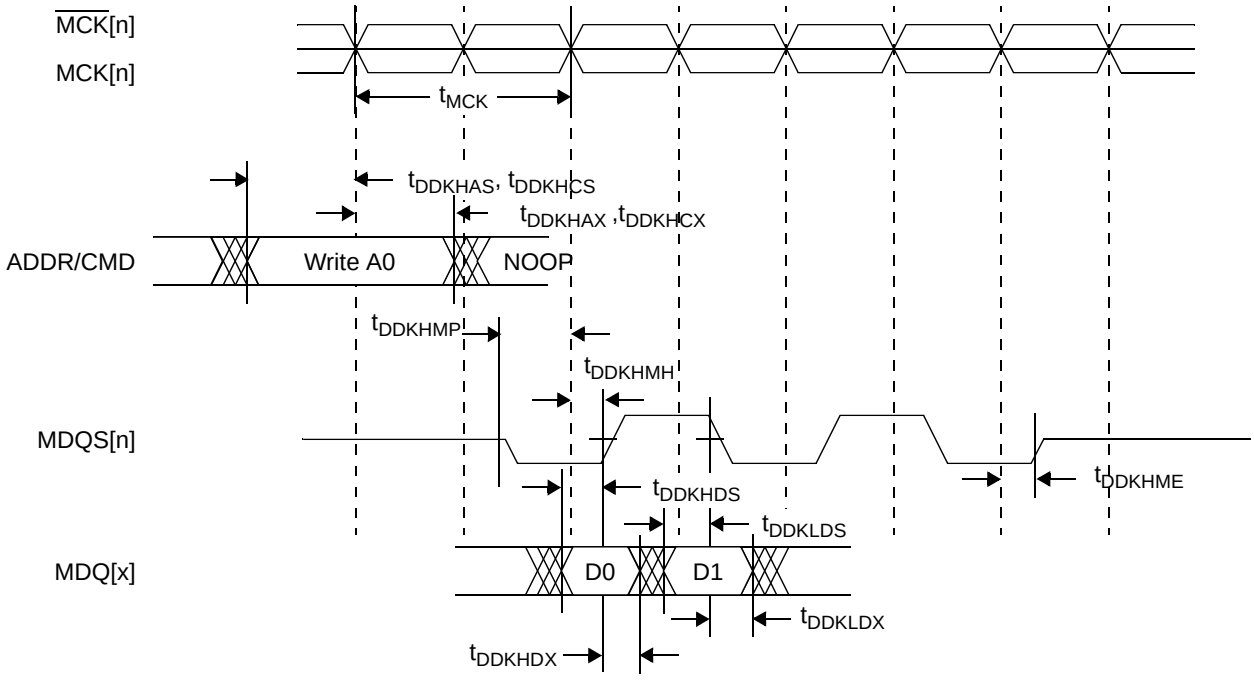


Figure 9. DDR SDRAM Output Timing

Table 25. Short Run Transmitter AC Timing Specifications—1.25 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 26. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple Output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 27. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

Table 28. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

2.6.5.6 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 32, Table 33, and Table 34) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 14 with the parameters specified in Table 35. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω ±5% differential resistive load.

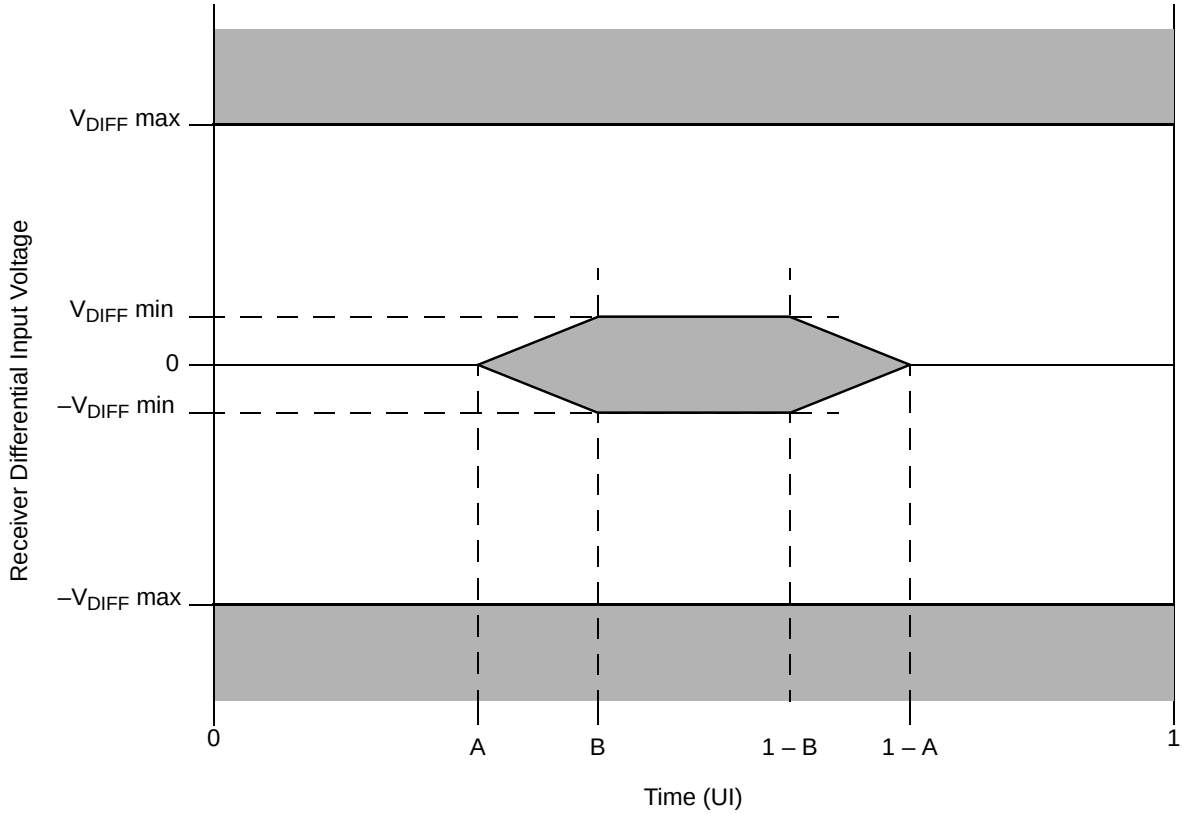


Figure 14. Receiver Input Compliance Mask

Table 35. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

2.6.5.7 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of **IEEE** Std. 802.3ae-2002™, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of **IEEE** Std. 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of **IEEE** Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

Figure 28 shows the RMII transmit and receive AC timing diagram.

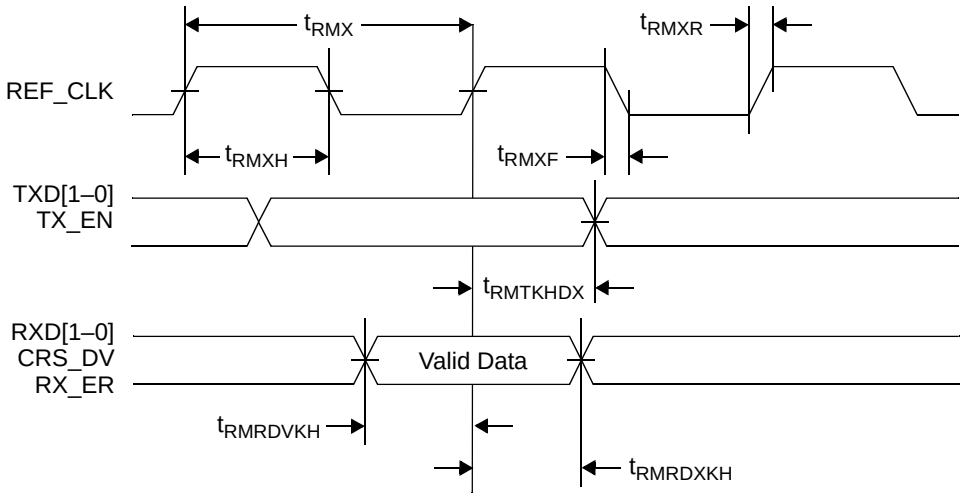


Figure 28. RMII Transmit and Receive AC Timing

Figure 29 provides the AC test load.

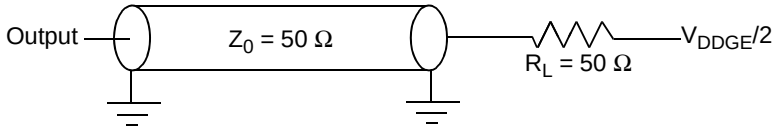


Figure 29. AC Test Load

2.6.10.5 SMII AC Timing Specification

Table 44. SMII Mode Signal Timing

Characteristics	Symbol	Min	Max	Unit
ETHSYNC_IN, ETHRXD to ETHCLOCK rising edge setup time	t_{SMDVKH}	1.5	—	ns
ETHCLOCK rising edge to ETHSYNC_IN, ETHRXD hold time	t_{SMDXKH}	1.0	—	ns
ETHCLOCK rising edge to ETHSYNC, ETHTXD output delay	t_{SMXR}	1.5	5.0	ns

Notes:
1. Typical REF_CLK clock period is 8ns
2. Measured using a 5 pF load.
3. Measured using a 15 pF load
4. Program GCR4 as 0x00002008

Figure 30 shows the SMII Mode signal timing.

Figure 31 shows the RGMII AC timing and multiplexing diagrams.

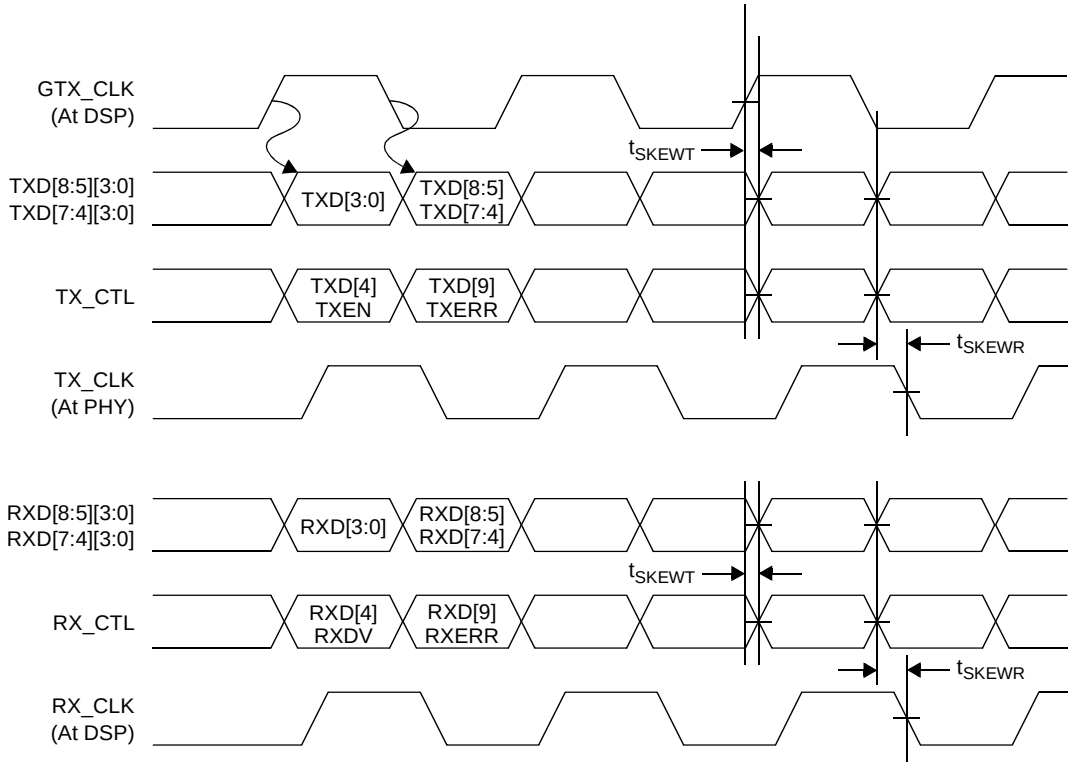


Figure 31. RGMII AC Timing and Multiplexing

2.6.11 ATM/UTOPIA/POS Timing

Table 47 provides the ATM/UTOPIA/POS input and output AC timing specifications.

Table 47. ATM/UTOPIA/POS AC Timing (External Clock) Specifications

Characteristic	Symbol	Min	Max	Unit
Outputs—External clock delay	t_{UEKHOV}	1	9	ns
Outputs—External clock High Impedance[1]	t_{UEKHOX}	1	9	ns
Inputs—External clock input setup time	t_{UEIVKH}	4		ns
Inputs—External clock input hold time	t_{UEIXKH}	1		ns

Notes:
1. Not tested. Guaranteed by design.
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. Although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 32 provides the AC test load for the ATM/UTOPIA/POS.

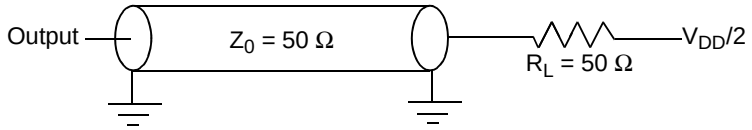


Figure 32. ATM/UTOPIA/POS AC Test Load

Figure 33 shows the ATM/UTOPIA/UTOPIA timing with external clock.

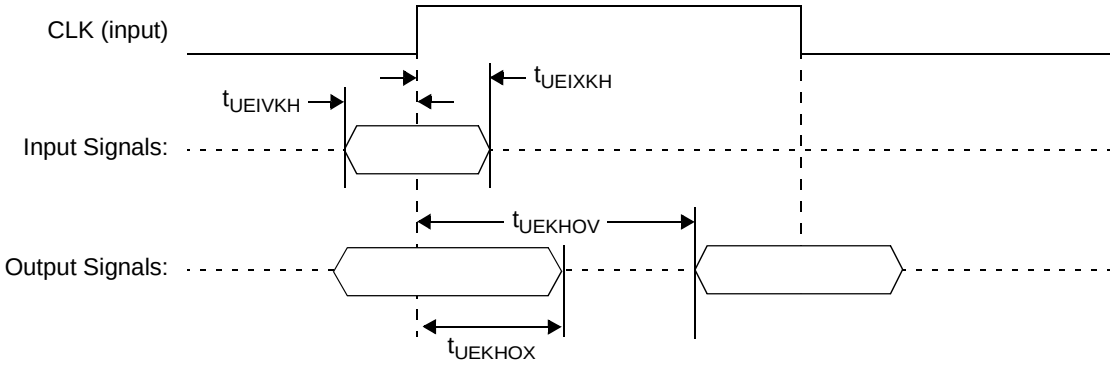


Figure 33. ATM/UTOPIAPOS AC Timing (External Clock)

2.6.12 SPI Timing

Table 48 lists the SPI input and output AC timing specifications.

Table 48. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t_{NIKHOV}		6	ns
SPI outputs hold—Master mode (internal clock) delay	t_{NIKHOX}	0.5		ns
SPI outputs valid—Slave mode (external clock) delay	t_{NEKHOV}		8	ns
SPI outputs hold—Slave mode (external clock) delay	t_{NEKHOX}	2		ns
SPI inputs—Master mode (internal clock input) setup time	t_{NIIVKH}	4		ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0		ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4		ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2		ns

Notes:
1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Figure 34 provides the AC test load for the SPI.

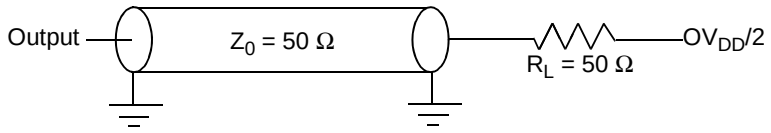
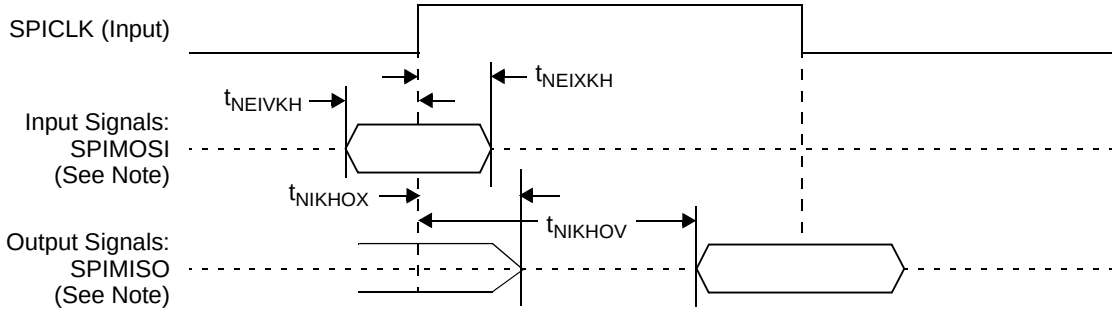


Figure 34. SPI AC Test Load

Figure 35 and Figure 36 represent the AC timings from Table 48. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 35 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 35. SPI AC Timing in Slave Mode (External Clock)

Figure 36 shows the SPI timings in master mode (internal clock).

Table 51. Connectivity of DDR Related Pins When the DDR Interface Is Not Used (continued)

Signal Name	Pin Connection
MDM[0–3]	NC
MBA[0–2]	NC
$\overline{\text{MCAS}}$	NC
MCKE[0–1]	NC
MODT[0–1]	NC
MDIC[0–1]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[0–7]	NC
ECC_MDM	NC
ECC_MDQS	NC
$\overline{\text{ECC\_MDQS}}$	NC
MV_{REF}	GND
V_{DDDDR}	GND
Note: If the DDR controller is not used, disable the internal DDR clock by writing a 1 to the CLK11DIS bit in the System Clock Control Register (SCCR[CLK!11DIS]). See **Chapter 7**, *Clocks*, in the ***MSC8144 Reference Manual*** for details.	

3.4.1.2 16-Bit DDR Memory Only

Table 52 lists unused pin connection when using 16-bit DDR memory. The 16 most significant data lines are not used.

Table 52. Connectivity of DDR Related Pins When Using 16-bit DDR Memory Only

Signal Name	Pin connection
MDQ[0–15]	in use
MDQ[16–31]	pull-up to V_{DDDDR}
MDQS[0–1]	in use
MDQS[2–3]	pull-down to GND
$\overline{\text{MDQS[0–1]}}$	in use
$\overline{\text{MDQS[2–3]}}$	pull-up to V_{DDDDR}
MA[0–15]	in use
MCK[0–2]	in use
$\overline{\text{MCK[0–2]}}$	in use
$\overline{\text{MCS[0–1]}}$	in use
MDM[0–1]	in use
MDM[2–3]	NC
MBA[0–2]	in use
$\overline{\text{MCAS}}$	in use
MCKE[0–1]	in use
MODT[0–1]	in use
MDIC[0–1]	in use
$\overline{\text{MRAS}}$	in use

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	NC
GE2_TD[0–3]	NC
GE2_TX_EN	NC

3.4.4.3 GE1 and GE2 Management Pins

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used (that is, V_{DDGE2} is connected to GND), Table 61 lists the recommended management pin connections.

Table 61. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

3.4.5 UTOPIA/POS Related Pins

Table 62 lists the board connections of the UTOPIA/POS pins when the entire UTOPIA/POS interface is not used or subset of UTOPIA/POS interface is used. For multiplexing options that select a subset of the UTOPIA/POS interface, use the connections described in Table 62 for those signals that are not selected. Table 62 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 62. Connectivity of UTOPIA/POS Related Pins When UTOPIA/POS Interface Is Not Used

Signal Name	Pin Connection
UTP_IR	GND
UTP_RADDR[0–4]	V_{DDIO}
UTP_RCLAV_PDRPA	NC
UTP_RCLK	GND
UTP_RD[0–15]	GND
$\overline{\text{UTP\_REN}}$	V_{DDIO}
UTP_RPRTY	GND
UTP_RSOC	GND
UTP_TADDR[0–4]	V_{DDIO}
UTP_TCLAV	NC
UTP_TCLK	GND
UTP_TD[0–15]	NC
$\overline{\text{UTP\_TEN}}$	V_{DDIO}
UTP_TPRTY	NC
UTP_TSOC	NC
V_{DDIO}	3.3 V

3.4.6 TDM Interface Related Pins

Table 63 lists the board connections of the TDM pins when an entire specific TDM is not used. For multiplexing options that select a subset of a TDM interface, use the connections described in Table 63 for those signals that are not selected. Table 63 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 63. Connectivity of TDM Related Pins When TDM Interface Is Not Used

Signal Name	Pin Connection
TDM***x***RCLK	GND
TDM***x***RDAT	GND
TDM***x***RSYN	GND
TDM***x***TCLK	GND
TDMT***x***DAT	GND
TDM***x***TSYN	GND
V_{DDIO}	3.3 V

Notes: **1.** ***x*** = {0, 1, 2,3, 4, 5, 6, 7}
2. In case of subset of TDM interface usage please make sure to disable unused TDM modules. See **Chapter 20**, *TDM*, in the ***MSC8144 Reference Manual*** for details.

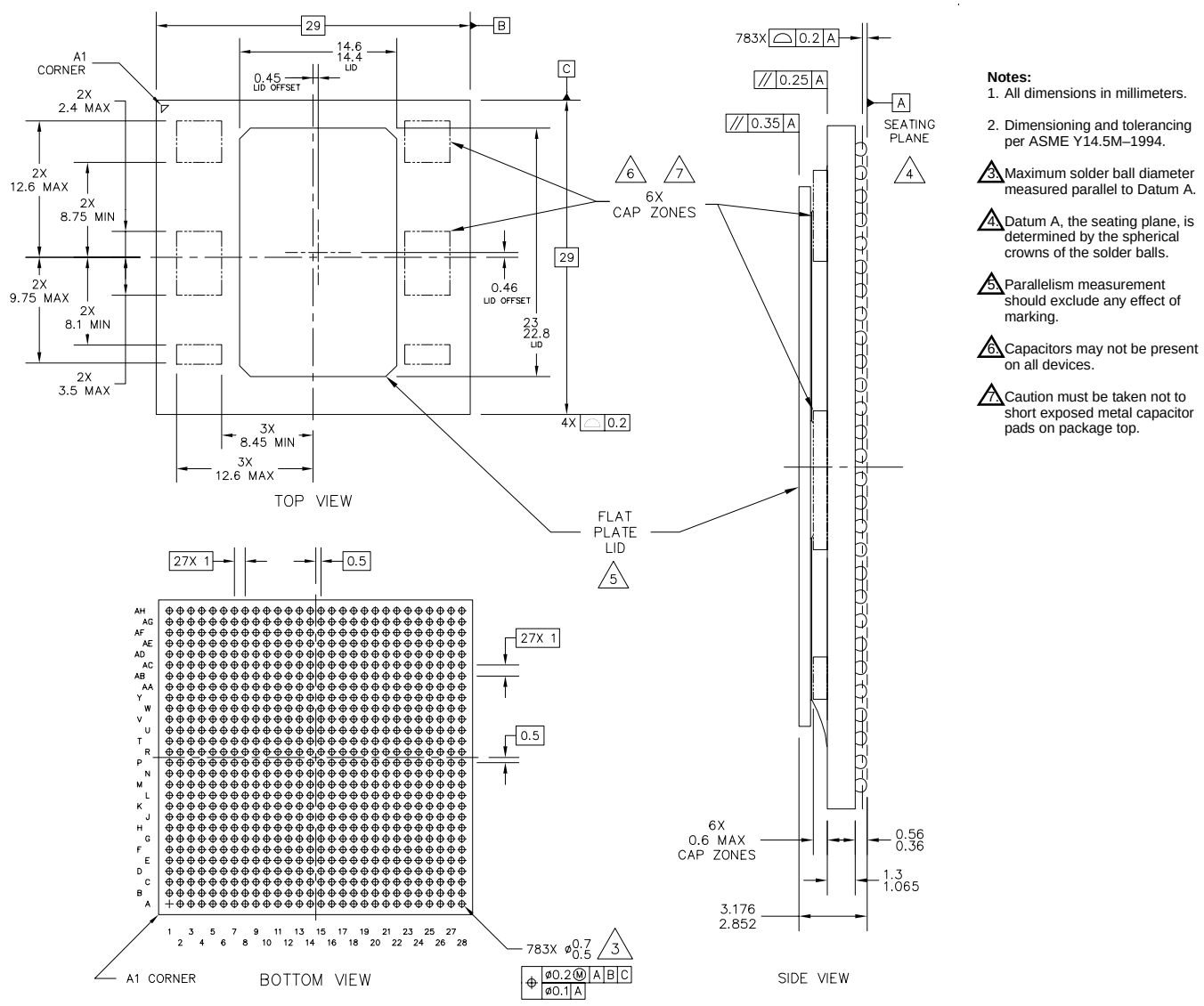
3.4.7 PCI Related Pins

Table 64 lists the board connections of the pins when PCI is not used. Table 64 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 64. Connectivity of PCI Related Pins When PCI Is Not Used

Signal Name	Pin Connection
PCI_AD[0–31]	GND
$\overline{\text{PCI\_CBE[0–3]}}$	GND
PCI_CLK_IN	GND
$\overline{\text{PCI\_DEVSEL}}$	V_{DDIO}
$\overline{\text{PCI\_FRAME}}$	V_{DDIO}
$\overline{\text{PCI\_GNT}}$	V_{DDIO}
PCI_IDS	GND
$\overline{\text{PCI\_IRDY}}$	V_{DDIO}
PCI_PAR	GND
$\overline{\text{PCI\_PERR}}$	V_{DDIO}
$\overline{\text{PCI\_REQ}}$	NC
$\overline{\text{PCI\_SERR}}$	V_{DDIO}
$\overline{\text{PCI\_STOP}}$	V_{DDIO}
$\overline{\text{PCI\_TRDY}}$	V_{DDIO}
V_{DDIO}	3.3 V

5 Package Information



Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement should exclude any effect of marking.
6. Capacitors may not be present on all devices.
7. Caution must be taken not to short exposed metal capacitor pads on package top.

CASE NO. 1842-04

Figure 44. MSC8144 Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

- *MSC8144 Technical Data Sheet* (MSC8144). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8144 device.
- *MSC8144 Reference Manual* (MSC8144RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes.* Cover various programming topics related to the StarCore DSP core and the MSC8144 device.
- *SC3400 DSP Core Reference Manual*. Covers the SC3400 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8144 SC3400 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

Table 66. Document Revision History (continued)

Rev.	Date	Description
7	Dec 2007	• Changed minimum voltage level for V_{DDM3} to 1.213 (1.25 – 3%) in Table 3. • Added POS to titles in **Section 2.6.6**. • Added additional signals to titles in **Section 2.6.8**. Added high and low voltage ranges to Table 19. • Added ATM and POS to headings in **Section 2.7.11**. Changed characteristics to generic input/output in Table 52, Figure 33, and Figure 34. • Replaced **Sections 2.7.13** and **2.7.14** with new **Section 2.7.13**, *Asynchronous Signal Timing*. Renumbered subsequent sections, tables, and figures. • Added POS to all UTOPIA references in **Section 3.4.5**.
8	Dec 2007	• Changed GCR4 program value to 0x0004C130 in Note 7 in Table 51.
9	Mar 2008	• Changed description of Table 20 in **Section 2.7.2**.
10	Apr 2008	• Added [3] to the PLL supply voltage row in **Table 2**. • Changed the first sentence in **Section 3.4.8** to reflect that **Table 70** indicates what to do with pins if they are "not" required by the design. Changed the Pin Connection for GPIO[0–31] to GND. • Updated ordering information in **Section 4**. • Multiple corrections of minor punctuation errors.
11	Aug 2008	• Removed the comment about preliminary estimates before Table 4 and removed non-DDR rows in the table. • Table 9 and Table 11 for DDR and DDR2 SDRAM capacitance removed and subsequent tables renumbered. • Changed units for I_{OH} and I_{OL} to mA in Table 9. • Removed signal low and high input current from Table 12. • Added a note to Table 15 to exclude TDM and TMS. Removed reference to overshoot and undershoot and associated figure. • Changed minimum clock frequency to 33 MHz and maximum clock frequency to 133 MHz in Table 16. • Deleted old Table 17 Clock Parameters. • Changed minimum input clock frequency to 33 MHz in Table 19. • Changed the t_{DDKHAX} minimum value in Table 23 to 1.85 ns. • Removed t_{REFPJ} and t_{REFCJ} from Table 24 because the specifications are not required or tested. • Removed $t_{PCRSTCLK}$, $t_{PCRSTOFF}$, t_{PCRST}, and t_{PCRHFA} from Table 36 because the specifications are not required or tested. • Removed t_{UAVKH} and t_{UAVXH} from Table 38 because the specifications are not required or tested. • The parameters t_{MDCH}, t_{MDCR}, and t_{MDHF} were removed from Table 40 because the specifications are not required or tested. • The parameters t_{MTXH}/t_{MTX}, t_{MTXR}, and t_{MTXF} were removed from Table 41 because the specifications are not required or tested. • The parameters t_{MRXH}/t_{MRX}, t_{MRXR}, and t_{MRXF} were removed from Table 42 because the specifications are not required or tested. • The parameters t_{RMXH}/t_{RMX}, t_{RMXR}, and t_{RMXF} were removed from Table 43 because the specifications are not required or tested. • Removed the parameters t_{RGT}, t_{RGTH}/t_{RGT} (1000Base-T), t_{RGTH}/t_{RGT} (10Base-T), t_{RGTR}, t_{RGTF}, t_{G12}, and t_{G125H}/t_{G125} were removed from Table 45 and Table 46 because the specifications are not required or tested. • Changed t_{UEKHOX} to guaranteed by design in Table 47. • Updated Figure 35 and Figure 36 SPI timing diagrams. • Removed TCK rise and fall time from Table 50. • Updated orderable part numbers in **Section 4**.
12	Aug 2008	• Changed b8t to bit in the M3 memory description on the first page. • Changed maximum input high voltage (VIH) for SPI to 3.465 in the first row of Table 14. • Changed packet processor to QUICC Engine Subsystem in the last row of Table 18.
13	Feb 2009	• In Figure 31, for GTX_CLK, changed (at transmitter) to (at DSP) and for RX_CLK, changed (at PHY) to (at DSP). • Updated package drawing to the latest revision, Case No. 1842-04 in Figure 44.
14	Jul 2009	• Updated MV_{REF} equations and temperature ranges in Table 3. • Updated orderable part numbers to **Section 4**.
15	Nov 2009	• Updated Core and PLL input voltage tolerance in Table 3.
16	May 2010	• Corrected typo in Table 23. Changed MCLK minimum time to 5 ns.

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