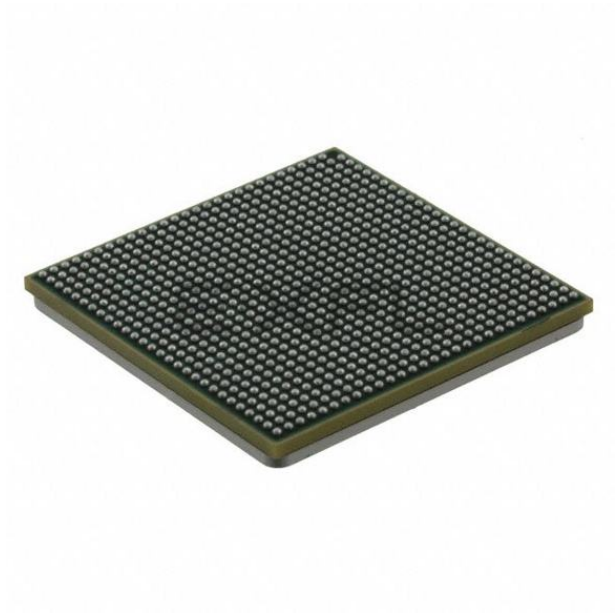

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	Ethernet, I²C, SPI, TDM, UART, UTOPIA
Clock Rate	800MHz
Non-Volatile Memory	External
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8144svt800a

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
B10	Reserved[1]										—
B11	Reserved[1]										—
B12	$\overline{\text{SRIO\_RXD0}}$										V_{DDSXC}
B13	GND_{SXC}										GND_{SXC}
B14	$\overline{\text{SRIO\_RXD1}}$										V_{DDSXC}
B15	GND_{SXC}										GND_{SXC}
B16	SRIO_REF_CLK										V_{DDSXC}
B17	Reserved[1]										—
B18	V_{DDSXC}										V_{DDSXC}
B19	$\overline{\text{SRIO\_RXD2}}$/ $\overline{\text{GE1\_SGMII\_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B20	GND_{SXC}										GND_{SXC}
B21	$\overline{\text{SRIO\_RXD3}}$/ $\overline{\text{GE2\_SGMII\_RX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
B22	GND_{SXC}										GND_{SXC}
B23	GND_{SXP}										GND_{SXP}
B24	MDQ27										V_{DDDDR}
B25	V_{DDDDR}										V_{DDDDR}
B26	GND										GND
B27	V_{DDDDR}										V_{DDDDR}
B28	MDQS3										V_{DDDDR}
C1	Reserved[1]										—
C2	GE2_RX_CLK/PCI_AD29		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C3	V_{DDGE2}										V_{DDGE2}
C4	TDM7RSYN/GE2_TD2/ PCI_AD2/UTP_TER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C5	TDM7RCLK/GE2_RD2/ PCI_AD0/UTP_RVL		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
C6	V_{DDGE2}										V_{DDGE2}
C7	GE2_RD0/PCI_AD27		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
C8	Reserved[1]										—
C9	Reserved[1]										—
C10	Reserved[1]										—
C11	Reserved[1]										—
C12	V_{DDSXP}										V_{DDSXP}
C13	$\overline{\text{SRIO\_TXD0}}$										V_{DDSXP}
C14	V_{DDSXP}										V_{DDSXP}
C15	$\overline{\text{SRIO\_TXD1}}$										V_{DDSXP}
C16	GND_{SXC}										GND_{SXC}
C17	GND_{RIOPLL}										GND_{RIOPLL}
C18	Reserved[1]										—
C19	V_{DDSXP}										V_{DDSXP}
C20	$\overline{\text{SRIO\_TXD2}}$/$\overline{\text{GE1\_SGMII\_TX}}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
G23	MBA1										V_{DDDDR}
G24	MA3										V_{DDDDR}
G25	MA8										V_{DDDDR}
G26	V_{DDDDR}										V_{DDDDR}
G27	GND										GND
G28	$\overline{\text{MCK0}}$										V_{DDDDR}
H1	Reserved[1]										—
H2	CLKIN										V_{DDIO}
H3	$\overline{\text{HRESET}}$										V_{DDIO}
H4	PCI_CLK_IN										V_{DDIO}
H5	$\overline{\text{NMI}}$										V_{DDIO}
H6	URXD/GPIO14/$\overline{\text{IRQ8}}$/ $\overline{\text{RC\_LDF}}$[3, 6]	$\overline{\text{RC\_LDF}}$	UART/GPIO/IRQ								V_{DDIO}
H7	GE1_RX_ER/PCI_AD6/ GPIO25/$\overline{\text{IRQ15}}$[3, 6]		GPIO/ IRQ	Ethernet 1	PCI			GPIO/ IRQ	Ethernet 1		V_{DDIO}
H8	GE1_CRS/PCI_AD5		PCI	Ethernet 1	PCI				Ethernet 1		V_{DDIO}
H9	GND										GND
H10	V_{DD}										V_{DD}
H11	GND										GND
H12	V_{DD}										V_{DD}
H13	GND										GND
H14	V_{DD}										V_{DD}
H15	V_{DD}										V_{DD}
H16	V_{DD}										V_{DD}
H17	GND										GND
H18	V_{DD}										V_{DD}
H19	GND										GND
H20	V_{DD}										V_{DD}
H21	V_{DD}										V_{DD}
H22	V_{DDDDR}										V_{DDDDR}
H23	MBA0										V_{DDDDR}
H24	MA15										V_{DDDDR}
H25	V_{DDDDR}										V_{DDDDR}
H26	MA9										V_{DDDDR}
H27	MA7										V_{DDDDR}
H28	MCK0										V_{DDDDR}
J1	Reserved[1]										—
J2	GND										GND
J3	V_{DDIO}										V_{DDIO}
J4	STOP_BS										V_{DDIO}
J5	$\overline{\text{NMI\_OUT}}$[4]										V_{DDIO}
J6	$\overline{\text{INT\_OUT}}$[4]										V_{DDIO}
J7	SDA/GPIO27[3, 4, 6]		I2C/GPIO								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AD4	GPIO2[3, 6]		GPIO								V_{DDIO}
AD5	GND										GND
AD6	TDM1TCLK		TDM								V_{DDIO}
AD7	TDM3TDAT/RC10	RC10	TDM								V_{DDIO}
AD8	TDM3RSYN/RC9	RC9	TDM								V_{DDIO}
AD9	TDM3RDAT/RC8	RC8	TDM								V_{DDIO}
AD10	GND										GND
AD11	V_{25M3}										V_{25M3}
AD12	GND										GND
AD13	V_{DDM3}										V_{DDM3}
AD14	GND										GND
AD15	V_{25M3}										V_{25M3}
AD16	GND										GND
AD17	V_{DDM3}										V_{DDM3}
AD18	GND										GND
AD19	V_{25M3}										V_{25M3}
AD20	GND										GND
AD21	Reserved[1]										—
AD22	V_{DDDDR}										V_{DDDDR}
AD23	GND										GND
AD24	V_{DDDDR}										V_{DDDDR}
AD25	GND										GND
AD26	V_{DDDDR}										V_{DDDDR}
AD27	GND										GND
AD28	V_{DDDDR}										V_{DDDDR}
AE1	Reserved[1]										—
AE2	GPIO0[3, 6]		GPIO								V_{DDIO}
AE3	GPIO3[3, 6]		GPIO								V_{DDIO}
AE4	TDM1RCLK		TDM								V_{DDIO}
AE5	TDM1TSYN/RC3	RC3	TDM								V_{DDIO}
AE6	TDM1TDAT/RC2	RC2	TDM								V_{DDIO}
AE7	TDM1RSYN/RC1	RC1	TDM								V_{DDIO}
AE8	TDM3RCLK/RC16	RC16	TDM								V_{DDIO}
AE9	TDM3TCLK		TDM								V_{DDIO}
AE10	TDM2TDAT/RC6	RC6	TDM								V_{DDIO}
AE11	GPIO21/$\overline{IRQ1}$[3, 6]/SPICLK		GPIO/IRQ/SPI								V_{DDIO}
AE12	GND										GND
AE13	Reserved[1]										—
AE14	GND										GND
AE15	Reserved[1]										—
AE16	Reserved[1]										—
AE17	Reserved[1]										—
AE18	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AG4	TDM0RSYN/RCW_SRC0	RCW_SRC0	TDM								V_{DDIO}
AG5	TDM0RCLK		TDM								V_{DDIO}
AG6	TDM0TDAT/RCW_SRC1	RCW_SRC1	TDM								V_{DDIO}
AG7	TDM2TSYN/RC7	RC7	TDM								V_{DDIO}
AG8	TDM2RCLK		TDM								V_{DDIO}
AG9	TDM2RSYN/RC5	RC5	TDM								V_{DDIO}
AG10	GPIO24/$\overline{\text{IRQ6}}$[3, 6]/$\overline{\text{SPISEL}}$		GPIO/IRQ/SPI								V_{DDIO}
AG11	GPIO23/$\overline{\text{IRQ5}}$[3, 6]/SPIMISO		GPIO/IRQ/SPI								V_{DDIO}
AG12	Reserved[1]										—
AG13	GND										GND
AG14	GND										GND
AG15	GND										GND
AG16	GND										GND
AG17	Reserved[1]										—
AG18	Reserved[1]										—
AG19	GND										GND
AG20	GND										GND
AG21	V_{DDM3IO}										V_{DDM3IO}
AG22	GND										GND
AG23	GND										GND
AG24	GND										GND
AG25	V_{DDDDR}										V_{DDDDR}
AG26	GND										GND
AG27	V_{DDDDR}										V_{DDDDR}
AG28	GND										GND
AH1	Reserved[1]										—
AH2	Reserved[1]										—
AH3	Reserved[1]										—
AH4	Reserved[1]										—
AH5	Reserved[1]										—
AH6	Reserved[1]										—
AH7	Reserved[1]										—
AH8	Reserved[1]										—
AH9	Reserved[1]										—
AH10	Reserved[1]										—
AH11	Reserved[1]										—
AH12	Reserved[1]										—
AH13	Reserved[1]										—
AH14	Reserved[1]										—
AH15	Reserved[1]										—
AH16	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AH17	Reserved[1]										—
AH18	Reserved[1]										—
AH19	Reserved[1]										—
AH20	Reserved[1]										—
AH21	Reserved[1]										—
AH22	Reserved[1]										—
AH23	Reserved[1]										—
AH24	Reserved[1]										—
AH25	Reserved[1]										—
AH26	Reserved[1]										—
AH27	Reserved[1]										—
AH28	Reserved[1]										—

Notes:
1. Reserved signals should be disconnected for compatibility with future revisions of the device.
2. For signals with same functionality in all modes the appropriate cells are empty.
3. The choice between GPIO function and other function is by GPIO registers setup. For configuration details, see **Chapter 23,** *GPIO* in the *MSC8144 Reference Manual*.
4. Open-drain signal.
5. Internal 20 KΩ pull-up resistor.
6. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See **Chapter 23**, *GPIO* of the *MSC8144 Reference Manual* for configuration details.

2.5.2.2 Spread Spectrum Clock

SRIO_REF_CLK/ $\overline{\text{SRIO\_REF\_CLK}}$ is designed to work with a spread spectrum clock (0 to 0.5% spreading at 3033 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

2.5.3 PCI DC Electrical Characteristics

Table 9. PCI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDPCI}	3.135	3.465	V
Input high voltage	V_{IH}	$0.5 \times V_{DDPCI}$	3.465	V
Input low voltage	V_{IL}	–0.5	$0.3 \times V_{DDPCI}$	V
Input Pull-up voltage[1]	V_{IPU}	$0.7 \times V_{DDPCI}$		
Input leakage current, $0<V_{IN}<V_{DDPCI}$	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current, $0<V_{IN}<V_{DDPCI}$	I_{OZ}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.0 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –0.5 mA, except open drain pins	V_{OH}	$0.9 \times V_{DDPCI}$	—	V
Output low voltage, I_{OL}= 1.5 mA	V_{OL}	—	$0.1 \times V_{DDPCI}$	V
Input Pin Capacitance[1]	C_{IN}		10	pF

Notes: **1.** Not tested. Guaranteed by design.

2.5.4 TDM DC Electrical Characteristics

Table 10. TDM DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDTDM}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current $0<V_{IN}<V_{DDTDM}$	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current	I_{OZ}	–30	30	µA
Output high voltage, I_{OH} = –1.6 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL}= 0.4mA	V_{OL}	—	0.4	V

Table 18. Reset Actions for Each Reset Source (continued)

Reset Action/Reset Source	Power-On Reset (PORESET)	Hard Reset (HRESET)	Soft Reset (SRESET)	
	External only	External or Internal (Software Watchdog, Software or RapidIO)	External or internal Software	JTAG Command: EXTEST, CLAMP, or HIGHZ
HRESET driven	Yes	Yes	No	No
IPBus modules reset (TDM, UART, SWT, DDRC, IPBus master, GIC, HS, and GPIO)	Yes	Yes	Yes	Yes
SRESET driven	Yes	Yes	Yes	Depends on command
Extended cores reset	Yes	Yes	Yes	Yes
CLASS registers reset	Yes	Yes	Some registers	Some registers
Timers, Performance Monitor	Yes	Yes	No	No
QUICC Engine subsystem, PCI, DMA	Yes	Yes	Most registers	Most registers

2.6.3.1 Power-On Reset (PORESET) Pin

Asserting PORESET initiates the power-on reset flow. PORESET must be asserted externally for at least 32 CLKIN cycles after V_{DD} and V_{DDIO} are both at their nominal levels.

2.6.3.2 Reset Configuration

The MSC8144 has two mechanisms for writing the reset configuration:

- Through the I^2C port
- Through external pins
- Through internal hard coded

Twenty-three signals (see **Section 1** for signal description details) are sampled during the power-on reset sequence to define the Reset Word Configuration Source and operating conditions:

- RCW_SRC[2–0]
- RC[16–0]

The RCFG_CLKIN_RNG pin must be valid during power-on or hard reset sequence. The STOP_BS pin must be always valid and is also sampled during power-on reset sequence for RCW loading from an I^2C EEPROM.

2.6.3.3 Reset Timing Tables

Table 19 and Figure 7 describe the reset timing for a reset configuration.

Table 19. Timing for a Reset Configuration Write

No.	Characteristics	Expression	Max	Min	Unit
1	Required external PORESET duration minimum	32/CLKIN			
	• 33 MHz <= CLKIN < 44 MHz		1280	727	ns
	• 44 MHz <= CLKIN < 66 MHz		728	484	ns
	• 66 MHz <= CLKIN < 100 MHz		485	320	ns
	• 100 MHz <= CLKIN < 133 MHz		320	241	ns

2.6.4.2 DDR SDRAM Output AC Timing Specifications

Table 23 provides the output AC timing specifications for the DDR SDRAM interface.

Table 23. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)[2]	t_{MCK}	5	10	ns
ADDR/CMD output setup with respect to MCK[3]	t_{DDKHAS}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
ADDR/CMD output hold with respect to MCK[3]	t_{DDKHAX}			
• 400 MHz		1.85	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
$\overline{\text{MCS}}$n output setup with respect to MCK[3]	t_{DDKHCS}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
$\overline{\text{MCS}}$n output hold with respect to MCK[3]	t_{DDKHCX}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
MCK to MDQS Skew[4]	t_{DDKHMH}	–0.6	0.6	ns
MDQ/MECC/MDM output setup with respect to MDQS[5]	t_{DDKHDS}, t_{DDKLDS}			
• 400 MHz		700	—	ps
• 333 MHz		900	—	ps
• 266 MHz		1100	—	ps
• 200 MHz		1200	—	ps
MDQ/MECC/MDM output hold with respect to MDQS[5]	t_{DDKHDX}, t_{DDKLDX}			
• 400 MHz		700	—	ps
• 333 MHz		900	—	ps
• 266 MHz		1100	—	ps
• 200 MHz		1200	—	ps
MDQS preamble start[6]	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns
MDQS epilogue end[6]	t_{DDKHME}	–0.6	0.6	ns

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MSC8144 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) ± 5%.

Figure 8 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

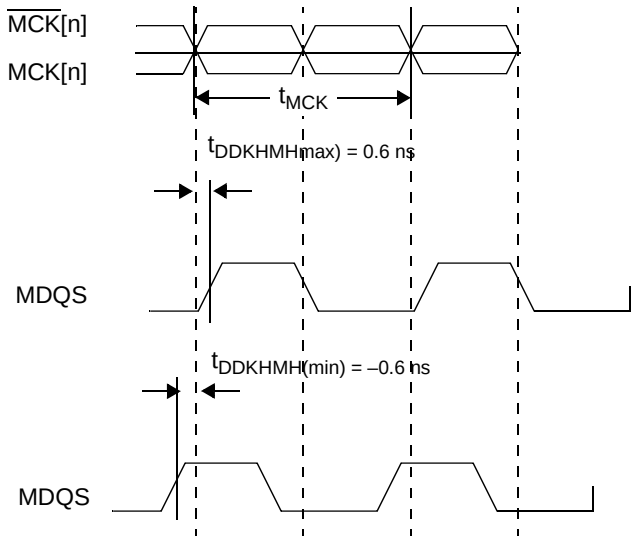

Figure 8. Timing for t_{DDKHMH}

Figure 9 shows the DDR SDRAM output timing diagram.

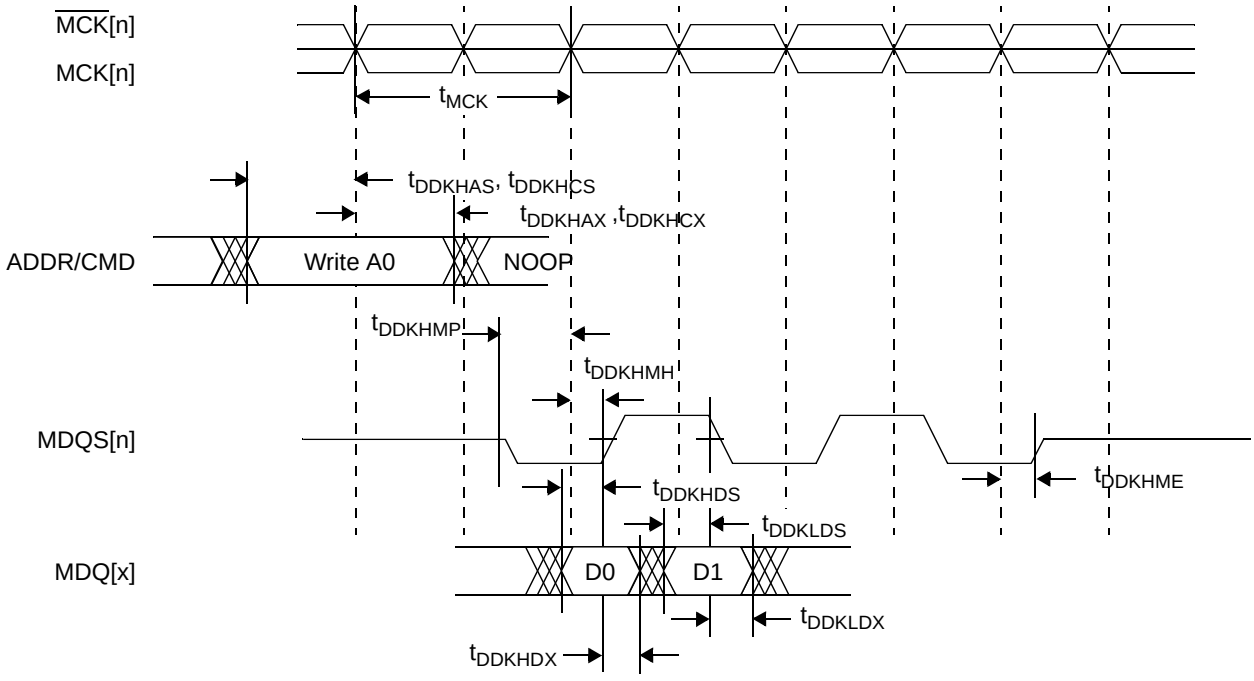

Figure 9. DDR SDRAM Output Timing

Figure 10 provides the AC test load for the DDR bus.

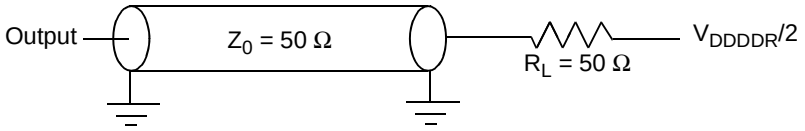

Figure 10. DDR AC Test Load

2.6.5 Serial RapidIO Timing and SGMII Timing

2.6.5.1 AC Requirements for SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$

Table 24 lists AC signal specifications.

Table 24. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Signal Specifications

Parameter Description	Symbol	Min	Typical	Max	Units	Comments
REFCLK cycle time	t_{REF}	—	10 (8, 6.4)	—	ns	8 ns applies only to serial RapidIO system with 125-MHz reference clock. 6.4 ns applies only to serial RapidIO systems with a 156.25 MHz reference clock. **Note:** SGMII uses the 8 ns (125 MHz) value only.

2.6.5.2 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 11 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between voltage levels A and B, where A > B.

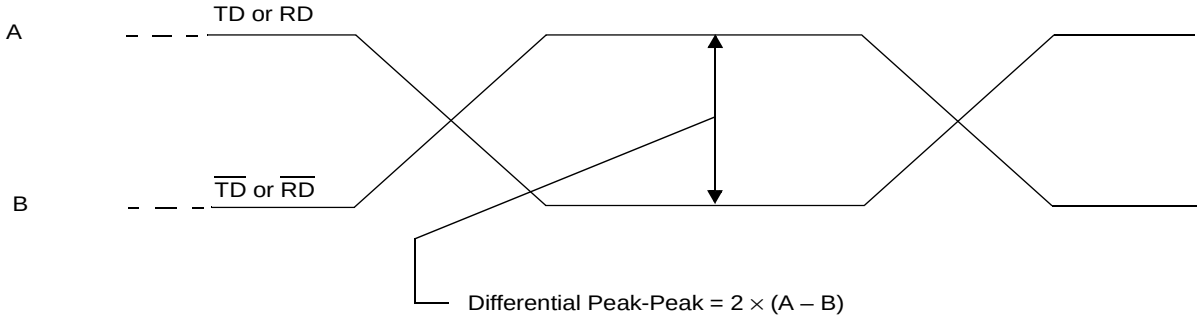

Figure 11. Differential V_{PP} of Transmitter or Receiver

Note: This explanation uses generic TD/$\overline{\text{TD}}$/RD/$\overline{\text{RD}}$ signal names. These correspond to SRIO_TXD/$\overline{\text{SRIO\_TXD}}$/ SRIO_RXD/$\overline{\text{SRIO\_RXD}}$ respectively.

Table 25. Short Run Transmitter AC Timing Specifications—1.25 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 26. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple Output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 27. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

Table 28. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

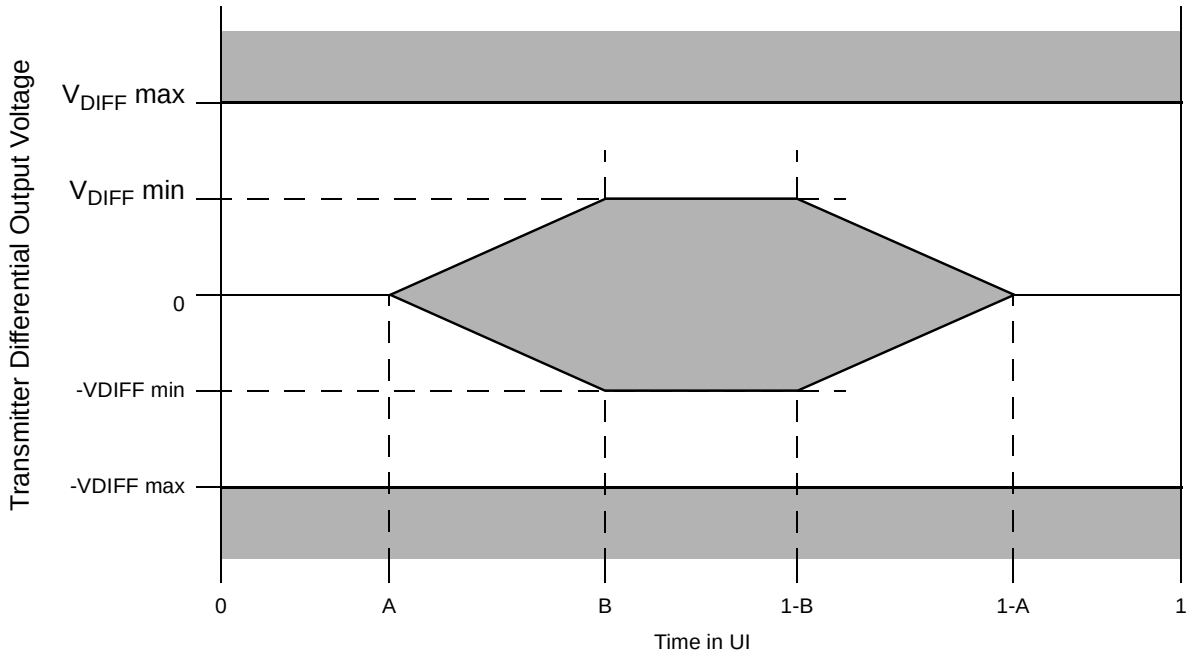

Figure 12. Transmitter Output Compliance Mask

Table 31. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

2.6.5.6 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 32, Table 33, and Table 34) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 14 with the parameters specified in Table 35. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω ±5% differential resistive load.

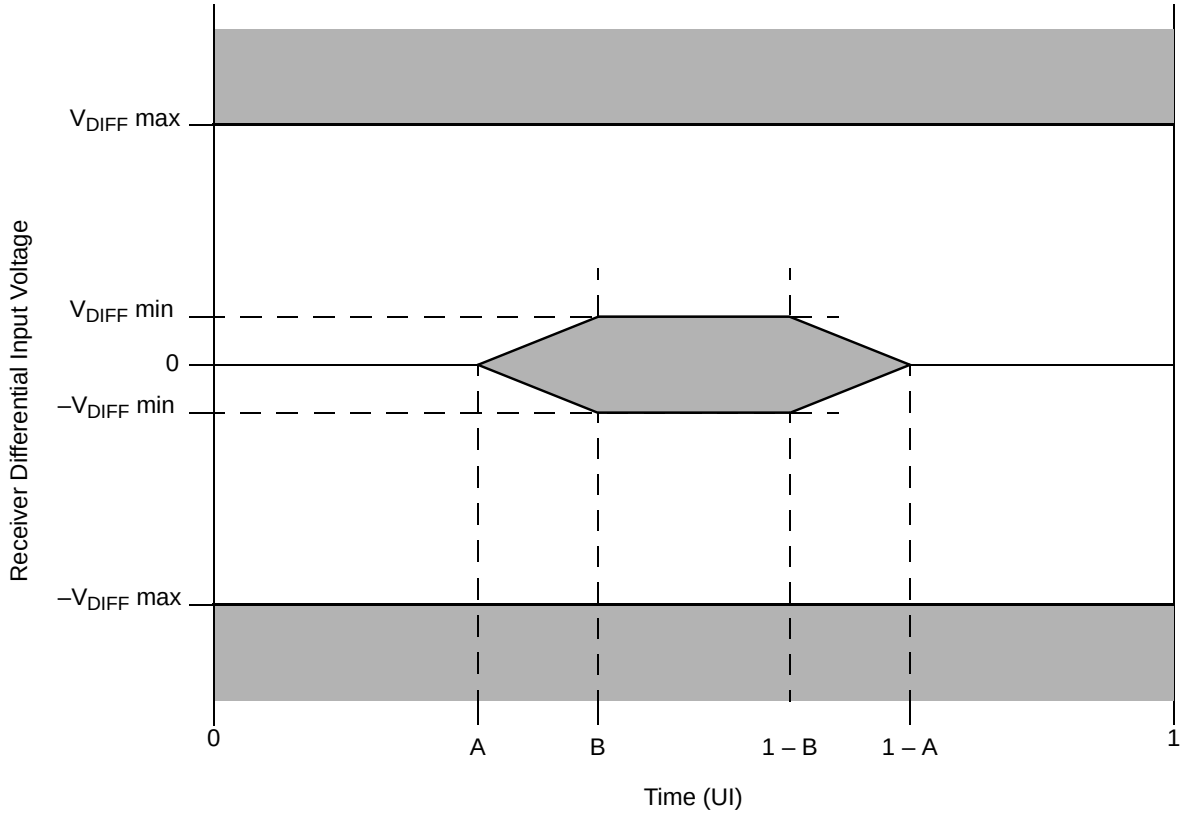

Figure 14. Receiver Input Compliance Mask

Table 35. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

2.6.5.7 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of **IEEE** Std. 802.3ae-2002™, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of **IEEE** Std. 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of **IEEE** Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

2.6.9 Timer Timing

Table 39. Timer Timing

Characteristics	Symbol	Min	Unit
TIMERx frequency	$T_{TMREFCLK}$	10.0	ns
TIMERx Input high phase	T_{TMCH}	4.0	ns
TIMERx Output low phase	T_{TMCL}	4.0	ns

Figure 23 shows the timer input AC timing

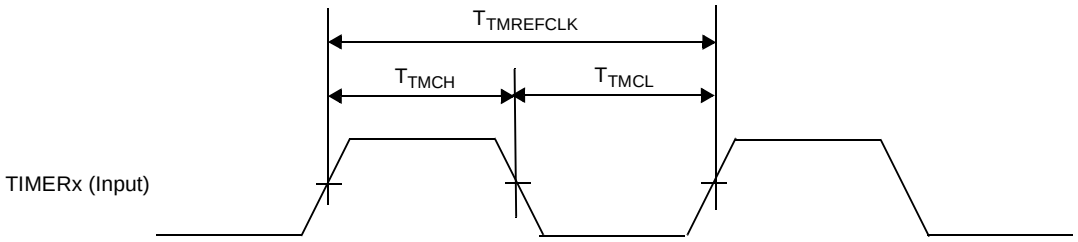

Figure 23. Timer Timing

2.6.10 Ethernet Timing

This section describes the AC electrical characteristics for the Ethernet interface.

There are programmable delay units (PDU) that should be programmed differently for each Interface to meet timing. There is a general configuration register 4 (GCR4) used to configure the timing. For additional information, see the *MSC8144 Reference Manual*.

2.6.10.1 Management Interface Timing

Table 40. Ethernet Controller Management Interface Timing

Characteristics	Symbol	Min	Max	Unit
ETHMDC to ETHMDIO delay[2]	t_{MDKHDX}	10	70	ns
ETHMDIO to ETHMDC rising edge setup time	t_{MDDVKH}	7	—	ns
ETHMDC rising edge to ETHMDIO hold time	t_{MDDXKH}	0	—	ns

Notes:
1. Program the ETHMDC frequency (f_{MDC}) to a maximum value of 2.5 MHz (400 ns period for t_{MDC}). The value depends on the source clock and configuration of MIIMCFG[MCS] and UPSMR[MDCP]. For example, for a source clock of 400 MHz, to achieve f_{MDC} = 2.5 MHz, program MIIMCFG[MCS] = 0x4 and UPSMR[MDCP] = 0. See the *MSC8144 Reference Manual* for configuration details.
2. The value depends on the source clock. For example, for a source clock of 267 MHz, the delay is 70 ns. For a source clock of 333 MHz, the delay is 58 ns.

2.6.14 JTAG Signals

Table 50. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at V_M = 1.6 V	t_{TCKH}	15.0	—	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
$\overline{\text{TRST}}$ assert time	t_{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 38 shows the Test Clock Input Timing Diagram

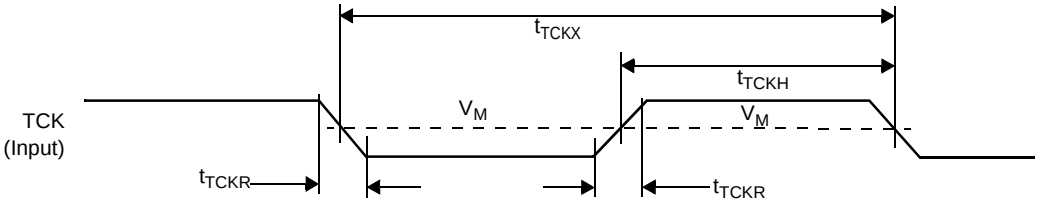

Figure 38. Test Clock Input Timing

Figure 39 shows the boundary scan (JTAG) timing diagram.

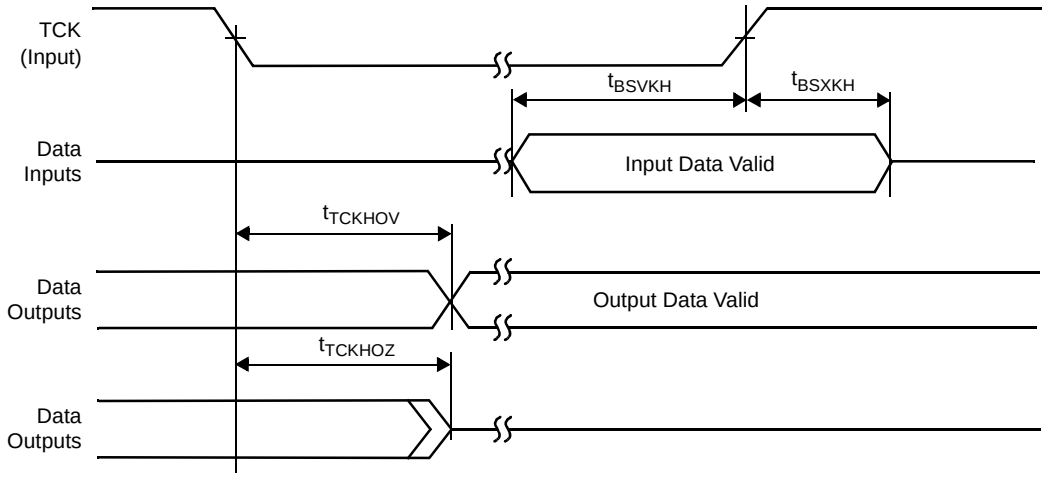

Figure 39. Boundary Scan (JTAG) Timing

The following supplies should rise before any other supplies in any sequence

- V_{DD} and V_{DDPLL} coupled together
- V_{DDM3}

After the above supplies rise to 90% of their nominal value the following I/O supplies may rise in any sequence (see Figure 42):

- V_{DDGE1}
- V_{DDGE2}
- V_{DDIO}
- V_{DDDDR} and MV_{REF} coupled one to another. MV_{REF} should be either at same time or after V_{DDDDR}.
- V_{DDM3IO}
- V_{25M3}

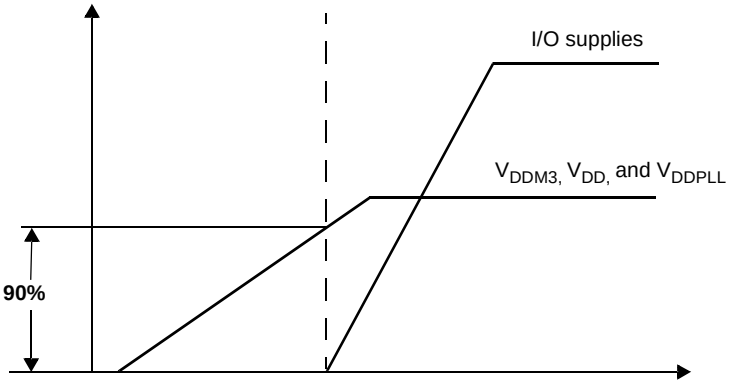

Figure 42. V_{DDM3}, V_{DDM3IO} and V_{25M3} Power-on Sequence

Note:
1. This recommended power sequencing is different from the MSC8122/MSC8126.
2. If no pins that require V_{DDGE1} as a reference supply are used (see Table 1), V_{DDGE1} can be tied to GND.
3. If no pins that require V_{DDGE2} as a reference supply are used (see Table 1), V_{DDGE2} can be tied to GND.
4. If the DDR interface is not used, V_{DDDDR} and MV_{REF} can be tied to GND.
5. If the M3 memory is not used, V_{DDM3}, V_{DDM3IO}, and V_{25M3} can be tied to GND.
6. If the RapidIO interface is not used, V_{DDSX}, V_{DDSXP}, and $V_{DDRIOPLL}$ can be tied to GND.

3.1.2 Start-Up Timing

Section 2.6.1 describes the start-up timing.

Table 52. Connectivity of DDR Related Pins When Using 16-bit DDR Memory Only (continued)

Signal Name	Pin connection
$\overline{\text{MWE}}$	in use
MV_{REF}	$1/2*V_{DDDDR}$
V_{DDDDR}	2.5 V or 1.8 V

3.4.1.3 ECC Unused Pin Connections

When the error code corrected mechanism is not used in any 32- or 16-bit DDR configuration, refer to Table 53 to determine the correct pin connections.

Table 53. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[0–7]	pull-up to V_{DDDDR}
ECC_MDM	NC
ECC_MDQS	pull-down to GND
$\overline{\text{ECC\_MDQS}}$	pull-up to V_{DDDDR}

3.4.2 Serial RapidIO Interface Related Pins

3.4.2.1 Serial RapidIO interface Is Not Used

Table 54. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	GND
SRIO_IMP_CAL_TX	GND
$\overline{\text{SRIO\_REF\_CLK}}$	GND
SRIO_REF_CLK	GND
SRIO_RXD[0–3]	GND
$\overline{\text{SRIO\_RXD[0–3]}}$	GND
$\overline{\text{SRIO\_TXD[0–3]}}$	NC
SRIO_TXD[0–3]	NC
$V_{DDRIOPLL}$	GND
GND_{RIOPLL}	GND
GND_{SXP}	GND
GND_{SXC}	GND
V_{DDSXP}	GND
V_{DDSXC}	GND

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	NC
GE2_TD[0–3]	NC
GE2_TX_EN	NC

3.4.4.3 GE1 and GE2 Management Pins

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used (that is, V_{DDGE2} is connected to GND), Table 61 lists the recommended management pin connections.

Table 61. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

3.4.5 UTOPIA/POS Related Pins

Table 62 lists the board connections of the UTOPIA/POS pins when the entire UTOPIA/POS interface is not used or subset of UTOPIA/POS interface is used. For multiplexing options that select a subset of the UTOPIA/POS interface, use the connections described in Table 62 for those signals that are not selected. Table 62 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 62. Connectivity of UTOPIA/POS Related Pins When UTOPIA/POS Interface Is Not Used

Signal Name	Pin Connection
UTP_IR	GND
UTP_RADDR[0–4]	V_{DDIO}
UTP_RCLAV_PDRPA	NC
UTP_RCLK	GND
UTP_RD[0–15]	GND
$\overline{\text{UTP\_REN}}$	V_{DDIO}
UTP_RPRTY	GND
UTP_RSOC	GND
UTP_TADDR[0–4]	V_{DDIO}
UTP_TCLAV	NC
UTP_TCLK	GND
UTP_TD[0–15]	NC
$\overline{\text{UTP\_TEN}}$	V_{DDIO}
UTP_TPRTY	NC
UTP_TSOC	NC
V_{DDIO}	3.3 V

7 Revision History

Table 66 provides a revision history for this data sheet.

Table 66. Document Revision History

Rev.	Date	Description
0	Feb. 2007	• Initial public release.
1	Apr. 2007	• Adds new I/O multiplexing mode 7 that supports POS functionality. • Updates reference voltage supply for pins G5, H7, and H8 in Table 1. • Updates start-up timing recommendations with regard to $\overline{\text{TRST}}$ and $\overline{\text{M3\_RESET}}$ in Section 2.7.1. • Adds input clock duty cycles in Table 20. • Updates PCI AC timings in Table 41. • Removes UTOPIA internal clock specifications in Table 52. • Updates JTAG timings in Table 56. • Clarifies connectivity guidelines for Ethernet pins in Section 3.3.4. • Miscellaneous pin connectivity guidelines were updated in Table 71. • Updates name of core subsystem reference manual.
2	June 2007	• Corrected AA4 definition in Table 1. Changed TDM5TD3 to correct name TDM5TDAT. • Removed Figure 35 because the device does not support UTOPIA using an internal clock. Renumbered subsequent figures. • Removed Section 3.5 *Thermal Considerations*. To be replaced with an application note.
3	Sep 2007	• Updated M3 voltage range in Table 3. • Changed note in Table 7 for PLL power supplies. • DDR voltage designator changed from V_{DD} to V_{DDDDR} in Table 8, Table 10, **Section 2.7.4.1**, **Section 2.7.4.2**, and Figure 11. Changed range on I_{OZ} in Table 8 and Table 10. • Deleted text before Table 13 and added note 2 to input pin capacitance. • Deleted text before Table 14, added a 1 to the note, and added note 1 to input pin capacitance. • Deleted **Section 2.6.5** on page 32 and renumbered subsequent subsections. • Deleted text before new **Section 2.6.5.1**. • Added a 1 to the note in Table 15 and added note 1 to input pin capacitance. • Deleted ac voltage rows from Table 16. Added note 1 to input pin capacitance. • Changed output high and low voltage levels in Table 17 and Table 18. • Deleted text before Table 19. • Added clock skew ranges in percent in Table 21. • Changed V_{REF} to MV_{REF} in Table 26. • Changed V_{DD} to V_{DDIO} in Table 41 Updated note 2. • Added note 4 to Table 42. Changed $t_{TDMSHOX}$ value. • Changed V_{DD} to V_{DDGE} in Figure 27 and Figure 30. • Changed the value of the data to clock out skew in Table 51. • Changed EE pin timing in Table 55. • Changed the head for the JTAG timing section, now **Section 2.7.15**. • Updated JTAG timing for TCK cycle time, TCK high phase, and boundary scan input data hold time in Table 56. • Added new **Section 3.3** with guidelines for board layout for clock and timing signals. Renumbered subsequent sections.
4	Sep 2007	• Changed leakage current values in Table 13, Table 14, Table 11, Table 16, Table 17, Table 18, and Table 19 from –10 and 10 µa to –30 and 30 µa. • Change the minimum value of t_{MDDVKH} in Table 45 from 5 ns to 7 ns. • Updated note 1 in Table 45.
5	Oct 2007	• Corrected column numbering in Figure 3 and Figure 4. • Updated SPI signal names in Table 1.
6	Oct 2007	• Updated SPI signal names in Table 1.