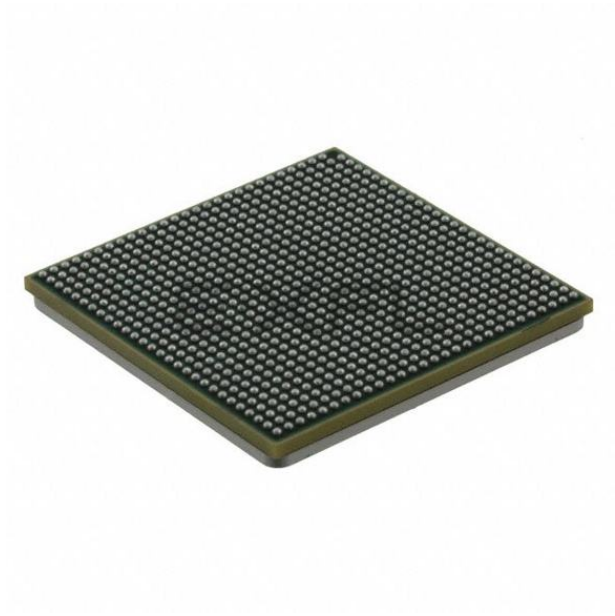

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	Ethernet, I²C, SPI, TDM, UART, UTOPIA
Clock Rate	1GHz
Non-Volatile Memory	External
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8144tvt1000a

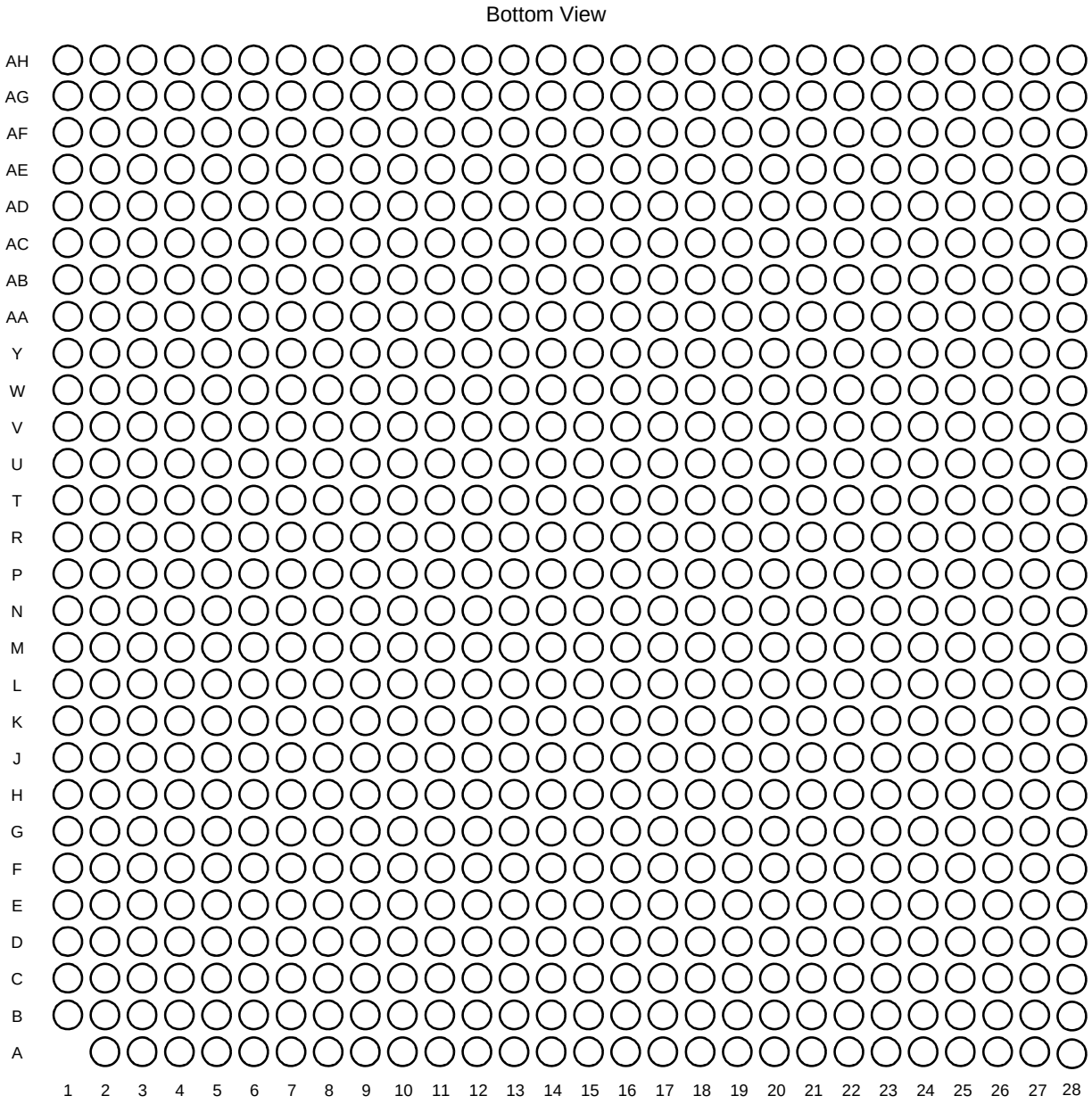

Figure 4. MSC8144 FC-PBGA Package, Bottom View

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. The functionality of multi-functional (multiplexed) pins is separated for each mode. When designing a board, make sure that the reference supply for each signal is appropriately considered. The specified reference supply must be tied to the voltage level specified in this document if any of the related signal functions are used (active).

Table 1. Signal List by Ball Number

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
A2	GND										GND
A3	GE2_RX_ER/PCI_AD31		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A4	V_{DDGE2}										V_{DDGE2}
A5	GE2_RX_DV/PCI_AD30		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A6	GE2_TD0/$\overline{\text{PCI\_CBE0}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
A7	SRIO_IMP_CAL_RX										V_{DDSXC}
A8	Reserved[1]										—
A9	Reserved[1]										—
A10	Reserved[1]										—
A11	Reserved[1]										—
A12	SRIO_RXD0										V_{DDSXC}
A13	V_{DDSXC}										V_{DDSXC}
A14	SRIO_RXD1										V_{DDSXC}
A15	V_{DDSXC}										V_{DDSXC}
A16	$\overline{\text{SRIO\_REF\_CLK}}$										V_{DDSXC}
A17	$V_{DDRIOPLL}$										GND_{RIOPLL}
A18	GND_{SXC}										GND_{SXC}
A19	SRIO_RXD2/ GE1_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A20	V_{DDSXC}										V_{DDSXC}
A21	SRIO_RXD3/ GE2_SGMII_RX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXC}
A22	V_{DDSXC}										V_{DDSXC}
A23	SRIO_IMP_CAL_TX										V_{DDSXP}
A24	MDQ28										V_{DDDDR}
A25	MDQ29										V_{DDDDR}
A26	MDQ30										V_{DDDDR}
A27	MDQ31										V_{DDDDR}
A28	$\overline{\text{MDQS3}}$										V_{DDDDR}
B1	Reserved[1]										—
B2	GE2_TD1/$\overline{\text{PCI\_CBE1}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B3	GE2_TX_EN/$\overline{\text{PCI\_CBE2}}$		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
B4	GE_MDIO		Ethernet								V_{DDGE2}
B5	GND										GND
B6	GE_MDC		Ethernet								V_{DDGE2}
B7	GND_{SXC}										GND_{SXC}
B8	Reserved[1]										—
B9	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
K23	MBA2										V_{DDDDR}
K24	MA10										V_{DDDDR}
K25	MA12										V_{DDDDR}
K26	MA14										V_{DDDDR}
K27	MA4										V_{DDDDR}
K28	MV_{REF}										V_{DDDDR}
L1	Reserved[1]										—
L2	CLKOUT										V_{DDIO}
L3	TMR1/UTP_IR/$\overline{\text{PCI\_CBE3}}$/ GPIO17[3, 6]		UTOPIA		TMR/ GPIO	UTOPIA	PCI	UTOPIA			V_{DDIO}
L4	TMR4/PCI_PAR/GPIO20[3, 6]/ UTP_REOP		TIMER/GPIO				PCI	TIMER/GPIO			V_{DDIO}
L5	GND										GND
L6	TMR2/$\overline{\text{PCI\_FRAME}}$/ GPIO18[3, 6]		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
L7	SCL/GPIO26[3, 4, 6]		I^2C/GPIO								V_{DDIO}
L8	UTXD/GPIO15/$\overline{\text{IRQ9}}$[3, 6]		UART/GPIO/IRQ								V_{DDIO}
L9	GND										GND
L10	V_{DD}										V_{DD}
L11	GND										GND
L12	V_{DD}										V_{DD}
L13	GND										GND
L14	V_{DD}										V_{DD}
L15	Reserved[1]										GND
L16	V_{DD}										V_{DD}
L17	GND										GND
L18	V_{DD}										V_{DD}
L19	GND										GND
L20	V_{DD}										V_{DD}
L21	GND										GND
L22	GND										GND
L23	MCKE1										V_{DDDDR}
L24	MA1										V_{DDDDR}
L25	V_{DDDDR}										V_{DDDDR}
L26	GND										GND
L27	V_{DDDDR}										V_{DDDDR}
L28	$\overline{\text{MCK1}}$										V_{DDDDR}
M1	Reserved[1]										—
M2	$\overline{\text{TRST}}$										V_{DDIO}
M3	EE0										V_{DDIO}
M4	EE1										V_{DDIO}
M5	UTP_RCLK/PCI_AD13		UTOPIA		PCI	UTOPIA					V_{DDIO}
M6	UTP_RADDR0/PCI_AD7		UTOPIA		PCI	UTOPIA					V_{DDIO}
M7	UTP_TD8/PCI_AD30		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
M8	V_{DDIO}										V_{DDIO}
M9	V_{DD}										V_{DD}
M10	GND										GND
M11	V_{DD}										V_{DD}
M12	GND										GND
M13	V_{DD}										V_{DD}
M14	GND										GND
M15	V_{DD}										V_{DD}
M16	GND										GND
M17	V_{DD}										V_{DD}
M18	GND										GND
M19	V_{DD}										V_{DD}
M20	GND										GND
M21	V_{DD}										V_{DD}
M22	V_{DDDDR}										V_{DDDDR}
M23	$\overline{MCS1}$										V_{DDDDR}
M24	MA13										V_{DDDDR}
M25	MA2										V_{DDDDR}
M26	MA0										V_{DDDDR}
M27	GND										GND
M28	MCK1										V_{DDDDR}
N1	Reserved[1]										—
N2	V_{DDIO}										V_{DDIO}
N3	TMS										V_{DDIO}
N4	UTP_RD10/PCI_AD14[5]		UTOPIA		PCI	UTOPIA					V_{DDIO}
N5	V_{DDIO}		Power								V_{DDIO}
N6	UTP_RADDR1/PCI_AD8		UTOPIA		PCI	UTOPIA					V_{DDIO}
N7	UTP_TD9/PCI_AD31		UTOPIA		PCI	UTOPIA					V_{DDIO}
N8	TMR3/$\overline{PCI\_IRDY}$/GPIO19[3,6]/ UTP_TEOP		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V_{DDIO}
N9	GND										GND
N10	V_{DDM3}										V_{DDM3}
N11	V_{DD}										V_{DD}
N12	V_{DDM3}										V_{DDM3}
N13	V_{DD}										V_{DD}
N14	V_{DDM3}										V_{DDM3}
N15	V_{DD}										V_{DD}
N16	V_{DDM3}										V_{DDM3}
N17	V_{DD}										V_{DD}
N18	V_{DDM3}										V_{DDM3}
N19	V_{DD}										V_{DD}
N20	V_{DDM3}										V_{DDM3}
N21	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
N22	GND										GND
N23	MODT1										V_{DDDDR}
N24	MCKE0										V_{DDDDR}
N25	V_{DDDDR}										V_{DDDDR}
N26	MA5										V_{DDDDR}
N27	MA6										V_{DDDDR}
N28	MA11										V_{DDDDR}
P1	Reserved[1]										—
P2	TDI[5]										V_{DDIO}
P3	UTP_RD11/PCI_AD15		UTOPIA		PCI	UTOPIA					V_{DDIO}
P4	GND										GND
P5	UTP_RADDR3/PCI_AD10		UTOPIA		PCI	UTOPIA					V_{DDIO}
P6	UTP_RADDR2/PCI_AD9		UTOPIA		PCI	UTOPIA					V_{DDIO}
P7	$\overline{\text{PCI\_GNT}}$/GPIO29/$\overline{\text{IRQ7}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
P8	$\overline{\text{PCI\_STOP}}$/GPIO30/$\overline{\text{IRQ2}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
P9	GND										GND
P10	GND										GND
P11	V_{DDM3}										V_{DDM3}
P12	GND										GND
P13	V_{DDM3}										V_{DDM3}
P14	GND										GND
P15	V_{DDM3}										V_{DDM3}
P16	GND										GND
P17	V_{DDM3}										V_{DDM3}
P18	GND										GND
P19	V_{DDM3}										V_{DDM3}
P20	GND										GND
P21	GND										GND
P22	V_{DDDDR}										V_{DDDDR}
P23	$\overline{\text{MCS0}}$										V_{DDDDR}
P24	$\overline{\text{MRAS}}$										V_{DDDDR}
P25	GND										GND
P26	V_{DDDDR}										V_{DDDDR}
P27	GND										GND
P28	$\overline{\text{MCK2}}$										V_{DDDDR}
R1	Reserved[1]										—
R2	TCK										V_{DDIO}
R3	TDO										V_{DDIO}
R4	UTP_RD12/PCI_AD16		UTOPIA		PCI	UTOPIA					V_{DDIO}
R5	UTP_RCLAV_PDRPA/ PCI_AD12		UTOPIA		PCI	UTOPIA					V_{DDIO}
R6	UTP_RADDR4/PCI_AD11		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
R7	V_{DDIO}										V_{DDIO}
R8	$\overline{\text{PCI\_REQ}}$		PCI								V_{DDIO}
R9	GND										GND
R10	GND										GND
R11	GND										GND
R12	GND										GND
R13	GND										GND
R14	GND										GND
R15	GND										GND
R16	GND										GND
R17	GND										GND
R18	GND										GND
R19	GND										GND
R20	GND										GND
R21	GND										GND
R22	GND										GND
R23	MODT0										V_{DDDDR}
R24	MDIC1										V_{DDDDR}
R25	MDIC0										V_{DDDDR}
R26	$\overline{\text{MCAS}}$										V_{DDDDR}
R27	$\overline{\text{MWE}}$										V_{DDDDR}
R28	MCK2										V_{DDDDR}
T1	Reserved[1]										—
T2	UTP_RPRTY/PCI_AD21		UTOPIA		PCI	UTOPIA					V_{DDIO}
T3	UTP_RD13/PCI_AD17		UTOPIA		PCI	UTOPIA					V_{DDIO}
T4	V_{DDIO}										V_{DDIO}
T5	UTP_RD14/PCI_AD18		UTOPIA		PCI	UTOPIA					V_{DDIO}
T6	UTP_RD15/PCI_AD19		UTOPIA		PCI	UTOPIA					V_{DDIO}
T7	$\overline{\text{PCI\_TRDY}}$		PCI								V_{DDIO}
T8	$\overline{\text{PCI\_DEVSEL}}$/GPIO31/ $\overline{\text{IRQ3}}$[3, 6]		GPIO/IRQ		PCI			GPIO/IRQ			V_{DDIO}
T9	GND										GND
T10	GND										GND
T11	GND										GND
T12	GND										GND
T13	GND										GND
T14	GND										GND
T15	GND										GND
T16	GND										GND
T17	GND										GND
T18	GND										GND
T19	GND										GND
T20	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
T21	GND										GND
T22	V_{DDDDR}										V_{DDDDR}
T23	GND										GND
T24	V_{DDDDR}										V_{DDDDR}
T25	GND										GND
T26	V_{DDDDR}										V_{DDDDR}
T27	GND										GND
T28	V_{DDDDR}										V_{DDDDR}
U1	Reserved[1]										—
U2	UTP_TCLK/PCI_AD29		UTOPIA		PCI	UTOPIA					V_{DDIO}
U3	UTP_TADDR4/PCI_AD27		UTOPIA		PCI	UTOPIA					V_{DDIO}
U4	UTP_TADDR2		UTOPIA								V_{DDIO}
U5	GND										GND
U6	$\overline{\text{UTP\_REN}}$/PCI_AD20		UTOPIA		PCI	UTOPIA					V_{DDIO}
U7	PCI_AD26		PCI								V_{DDIO}
U8	PCI_AD25		PCI								V_{DDIO}
U9	Reserved[1]										V_{DDIO}
U10	V_{DDM3}										V_{DDM3}
U11	GND										GND
U12	V_{DDM3}										V_{DDM3}
U13	GND										GND
U14	V_{DDM3}										V_{DDM3}
U15	GND										GND
U16	V_{DDM3}										V_{DDM3}
U17	GND										GND
U18	V_{DDM3}										V_{DDM3}
U19	GND										GND
U20	V_{DDM3}										V_{DDM3}
U21	GND										GND
U22	GND										GND
U23	MDQ7										V_{DDDDR}
U24	MDQ3										V_{DDDDR}
U25	MDQ4										V_{DDDDR}
U26	MDQ5										V_{DDDDR}
U27	MDQ1										V_{DDDDR}
U28	MDQ0										V_{DDDDR}
V1	Reserved[1]										—
V2	UTP_TD10/$\overline{\text{PCI\_CBE0}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
V3	UTP_TADDR3		UTOPIA								V_{DDIO}
V4	UTP_TD1/$\overline{\text{PCI\_PERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
V5	UTP_TADDR0/PCI_AD23		UTOPIA		PCI	UTOPIA					V_{DDIO}
V6	UTP_TADDR1/PCI_AD24		UTOPIA		PCI	UTOPIA					V_{DDIO}
V7	UTP_TCLAV/PCI_AD28		UTOPIA		PCI	UTOPIA					V_{DDIO}

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8144 Reference Manual*.

2.1 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{DD}).

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8144.

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Core supply voltage	V_{dd}	–0.3 to 1.1	V
PLL supply voltage[3]	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1	V
M3 memory Internal voltage	V_{DDM3}	–0.3 to 1.32	V
DDR memory supply voltage • DDR mode • DDR2 mode	V_{DDDDR}	 –0.3 to 2.75 –0.3 to 1.98	 V V
DDR reference voltage	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage	V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
Ethernet 1 I/O voltage	V_{DDGE1}	–0.3 to 3.465	V
Input Ethernet 1 I/O voltage	V_{INGE1}	–0.3 to V_{DDGE1} + 0.3	V
Ethernet 2 I/O voltage	V_{DDGE2}	–0.3 to 3.465	V
Input Ethernet 2I/O voltage	V_{INGE2}	–0.3 to V_{DDGE2} + 0.3	V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	–0.3 to 3.465	V
Input I/O voltage	V_{INIO}	–0.3 to V_{DDIO} + 0.3	V

Table 2. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
M3 memory I/O and M3 memory charge pump voltage	V_{DDM3IO} V_{25M3}	–0.3 to 2.75	V
Input M3 memory I/O voltage	V_{INM3IO}	–0.3 to V_{DDM3IO} + 0.3	V
Rapid I/O C voltage	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O P voltage	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	–0.3 to 1.21	V
Operating temperature	T_J	–40 to 105	°C
Storage temperature range	T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8144 (see Figure 43)

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage • 800 MHz (VT, SVT, TVT) and 1000 MHz (VT) • 1000 MHz (SVT, TVT)	V_{DD}	 0.97 0.97	 1.0 1.0	 1.05 1.03	 V V
PLL supply voltage • 800 MHz (VT, SVT, TVT) and 1000 MHz (VT) • 1000 MHz (SVT, TVT)	V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	 0.97 0.97	 1.0 1.0	 1.05 1.03	 V V
M3 memory Internal voltage	V_{DDM3}	1.213	1.25	1.313	V
DDR memory supply voltage • DDR mode • DDR2 mode DDR reference voltage	V_{DDDDR} MV_{REF}	 2.375 1.71 0.49 × V_{DDDDR} (nom)	 2.5 1.8 0.5 × V_{DDDDR} (nom)	 2.625 1.89 0.51 × V_{DDDDR} (nom)	 V V V
Ethernet 1 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE1}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
Ethernet 2 I/O voltage • 2.5 V mode • 3.3 V mode	V_{DDGE2}	 2.375 3.135	 2.5 3.3	 2.625 3.465	 V V
I/O voltage excluding Ethernet, DDR, M3, and RapidIO lines	V_{DDIO}	3.135	3.3	3.465	V
M3 memory I/O and M3 charge pump voltage	V_{DDM3IO} V_{25M3}	2.375	2.5	2.625	V
Rapid I/O C voltage	V_{DDSXC}	0.97	1.0	1.05	V
Rapid I/O P voltage • Short run (haul) mode • Long run (haul) mode	V_{DDSXP}	 0.97 1.14	 1.0 1.2	 1.05 1.26	 V V
Rapid I/O PLL voltage	$V_{DDRIOPLL}$	0.97	1.0	1.05	V
Operating temperature range: • Standard (VT) • Intermediate (SVT) • Extended (TVT)	 T_J T_J T_A T_J	 0 0 –40 —		 90 105 — 105	 °C °C °C °C

Note: PLL supply voltage is specified at input of the filter and not at pin of the MSC8144 (see Figure 43).

2.5.6 ATM/UTOPIA/POS DC Electrical Characteristics

Table 13. ATM/UTOPIA/POS DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.4 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –4 mA	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 4 mA	V_{OL}	—	0.5	V

Notes: **1.** Not tested. Guaranteed by design.

2.5.7 SPI DC Electrical Characteristics

Table 14 provides the SPI DC electrical characteristics.

Table 14. SPI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}		30	µA
Output high voltage, I_{OH} = –4.0 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 4.0 mA	V_{OL}	—	0.5	V

2.5.8 GPIO, UART, TIMER, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, JTAG Ports DC Electrical Characteristics

Table 15. GPIO, UART, Timer, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, and JTAG Port[1] DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current, V_{IN} = supply voltage	I_{OZ}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[2]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–30	30	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0.4	V

Notes: **1.** This does not include TDI and TMS, which have internal pullup resistors.
2. Not tested. Guaranteed by design.

2.6.4.2 DDR SDRAM Output AC Timing Specifications

Table 23 provides the output AC timing specifications for the DDR SDRAM interface.

Table 23. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit
MCK[n] cycle time, (MCK[n]/$\overline{\text{MCK}}$[n] crossing)[2]	t_{MCK}	5	10	ns
ADDR/CMD output setup with respect to MCK[3]	t_{DDKHAS}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
ADDR/CMD output hold with respect to MCK[3]	t_{DDKHAX}			
• 400 MHz		1.85	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
$\overline{\text{MCS}}$n output setup with respect to MCK[3]	t_{DDKHCS}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
$\overline{\text{MCS}}$n output hold with respect to MCK[3]	t_{DDKHCX}			
• 400 MHz		1.95	—	ns
• 333 MHz		2.40	—	ns
• 266 MHz		3.15	—	ns
• 200 MHz		4.20	—	ns
MCK to MDQS Skew[4]	t_{DDKHMH}	–0.6	0.6	ns
MDQ/MECC/MDM output setup with respect to MDQS[5]	t_{DDKHDS}, t_{DDKLDS}			
• 400 MHz		700	—	ps
• 333 MHz		900	—	ps
• 266 MHz		1100	—	ps
• 200 MHz		1200	—	ps
MDQ/MECC/MDM output hold with respect to MDQS[5]	t_{DDKHDX}, t_{DDKLDX}			
• 400 MHz		700	—	ps
• 333 MHz		900	—	ps
• 266 MHz		1100	—	ps
• 200 MHz		1200	—	ps
MDQS preamble start[6]	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns
MDQS epilogue end[6]	t_{DDKHME}	–0.6	0.6	ns

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MSC8144 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) ± 5%.

Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD and $\overline{RD}$ each have a peak-to-peak voltage (V_{PP}) swing of A – B.
2. The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD} - V_{\overline{TD}}$.
3. The differential input signal of the receiver, V_{ID}, is defined as $V_{RD} - V_{\overline{RD}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B).
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B.
6. The value of the differential transmitter output signal and the differential receiver input signal is $2 \times (A - B)$ V_{PP}.

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV_{PP}. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV_{PP}.

Note: AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described. The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of **IEEE™** Std 802.3ae-2002™. XAUI has similar application goals to serial RapidIO. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

2.6.5.3 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

2.6.5.4 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section. The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (baud frequency)/10 < freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ freq(f) ≤ baud frequency

The reference impedance for the differential return loss measurements is 100 Ω resistive. Differential return loss includes contributions from internal circuitry, packaging, and any external components related to the driver. The output impedance requirement applies to all valid output levels. It is recommended that the 20–80% rise/fall time of the transmitter, as measured at the transmitter output, have a minimum value 60 ps in each case. It is also recommended that the timing skew at the output of an LP-Serial transmitter between the two signals comprising a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB, and 15 ps at 3.125 GB.

Table 25. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	

Table 25. Short Run Transmitter AC Timing Specifications—1.25 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

Table 26. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	–0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple Output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 27. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

Table 28. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	±100 ppm

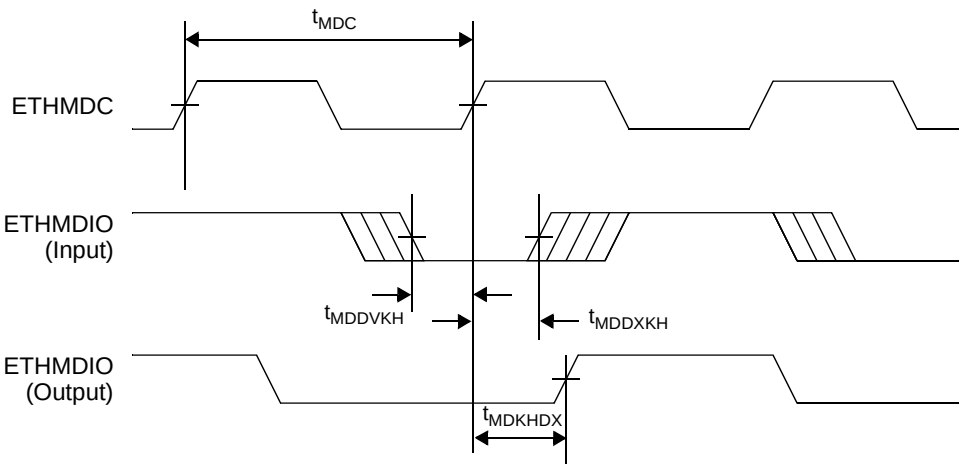

Figure 24. MII Management Interface Timing

2.6.10.2 MII Transmit AC Timing Specifications

Table 41 provides the MII transmit AC timing specifications.

Table 41. MII Transmit AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Max	Unit
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	25	ns

Notes: **1.** Typical TX_CLK period (t_{MTX}) for 10 Mbps is 400 ns and for 100 Mbps is 40 ns.
2. Program GCR4 as 0x00030CC3.

Figure 25 shows the MII transmit AC timing diagram.

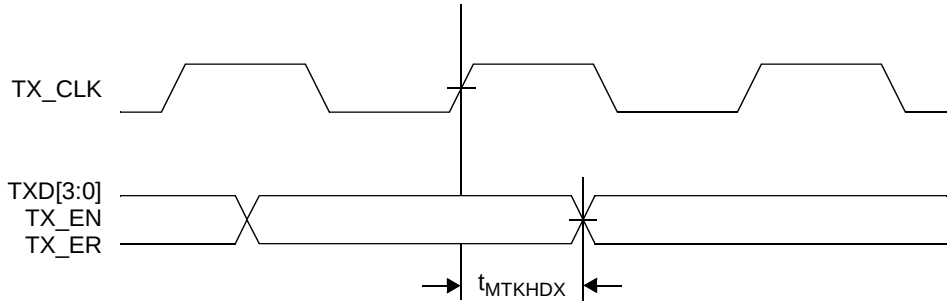

Figure 25. MII Transmit AC Timing

2.6.10.3 MII Receive AC Timing Specifications

Table 42 provides the MII receive AC timing specifications.

Table 42. MII Receive AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Max	Unit
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	2	—	ns

Notes: **1.** Typical RX_CLK period (t_{MRX}) for 10 Mbps is 400 ns and for 100 Mbps is 40 ns.
2. Program GCR4 as 0x00030CC3.

2.6.11 ATM/UTOPIA/POS Timing

Table 47 provides the ATM/UTOPIA/POS input and output AC timing specifications.

Table 47. ATM/UTOPIA/POS AC Timing (External Clock) Specifications

Characteristic	Symbol	Min	Max	Unit
Outputs—External clock delay	t_{UEKHOV}	1	9	ns
Outputs—External clock High Impedance[1]	t_{UEKHOX}	1	9	ns
Inputs—External clock input setup time	t_{UEIVKH}	4		ns
Inputs—External clock input hold time	t_{UEIXKH}	1		ns

Notes:
1. Not tested. Guaranteed by design.
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. Although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 32 provides the AC test load for the ATM/UTOPIA/POS.

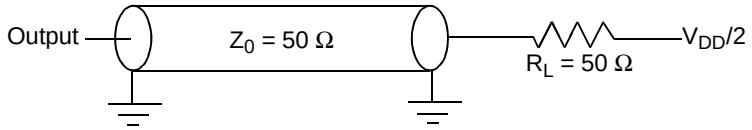

Figure 32. ATM/UTOPIA/POS AC Test Load

Figure 33 shows the ATM/UTOPIA/UTOPIA timing with external clock.

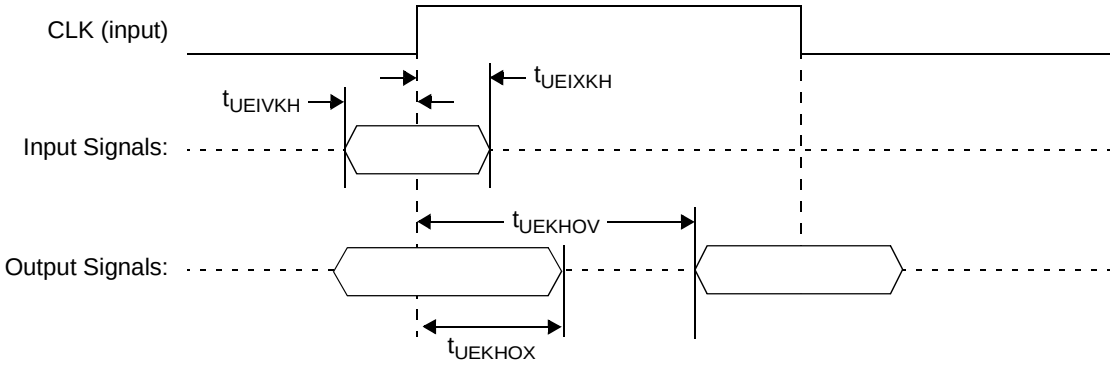

Figure 33. ATM/UTOPIAPOS AC Timing (External Clock)

Table 52. Connectivity of DDR Related Pins When Using 16-bit DDR Memory Only (continued)

Signal Name	Pin connection
$\overline{\text{MWE}}$	in use
MV_{REF}	$1/2*V_{DDDDR}$
V_{DDDDR}	2.5 V or 1.8 V

3.4.1.3 ECC Unused Pin Connections

When the error code corrected mechanism is not used in any 32- or 16-bit DDR configuration, refer to Table 53 to determine the correct pin connections.

Table 53. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[0–7]	pull-up to V_{DDDDR}
ECC_MDM	NC
ECC_MDQS	pull-down to GND
$\overline{\text{ECC\_MDQS}}$	pull-up to V_{DDDDR}

3.4.2 Serial RapidIO Interface Related Pins

3.4.2.1 Serial RapidIO interface Is Not Used

Table 54. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	GND
SRIO_IMP_CAL_TX	GND
$\overline{\text{SRIO\_REF\_CLK}}$	GND
SRIO_REF_CLK	GND
SRIO_RXD[0–3]	GND
$\overline{\text{SRIO\_RXD[0–3]}}$	GND
$\overline{\text{SRIO\_TXD[0–3]}}$	NC
SRIO_TXD[0–3]	NC
$V_{DDRIOPLL}$	GND
GND_{RIOPLL}	GND
GND_{SXP}	GND
GND_{SXC}	GND
V_{DDSXP}	GND
V_{DDSXC}	GND

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	NC
GE2_TD[0–3]	NC
GE2_TX_EN	NC

3.4.4.3 GE1 and GE2 Management Pins

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used (that is, V_{DDGE2} is connected to GND), Table 61 lists the recommended management pin connections.

Table 61. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

3.4.5 UTOPIA/POS Related Pins

Table 62 lists the board connections of the UTOPIA/POS pins when the entire UTOPIA/POS interface is not used or subset of UTOPIA/POS interface is used. For multiplexing options that select a subset of the UTOPIA/POS interface, use the connections described in Table 62 for those signals that are not selected. Table 62 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 62. Connectivity of UTOPIA/POS Related Pins When UTOPIA/POS Interface Is Not Used

Signal Name	Pin Connection
UTP_IR	GND
UTP_RADDR[0–4]	V_{DDIO}
UTP_RCLAV_PDRPA	NC
UTP_RCLK	GND
UTP_RD[0–15]	GND
$\overline{\text{UTP\_REN}}$	V_{DDIO}
UTP_RPRTY	GND
UTP_RSOC	GND
UTP_TADDR[0–4]	V_{DDIO}
UTP_TCLAV	NC
UTP_TCLK	GND
UTP_TD[0–15]	NC
$\overline{\text{UTP\_TEN}}$	V_{DDIO}
UTP_TPRTY	NC
UTP_TSOC	NC
V_{DDIO}	3.3 V

3.4.8 Miscellaneous Pins

Table 65 lists the board connections for the pins if they are not required by the system design. Table 65 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 65. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[0–31]	GND
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ}}$[0–15]	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[0–16]	GND
$\overline{\text{RC\_LDF}}$	NC
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[0–4]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	GND
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
V_{DDIO}	3.3 V
Note: When using I/O multiplexing mode 5 or 6, tie the TDM7TSYN/PCI_AD4 signal (ball number AC9) to GND.	

Note: For details on configuration, see the *MSC8144 Reference Manual*. For additional information, refer to the *MSC8144 Design Checklist* (AN3202).

7 Revision History

Table 66 provides a revision history for this data sheet.

Table 66. Document Revision History

Rev.	Date	Description
0	Feb. 2007	• Initial public release.
1	Apr. 2007	• Adds new I/O multiplexing mode 7 that supports POS functionality. • Updates reference voltage supply for pins G5, H7, and H8 in Table 1. • Updates start-up timing recommendations with regard to $\overline{\text{TRST}}$ and $\overline{\text{M3\_RESET}}$ in Section 2.7.1. • Adds input clock duty cycles in Table 20. • Updates PCI AC timings in Table 41. • Removes UTOPIA internal clock specifications in Table 52. • Updates JTAG timings in Table 56. • Clarifies connectivity guidelines for Ethernet pins in Section 3.3.4. • Miscellaneous pin connectivity guidelines were updated in Table 71. • Updates name of core subsystem reference manual.
2	June 2007	• Corrected AA4 definition in Table 1. Changed TDM5TD3 to correct name TDM5TDAT. • Removed Figure 35 because the device does not support UTOPIA using an internal clock. Renumbered subsequent figures. • Removed Section 3.5 *Thermal Considerations*. To be replaced with an application note.
3	Sep 2007	• Updated M3 voltage range in Table 3. • Changed note in Table 7 for PLL power supplies. • DDR voltage designator changed from V_{DD} to V_{DDDDR} in Table 8, Table 10, **Section 2.7.4.1**, **Section 2.7.4.2**, and Figure 11. Changed range on I_{OZ} in Table 8 and Table 10. • Deleted text before Table 13 and added note 2 to input pin capacitance. • Deleted text before Table 14, added a 1 to the note, and added note 1 to input pin capacitance. • Deleted **Section 2.6.5** on page 32 and renumbered subsequent subsections. • Deleted text before new **Section 2.6.5.1**. • Added a 1 to the note in Table 15 and added note 1 to input pin capacitance. • Deleted ac voltage rows from Table 16. Added note 1 to input pin capacitance. • Changed output high and low voltage levels in Table 17 and Table 18. • Deleted text before Table 19. • Added clock skew ranges in percent in Table 21. • Changed V_{REF} to MV_{REF} in Table 26. • Changed V_{DD} to V_{DDIO} in Table 41 Updated note 2. • Added note 4 to Table 42. Changed $t_{TDMSHOX}$ value. • Changed V_{DD} to V_{DDGE} in Figure 27 and Figure 30. • Changed the value of the data to clock out skew in Table 51. • Changed EE pin timing in Table 55. • Changed the head for the JTAG timing section, now **Section 2.7.15**. • Updated JTAG timing for TCK cycle time, TCK high phase, and boundary scan input data hold time in Table 56. • Added new **Section 3.3** with guidelines for board layout for clock and timing signals. Renumbered subsequent sections.
4	Sep 2007	• Changed leakage current values in Table 13, Table 14, Table 11, Table 16, Table 17, Table 18, and Table 19 from –10 and 10 µa to –30 and 30 µa. • Change the minimum value of t_{MDDVKH} in Table 45 from 5 ns to 7 ns. • Updated note 1 in Table 45.
5	Oct 2007	• Corrected column numbering in Figure 3 and Figure 4. • Updated SPI signal names in Table 1.
6	Oct 2007	• Updated SPI signal names in Table 1.