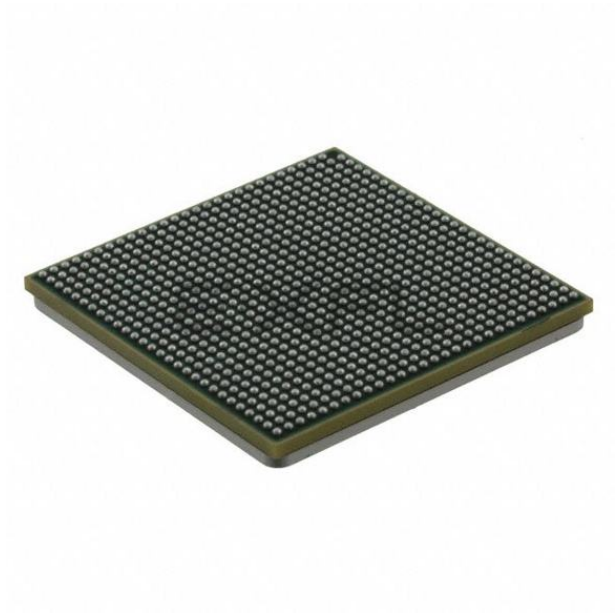

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	Ethernet, I²C, SPI, TDM, UART, UTOPIA
Clock Rate	1GHz
Non-Volatile Memory	External
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8144tvt1000b

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
C21	V_{DDSXP}										V_{DDSXP}
C22	$\overline{SRIO\_TXD3}$/GE2_SGMII_$\overline{TX}$		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
C23	V_{DDSXP}										V_{DDSXP}
C24	MDQ26										V_{DDDDR}
C25	MDQ25										V_{DDDDR}
C26	MDM3										V_{DDDDR}
C27	GND										GND
C28	MDQ24										V_{DDDDR}
D1	Reserved[1]										—
D2	GE2_RD1/PCI_AD28		Ethernet 2				PCI	Ethernet 2			V_{DDGE2}
D3	GND										GND
D4	TDM7TDAT/GE2_TD3/ PCI_AD3/UTP_TMD		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D5	TDM7RDAT/GE2_RD3/ PCI_AD1/UTP_STA		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D6	$\overline{GE1\_RD0}$/UTP_RD2/ $\overline{PCI\_CBE2}$		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
D7	TDM7TCLK/GE2_TCK/ PCI_IDS/UTP_RER		TDM		PCI			Ethernet 2		UTOPIA	V_{DDGE2}
D8	Reserved[1]										—
D9	Reserved[1]										—
D10	Reserved[1]										—
D11	Reserved[1]										—
D12	GND_{SXP}										GND_{SXP}
D13	SRIO_TXD0										V_{DDSXP}
D14	GND_{SXP}										GND_{SXP}
D15	SRIO_TXD1										V_{DDSXP}
D16	V_{DDSXC}										V_{DDSXC}
D17	Reserved[1]										—
D18	Reserved[1]										—
D19	GND_{SXP}										GND_{SXP}
D20	SRIO_TXD2/GE1_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D21	GND_{SXP}										GND_{SXP}
D22	SRIO_TXD3/GE2_SGMII_TX		SGMII support on SERDES is enabled by Reset Configuration Word								V_{DDSXP}
D23	GND_{SXP}										GND_{SXP}
D24	MDQ23										V_{DDDDR}
D25	V_{DDDDR}										V_{DDDDR}
D26	MDQ22										V_{DDDDR}
D27	MDQ21										V_{DDDDR}
D28	$\overline{MDQS2}$										V_{DDDDR}
E1	Reserved[1]										—

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E6	V_{DDGE1}										V_{DDGE1}
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
E8	Reserved[1]										—
E9	Reserved[1]										—
E10	GND										GND
E11	V_{DD}										V_{DD}
E12	GND										GND
E13	V_{DD}										V_{DD}
E14	GND										GND
E15	V_{DD}										V_{DD}
E16	GND										GND
E17	V_{DD}										V_{DD}
E18	GND										GND
E19	V_{DD}										V_{DD}
E20	GND										GND
E21	V_{DD}										V_{DD}
E22	GND										GND
E23	V_{DDDDR}										V_{DDDDR}
E24	MDQ20										V_{DDDDR}
E25	GND										GND
E26	V_{DDDDR}										V_{DDDDR}
E27	GND										GND
E28	MDQS2										V_{DDDDR}
F1	Reserved[1]										—
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F3	V_{DDGE1}										V_{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F6	GND										GND
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V_{DDGE1}
F8	V_{DDGE1}										V_{DDGE1}
F9	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
G23	MBA1										V_{DDDDR}
G24	MA3										V_{DDDDR}
G25	MA8										V_{DDDDR}
G26	V_{DDDDR}										V_{DDDDR}
G27	GND										GND
G28	$\overline{\text{MCK0}}$										V_{DDDDR}
H1	Reserved[1]										—
H2	CLKIN										V_{DDIO}
H3	$\overline{\text{HRESET}}$										V_{DDIO}
H4	PCI_CLK_IN										V_{DDIO}
H5	$\overline{\text{NMI}}$										V_{DDIO}
H6	URXD/GPIO14/$\overline{\text{IRQ8}}$/ $\overline{\text{RC\_LDF}}$[3, 6]	$\overline{\text{RC\_LDF}}$	UART/GPIO/IRQ								V_{DDIO}
H7	GE1_RX_ER/PCI_AD6/ GPIO25/$\overline{\text{IRQ15}}$[3, 6]		GPIO/ IRQ	Ethernet 1	PCI			GPIO/ IRQ	Ethernet 1		V_{DDIO}
H8	GE1_CRS/PCI_AD5		PCI	Ethernet 1	PCI				Ethernet 1		V_{DDIO}
H9	GND										GND
H10	V_{DD}										V_{DD}
H11	GND										GND
H12	V_{DD}										V_{DD}
H13	GND										GND
H14	V_{DD}										V_{DD}
H15	V_{DD}										V_{DD}
H16	V_{DD}										V_{DD}
H17	GND										GND
H18	V_{DD}										V_{DD}
H19	GND										GND
H20	V_{DD}										V_{DD}
H21	V_{DD}										V_{DD}
H22	V_{DDDDR}										V_{DDDDR}
H23	MBA0										V_{DDDDR}
H24	MA15										V_{DDDDR}
H25	V_{DDDDR}										V_{DDDDR}
H26	MA9										V_{DDDDR}
H27	MA7										V_{DDDDR}
H28	MCK0										V_{DDDDR}
J1	Reserved[1]										—
J2	GND										GND
J3	V_{DDIO}										V_{DDIO}
J4	STOP_BS										V_{DDIO}
J5	$\overline{\text{NMI\_OUT}}$[4]										V_{DDIO}
J6	$\overline{\text{INT\_OUT}}$[4]										V_{DDIO}
J7	SDA/GPIO27[3, 4, 6]		I2C/GPIO								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
W23	MDQ10										V_{DDDDR}
W24	GND										GND
W25	MDQ11										V_{DDDDR}
W26	MDM0										V_{DDDDR}
W27	GND										GND
W28	$\overline{\text{MDQS0}}$										V_{DDDDR}
Y1	Reserved[1]										-
Y2	UTP_TD14/$\overline{\text{PCI\_FRAME}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
Y3	TDM5TSYN/PCI_AD18/ GPIO12[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
Y4	TDM5TCLK/PCI_AD16		TDM			PCI		TDM			V_{DDIO}
Y5	TDM4RCLK/PCI_AD7		TDM			PCI		TDM			V_{DDIO}
Y6	TDM4TSYN/PCI_AD12		TDM			PCI		TDM			V_{DDIO}
Y7	UTP_TPRTY/RC14	RC14	UTOPIA								V_{DDIO}
Y8	$\overline{\text{UTP\_TEN}}$/PCI_PAR		UTOPIA		PCI	UTOPIA					V_{DDIO}
Y9	Reserved[1]										V_{DDIO}
Y10	GND										GND
Y11	V_{DDM3}										V_{DDM3}
Y12	GND										GND
Y13	V_{DDM3}										V_{DDM3}
Y14	GND										GND
Y15	V_{DDM3}										V_{DDM3}
Y16	GND										GND
Y17	V_{DDM3}										V_{DDM3}
Y18	GND										GND
Y19	V_{DDM3}										V_{DDM3}
Y20	GND										GND
Y21	GND										GND
Y22	V_{DDDDR}										V_{DDDDR}
Y23	MDQ13										V_{DDDDR}
Y24	V_{DDDDR}										V_{DDDDR}
Y25	GND										GND
Y26	MDQ9										V_{DDDDR}
Y27	V_{DDDDR}										V_{DDDDR}
Y28	MDQ8										V_{DDDDR}
AA1	Reserved[1]										—
AA2	UTP_TD13/$\overline{\text{PCI\_CBE3}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
AA3	TDM5RSYN/PCI_AD15/ GPIO10[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AA4	TDM5TDAT, AT/PCI_AD17/ GPIO11[6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AA5	TDM5RCLK/PCI_AD13/ GPIO28[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AA6	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AA7	TDM4TCLK/PCI_AD10		TDM			PCI		TDM			V_{DDIO}
AA8	TDM4TDAT/PCI_AD11		TDM			PCI		TDM			V_{DDIO}
AA9	V_{DDIO}										V_{DDIO}
AA10	V_{DDM3}										V_{DDM3}
AA11	GND										GND
AA12	V_{DDM3}										V_{DDM3}
AA13	GND										GND
AA14	V_{DDM3}										V_{DDM3}
AA15	GND										GND
AA16	V_{DDM3}										V_{DDM3}
AA17	GND										GND
AA18	V_{DDM3}										V_{DDM3}
AA19	GND										GND
AA20	V_{DDM3}										V_{DDM3}
AA21	GND										GND
AA22	GND										GND
AA23	MDQ15										V_{DDDDR}
AA24	MDQ14										V_{DDDDR}
AA25	MDM1										V_{DDDDR}
AA26	MDQ12										V_{DDDDR}
AA27	$\overline{\text{MDQS1}}$										V_{DDDDR}
AA28	MDQS1										V_{DDDDR}
AB1	Reserved[1]										-
AB2	UTP_TSOC/RC15	RC15	UTOPIA								V_{DDIO}
AB3	V_{DDIO}										V_{DDIO}
AB4	TDM6RDAT/PCI_AD20/ GPIO5/$\overline{\text{IRQ11}}$[3, 6]		TDM/GPIO/ IRQ			PCI		TDM/GPIO/ IRQ			V_{DDIO}
AB5	TDM5RDAT/PCI_AD14/ GPIO9[3, 6]		TDM/GPIO			PCI		TDM/GPIO			V_{DDIO}
AB6	TDM6TSYN/PCI_AD24/ GPIO8/ $\overline{\text{IRQ14}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB7	TDM6RCLK/PCI_AD19/ GPIO4/$\overline{\text{IRQ10}}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AB8	TDM4RSYN/PCI_AD9		TDM			PCI		TDM			V_{DDIO}
AB9	TDM4RDAT/PCI_AD8		TDM			PCI		TDM			V_{DDIO}
AB10	GND										GND
AB11	V_{DDM3}										V_{DDM3}
AB12	GND										GND
AB13	V_{DDM3}										V_{DDM3}
AB14	GND										GND
AB15	V_{DDM3}										V_{DDM3}
AB16	GND										GND
AB17	V_{DDM3}										V_{DDM3}
AB18	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AH17	Reserved[1]										—
AH18	Reserved[1]										—
AH19	Reserved[1]										—
AH20	Reserved[1]										—
AH21	Reserved[1]										—
AH22	Reserved[1]										—
AH23	Reserved[1]										—
AH24	Reserved[1]										—
AH25	Reserved[1]										—
AH26	Reserved[1]										—
AH27	Reserved[1]										—
AH28	Reserved[1]										—

Notes:
1. Reserved signals should be disconnected for compatibility with future revisions of the device.
2. For signals with same functionality in all modes the appropriate cells are empty.
3. The choice between GPIO function and other function is by GPIO registers setup. For configuration details, see **Chapter 23,** *GPIO* in the *MSC8144 Reference Manual*.
4. Open-drain signal.
5. Internal 20 KΩ pull-up resistor.
6. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See **Chapter 23**, *GPIO* of the *MSC8144 Reference Manual* for configuration details.

2.5.2 Serial RapidIO DC Electrical Characteristics

DC receiver logic levels are not defined since the receiver is AC-coupled.

2.5.2.1 DC Requirements for SerDes Reference Clocks

The SerDes reference clocks SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$ are AC-coupled differential inputs. Each differential clock input has an internal 50 Ω termination to GND_{SXC}. The reference clock must be able to drive this termination. The recommended minimum operating voltage is –0.4 V; the recommended maximum operating voltage is 1.32 V; and the maximum absolute voltage is 1.72 V.

The maximum average current allowed in each input is 8 mA. This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 Ω = 8 mA) while the minimum common mode input level is GND_{SXC}. For example, a clock with a 50/50 duty cycle can be driven by a current source output that ranges from 0 mA to 16 mA (0–0.8 V). The input is AC-coupled internally, so, therefore, the exact common mode input voltage is not critical.

Note: This internal AC-couple network does not function correctly with reference clock frequencies below 90 MHz.

If the device driving the $\overline{\text{SRIO\_REF\_CLK}}$ inputs cannot drive 50 Ω to GND_{SXC}, or if it exceeds the maximum input current limitations, then it must use external AC-coupling. The minimum differential peak-to-peak amplitude of the input clock is 0.4 V (0.2 V peak-to-peak per phase). The maximum differential peak-to-peak amplitude of the input clock is 1.6 V peak-to-peak (see Figure 5. The termination to GND_{SXC} allows compatibility with HCSL type reference clocks specified for PCI-Express applications. Many other low voltage differential type outputs can be used but will probably need to be AC-coupled due to the limited common mode input range. LVPECL outputs can produce too large an amplitude and may need to be source terminated with a divider network to reduce the amplitude. The amplitude of the clock must be at least a 400 mV differential peak-peak for single-ended clock. If driven differentially, each signal wire needs to drive 100 mV around common mode voltage. The differential reference clock (SRIO_REF_CLK/ $\overline{\text{SRIO\_REF\_CLK}}$) input is HCSL-compatible DC coupled or LVDS-compatible with AC-coupling.

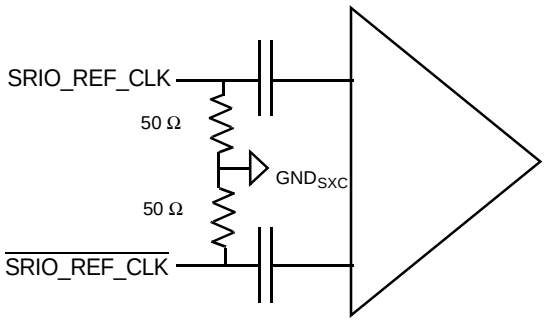


Figure 5. SerDes Reference Clocks Input Stage

2.5.2.2 Spread Spectrum Clock

SRIO_REF_CLK/ $\overline{\text{SRIO\_REF\_CLK}}$ is designed to work with a spread spectrum clock (0 to 0.5% spreading at 3033 kHz rate is allowed), assuming both ends have same reference clock. For better results use a source without significant unintended modulation.

2.5.3 PCI DC Electrical Characteristics

Table 9. PCI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDPCI}	3.135	3.465	V
Input high voltage	V_{IH}	$0.5 \times V_{DDPCI}$	3.465	V
Input low voltage	V_{IL}	–0.5	$0.3 \times V_{DDPCI}$	V
Input Pull-up voltage[1]	V_{IPU}	$0.7 \times V_{DDPCI}$		
Input leakage current, $0<V_{IN}<V_{DDPCI}$	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current, $0<V_{IN}<V_{DDPCI}$	I_{OZ}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.0 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –0.5 mA, except open drain pins	V_{OH}	$0.9 \times V_{DDPCI}$	—	V
Output low voltage, I_{OL}= 1.5 mA	V_{OL}	—	$0.1 \times V_{DDPCI}$	V
Input Pin Capacitance[1]	C_{IN}		10	pF

Notes: **1.** Not tested. Guaranteed by design.

2.5.4 TDM DC Electrical Characteristics

Table 10. TDM DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDTDM}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current $0<V_{IN}<V_{DDTDM}$	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current	I_{OZ}	–30	30	µA
Output high voltage, I_{OH} = –1.6 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL}= 0.4mA	V_{OL}	—	0.4	V

2.5.6 ATM/UTOPIA/POS DC Electrical Characteristics

Table 13. ATM/UTOPIA/POS DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.4 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –4 mA	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 4 mA	V_{OL}	—	0.5	V

Notes: **1.** Not tested. Guaranteed by design.

2.5.7 SPI DC Electrical Characteristics

Table 14 provides the SPI DC electrical characteristics.

Table 14. SPI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}		30	µA
Output high voltage, I_{OH} = –4.0 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 4.0 mA	V_{OL}	—	0.5	V

2.5.8 GPIO, UART, TIMER, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, JTAG Ports DC Electrical Characteristics

Table 15. GPIO, UART, Timer, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, and JTAG Port[1] DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current, V_{IN} = supply voltage	I_{OZ}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[2]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–30	30	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0.4	V

Notes: **1.** This does not include TDI and TMS, which have internal pullup resistors.
2. Not tested. Guaranteed by design.

2.6.4 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.4.1 DDR SDRAM Input Timings

Table 20 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 2.5 V.

Table 20. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V
Note: At recommended operating conditions with V_{DDDDR} of 2.5 ± 5%.				

Table 21 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 21. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.8 ± 5%.				

Table 22 provides the input AC timing specifications for the DDR SDRAM interface.

Table 22. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit
Controller Skew for MDQS—MDQ/MECC/MDM[1]	t_{CISKEW}			
• 400 MHz		–365	365	ps
• 333 MHz		–390	390	ps
• 266 MHz		–428	428	ps
• 200 MHz		–490	490	ps

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) ± 5%

Figure 8 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

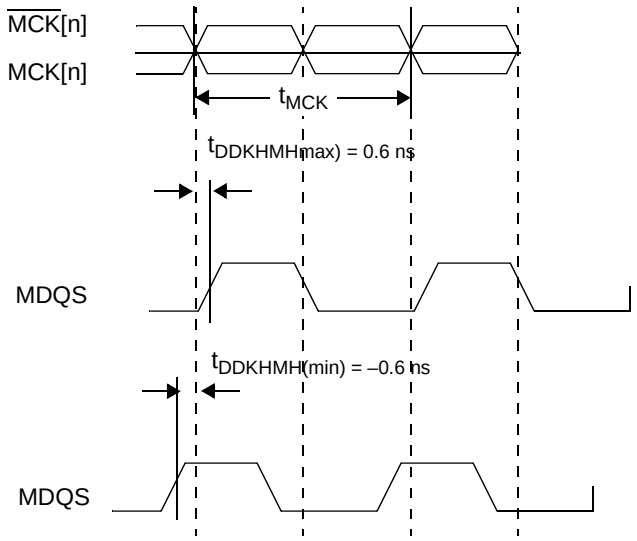


Figure 8. Timing for t_{DDKHMH}

Figure 9 shows the DDR SDRAM output timing diagram.

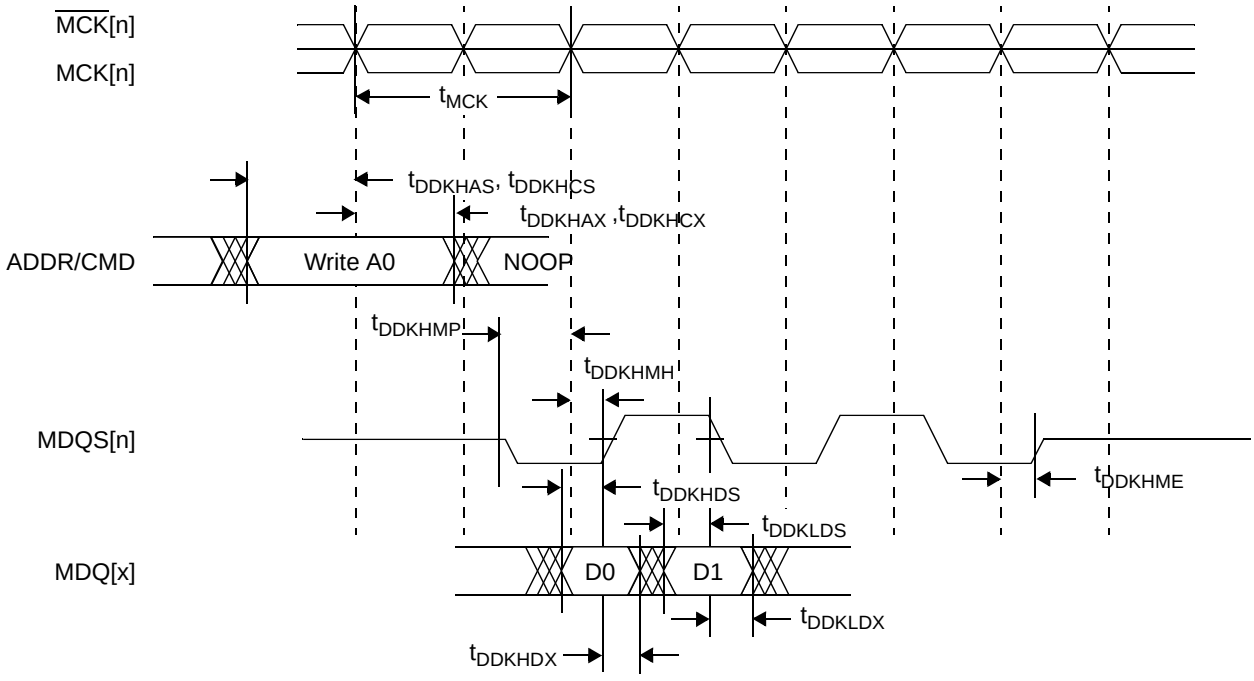


Figure 9. DDR SDRAM Output Timing

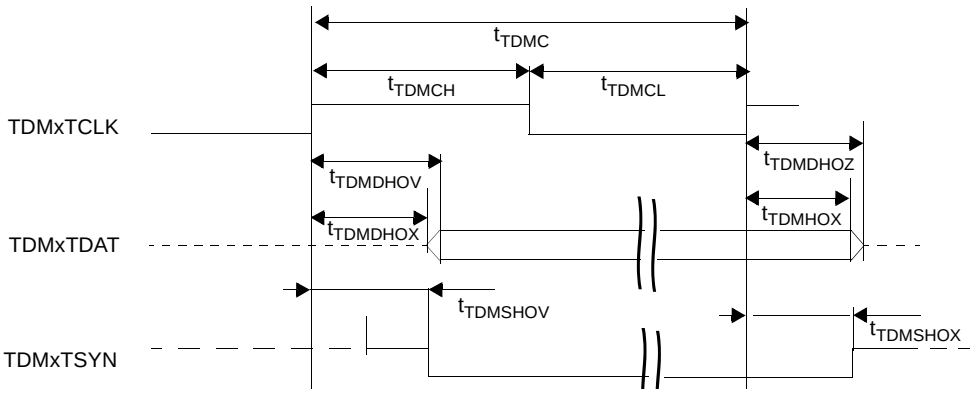


Figure 20. TDM Output Signals

Note: For some TDM modes, transmit data is output on other pins. This timing is also valid for those pins. See the *MSC8144 Reference Manual*

2.6.8 UART Timing

Table 38. UART Timing

Characteristics	Symbol	Expression	Min	Max	Unit
URXD and UTXD inputs high/low duration	$T_{UREFCLK}$	$16 \times T_{REFCLK}$	160	—	ns
Note: $T_{UREFCLK} = T_{REFCLK}$ is guaranteed by design.					

Figure 21 shows the UART input AC timing

Figure 21. UART Input Timing

Figure 22 shows the UART output AC timing

Figure 22. UART Output Timing

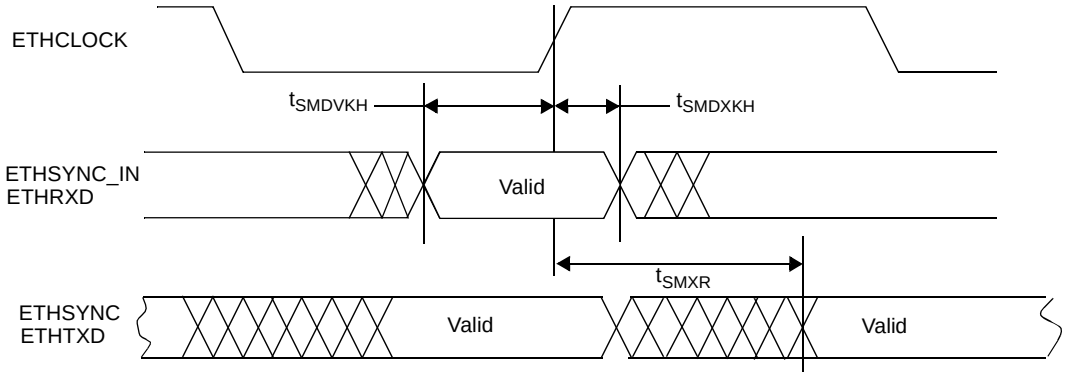


Figure 30. SMII Mode Signal Timing

2.6.10.6 RGMII AC Timing Specifications

Table 45 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 45. RGMII with On-Board Delay AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKEWT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) [2]	t_{SKEWR}	0.9	—	2.6	ns

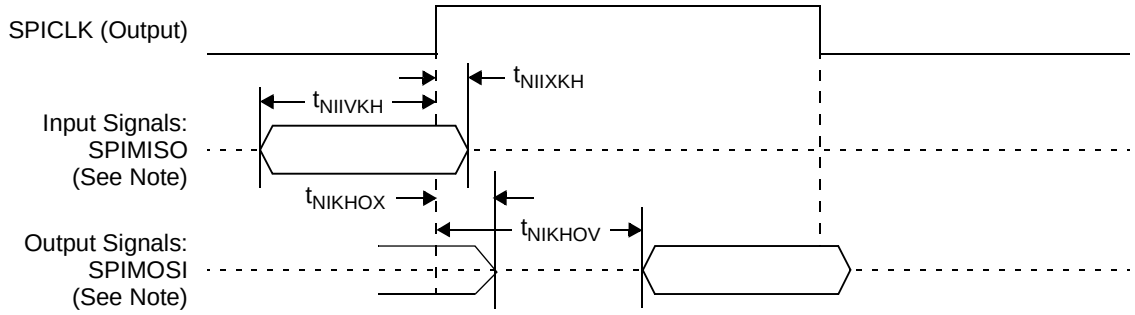
Notes:
1. At recommended operating conditions with LV_{DD} of 2.5 V +/- 5%.
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. GCR4 should be programmed as 0x00001004.

Table 46 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 46. RGMII with No On-Board Delay AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKEWT}	–2.6	—	–0.9	ns
Data to clock input skew (at receiver) [2]	t_{SKEWR}	–0.5	—	0.5	ns

Notes:
1. At recommended operating conditions with LV_{DD} of 2.5 V +/- 5%.
2. This implies that PC board design will require clocks to be routed with no additional trace delay
3. GCR4 should be programmed as 0x0004C130.



Note: The clock edge is selectable on SPI.

Figure 36. SPI AC Timing in Master Mode (Internal Clock)

2.6.13 Asynchronous Signal Timing

Table 49. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN cycle[1]
Output	t_{OUT}	Asynchronous	Application dependent
Note: 1. Relevant for EE0, $\overline{\text{IRQ}}$[15–0], and $\overline{\text{NMI}}$ only.			

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a GPI, the input should be driven until it is acknowledged by the device; the GPIO input status is read from a register.

- *EE port.* Signals EE0, EE1, EE2_0, EE2_1, EE2_2, and EE2_3.
- *Boot function*. Signal STOP_BS.
- *I^2C interface*. Signals I2C_SCL and I2C_SDA.
- *Interrupt inputs*. Signals $\overline{\text{IRQ}}$[15–0] and $\overline{\text{NMI}}$.
- *Interrupt outputs*. Signals $\overline{\text{INT\_OUT}}$ and $\overline{\text{NMI\_OUT}}$ (pulse width is 10 ns).

Figure 37 shows the behavior of the asynchronous signals.

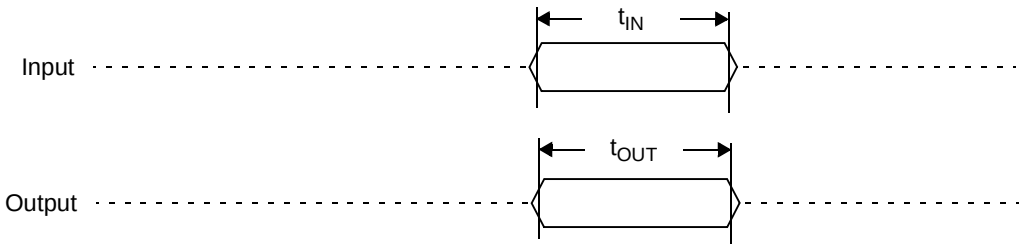


Figure 37. Asynchronous Signal Timing

Figure 40 shows the test access port timing diagram

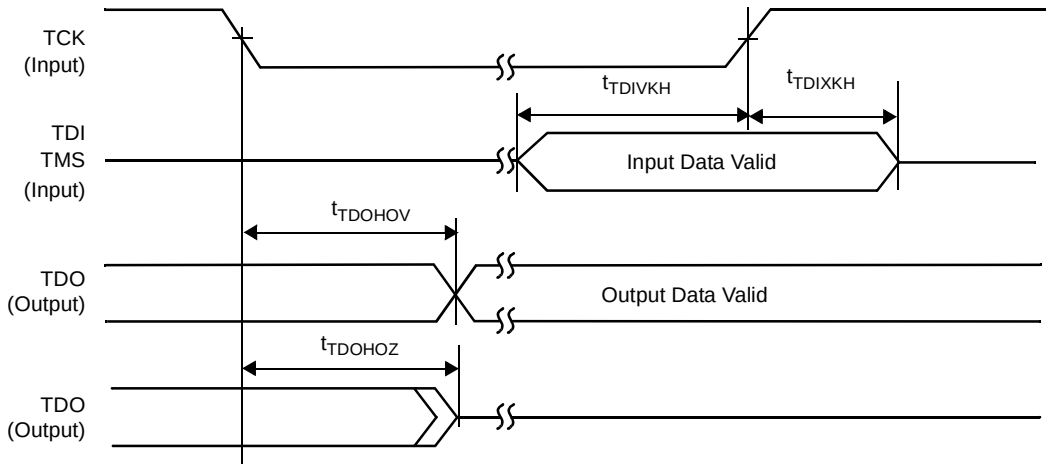


Figure 40. Test Access Port Timing

Figure 41 shows the $\overline{\text{TRST}}$ timing diagram.

Figure 41. $\overline{\text{TRST}}$ Timing

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8144 device is designed into a system.

3.1 Start-up Sequencing Recommendations

3.1.1 Power-on Sequence

Use the following guidelines for power-on sequencing:

- There are no dependencies in power-on/power-off sequence between V_{DDM3} and V_{DD} supplies.
- There are no dependencies in power-on/power-off sequence between RapidIO supplies: V_{DDSXC}, V_{DDSXP}, $V_{DDRIOPLL}$ and other MSC8144 supplies.
- V_{DDPLL} should be coupled with the V_{DD} power rail with extremely low impedance path.

External voltage applied to any input line must not exceed the related to this port I/O supply by more than 0.6 V at any time, including during power-up. Some designs require pull-up voltages applied to selected input lines during power-up for configuration purposes. This is an acceptable exception to the rule during start-up. However, each such input can draw up to 80 mA per input pin per MSC8144 device in the system during start-up. An assertion of the inputs to the high voltage level before power-up should be with slew rate less than 4 V/ns.

The following supplies should rise before any other supplies in any sequence

- V_{DD} and V_{DDPLL} coupled together
- V_{DDM3}

After the above supplies rise to 90% of their nominal value the following I/O supplies may rise in any sequence (see Figure 42):

- V_{DDGE1}
- V_{DDGE2}
- V_{DDIO}
- V_{DDDDR} and MV_{REF} coupled one to another. MV_{REF} should be either at same time or after V_{DDDDR}.
- V_{DDM3IO}
- V_{25M3}

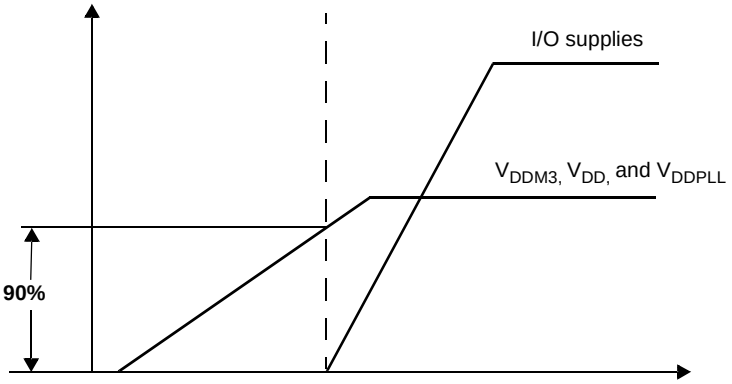


Figure 42. V_{DDM3}, V_{DDM3IO} and V_{25M3} Power-on Sequence

Note:
1. This recommended power sequencing is different from the MSC8122/MSC8126.
2. If no pins that require V_{DDGE1} as a reference supply are used (see Table 1), V_{DDGE1} can be tied to GND.
3. If no pins that require V_{DDGE2} as a reference supply are used (see Table 1), V_{DDGE2} can be tied to GND.
4. If the DDR interface is not used, V_{DDDDR} and MV_{REF} can be tied to GND.
5. If the M3 memory is not used, V_{DDM3}, V_{DDM3IO}, and V_{25M3} can be tied to GND.
6. If the RapidIO interface is not used, V_{DDSX}, V_{DDSXP}, and $V_{DDRIOPLL}$ can be tied to GND.

3.1.2 Start-Up Timing

Section 2.6.1 describes the start-up timing.

3.2 Power Supply Design Considerations

Each PLL supply must have an external RC filter for the V_{DDPLL} input. The filter is a 10 Ω resistor in series with two 2.2 µF, low ESL (<0.5 nH) and low ESR capacitors. All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately (see Figure 43). For optimal noise filtering, place the circuit as close as possible to its V_{DDPLL} inputs. These traces should be short and direct.

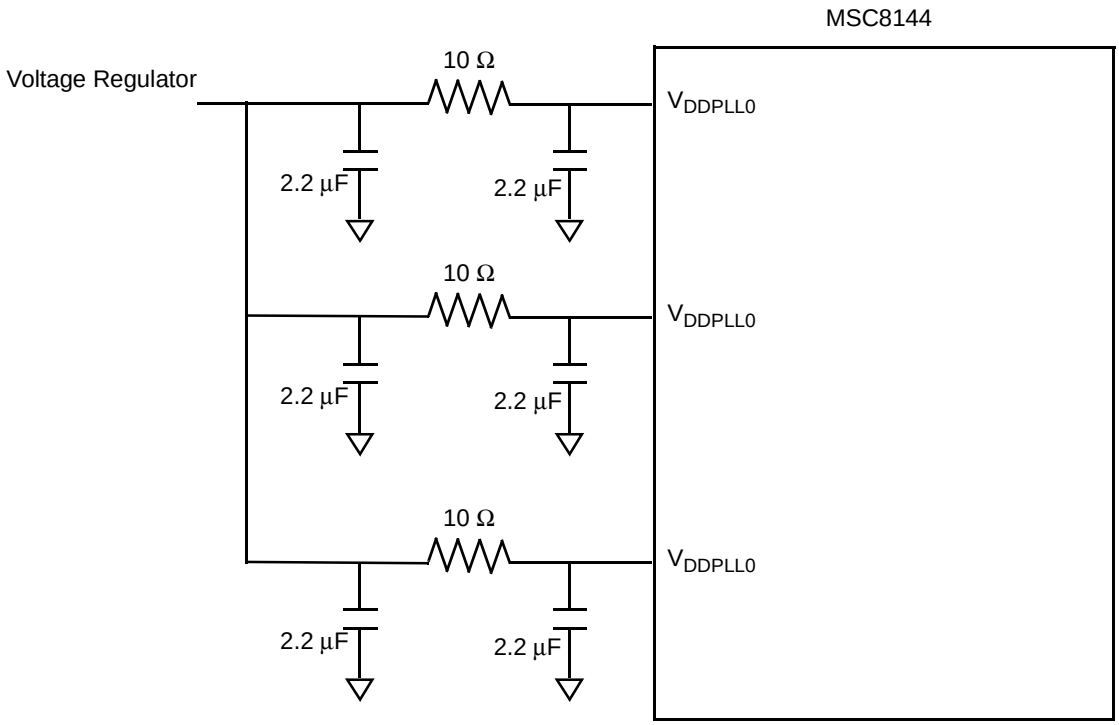


Figure 43. PLL Supplies

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

  Rterm = Rim – Rbuf

  where Rim = trace characteristic impedance

  Rbuf = clock buffer internal impedance.

Note: See *MSC8144 CLKIN and PCI_CLK_IN Board Layout* (AN3440) for an example layout.

3.4 Connectivity Guidelines

Note: Although the package actually uses a ball grid array, the more conventional term pin is used to denote signal connections in this discussion.

First, select the pin multiplexing mode to allocate the required I/O signals. Then use the guidelines presented in the following subsections for board design and connections. The following conventions are used in describing the connectivity requirements:

1. GND indicates using a 10 kΩ pull-down resistor (recommended) or a direct connection to the ground plane. Direct connections to the ground plane may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
2. V_{DD} indicates using a 10 kΩ pull-up resistor (recommended) or a direct connection to the appropriate power supply. Direct connections to the supply may yield DC current up to 50mA through the I/O supply that adds to overall power consumption.
3. Mandatory use of a pull-up or pull-down resistor it is clearly indicated as “pull-up/pull-down”.
4. NC indicates “not connected” and means do not connect anything to the pin.
5. The phrase “in use” indicates a typical pin connection for the required function.

Note: Please see recommendations #1 and #2 as mandatory pull-down or pull-up connection for unused pins in case of subset interface connection.

3.4.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with DDR1 and DDR2 memory.

Note: For information about unused differential/non-differential pins in DDR1/DDR2 modes (that is, unused negative lines of strobes in DDR1), please refer to Table 51.

3.4.1.1 DDR Interface Is Not Used

Table 51. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–31]	NC
MDQS[0–3]	NC
$\overline{\text{MDQS[0–3]}}$	NC
MA[0–15]	NC
MCK[0–2]	NC
$\overline{\text{MCK[0–2]}}$	NC
$\overline{\text{MCS[0–1]}}$	NC

3.4.8 Miscellaneous Pins

Table 65 lists the board connections for the pins if they are not required by the system design. Table 65 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 65. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[0–31]	GND
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ}}$[0–15]	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[0–16]	GND
$\overline{\text{RC\_LDF}}$	NC
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[0–4]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	GND
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
V_{DDIO}	3.3 V
Note: When using I/O multiplexing mode 5 or 6, tie the TDM7TSYN/PCI_AD4 signal (ball number AC9) to GND.	

Note: For details on configuration, see the *MSC8144 Reference Manual*. For additional information, refer to the *MSC8144 Design Checklist* (AN3202).

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Japan
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