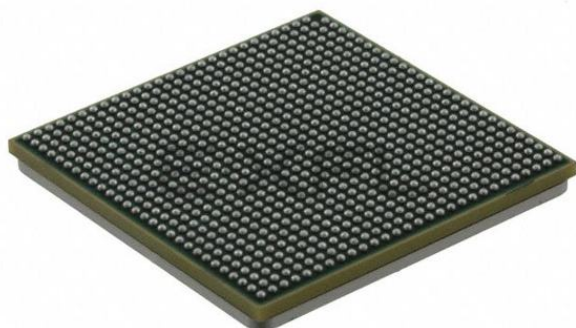




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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Obsolete
Type	SC3400 Core
Interface	Ethernet, I ² C, SPI, TDM, UART, UTOPIA
Clock Rate	800MHz
Non-Volatile Memory	External
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8144tvt800b

1 Pin Assignments and Reset States

This section includes diagrams of the MSC8144 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagrams

Top and bottom views of the FC-PBGA package are shown in Figure 3 and Figure 4 with their ball location index numbers.

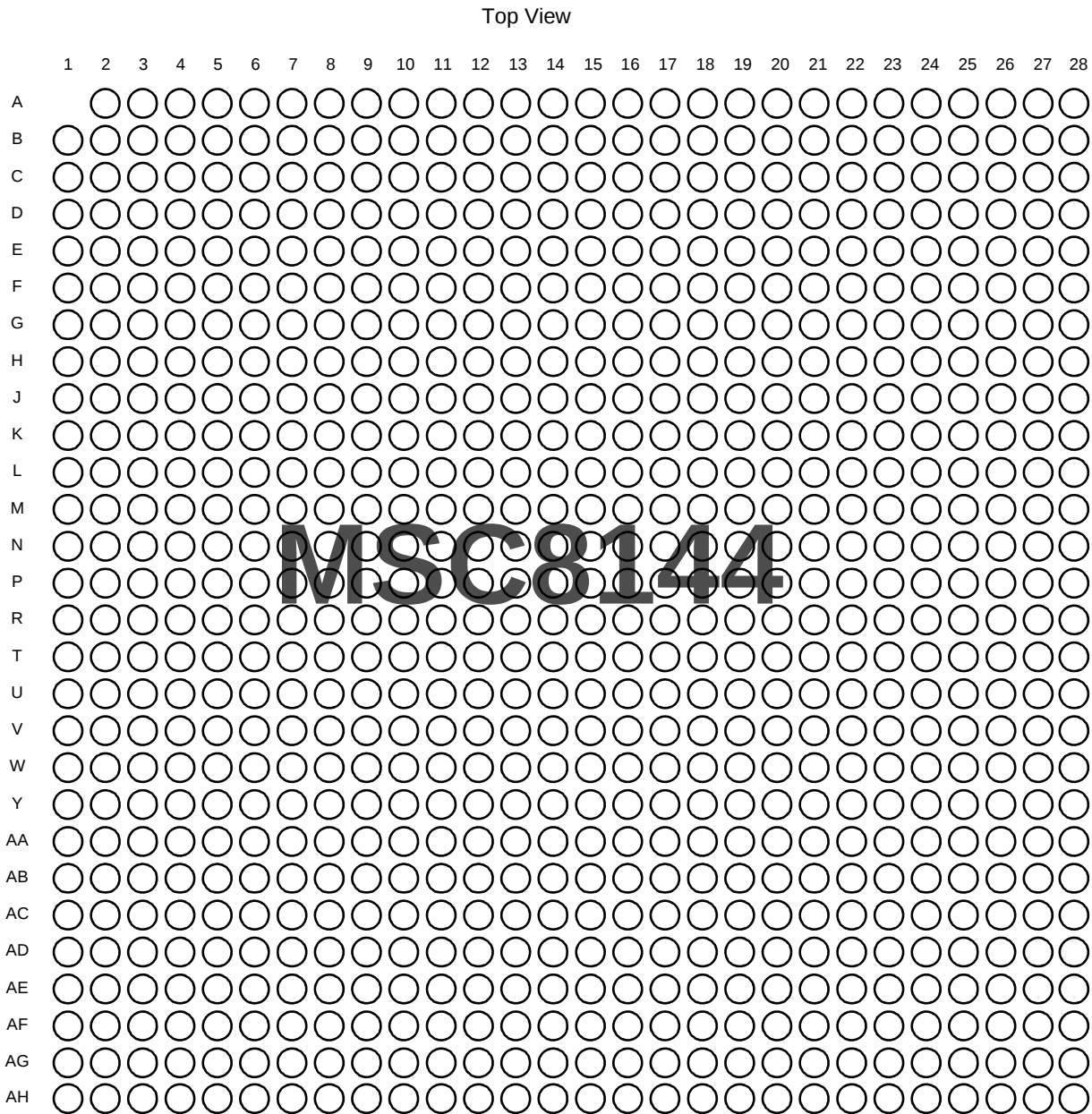


Figure 3. MSC8144 FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power- On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
E2	GE1_RX_CLK/UTP_RD6/ PCI_PAR		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E3	GE1_RD2/UTP_RD4/ PCI_FRAME		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E4	GE1_RD1/UTP_RD3/ PCI_CBE3		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E5	GE1_RD3/UTP_RD5/ PCI_IRDY		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E6	V _{DDGE1}										V _{DDGE1}
E7	GE1_TX_EN/UTP_TD6/ PCI_CBE0		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
E8	Reserved ¹										—
E9	Reserved ¹										—
E10	GND										GND
E11	V _{DD}										V _{DD}
E12	GND										GND
E13	V _{DD}										V _{DD}
E14	GND										GND
E15	V _{DD}										V _{DD}
E16	GND										GND
E17	V _{DD}										V _{DD}
E18	GND										GND
E19	V _{DD}										V _{DD}
E20	GND										GND
E21	V _{DD}										V _{DD}
E22	GND										GND
E23	V _{DDDDR}										V _{DDDDR}
E24	MDQ20										V _{DDDDR}
E25	GND										GND
E26	V _{DDDDR}										V _{DDDDR}
E27	GND										GND
E28	MDQS2										V _{DDDDR}
F1	Reserved ¹										—
F2	GE1_TX_CLK/UTP_RD0/ PCI_AD31		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
F3	V _{DDGE1}										V _{DDGE1}
F4	GE1_TD3/UTP_TD5/ PCI_AD30		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
F5	GE1_TD1/UTP_TD3/ PCI_AD28		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
F6	GND										GND
F7	GE1_TD0/UTP_TD2/ PCI_AD27		UTOPIA	Ethernet 1		PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}
F8	V _{DDGE1}										V _{DDGE1}
F9	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
F10	V _{DD}										V _{DD}
F11	GND										GND
F12	V _{DD}										V _{DD}
F13	GND										GND
F14	V _{DD}										V _{DD}
F15	GND										GND
F16	V _{DD}										V _{DD}
F17	GND										GND
F18	V _{DD}										V _{DD}
F19	GND										GND
F20	V _{DD}										V _{DD}
F21	Reserved ¹										—
F22	V _{DDDDR}										V _{DDDDR}
F23	GND										GND
F24	MDQ19										V _{DDDDR}
F25	MDQ18										V _{DDDDR}
F26	MDM2										V _{DDDDR}
F27	MDQ17										V _{DDDDR}
F28	MDQ16										V _{DDDDR}
G1	Reserved ¹										—
G2	SRESET ⁴										V _{DDIO}
G3	GND										GND
G4	PORESET ⁴										V _{DDIO}
G5	GE1_COL/UTP_RD1		UTOPIA	Ethernet 1	UTOPIA			Ethernet 1	UTOPIA	V _{DDIO}	
G6	GE1_TD2/UTP_TD4/ PCI_AD29		UTOPIA	Ethernet 1	PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}	
G7	GE1_RX_DV/UTP_RD7		UTOPIA	Ethernet 1	UTOPIA			Ethernet 1	UTOPIA	V _{DDGE1}	
G8	GE1_TX_ER/UTP_TD7/ PCI_CBE1		UTOPIA	Ethernet 1	PCI	UTOPIA		Ethernet 1	UTOPIA	V _{DDGE1}	
G9	V _{DD}										V _{DD}
G10	GND										GND
G11	V _{DD}										V _{DD}
G12	GND										GND
G13	V _{DD}										V _{DD}
G14	GND										GND
G15	V _{DD}										V _{DD}
G16	GND										GND
G17	V _{DD}										V _{DD}
G18	GND										GND
G19	V _{DD}										V _{DD}
G20	GND										GND
G21	Reserved ¹	—									—
G22	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power- On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
G23	MBA1										V _{DDDDR}
G24	MA3										V _{DDDDR}
G25	MA8										V _{DDDDR}
G26	V _{DDDDR}										V _{DDDDR}
G27	GND										GND
G28	MCK0										V _{DDDDR}
H1	Reserved ¹										—
H2	CLKIN										V _{DDIO}
H3	HRESET										V _{DDIO}
H4	PCI_CLK_IN										V _{DDIO}
H5	NMI										V _{DDIO}
H6	URXD/GPIO14/IRQ8/ RC_LDF ^{3, 6}	RC_LDF	UART/GPIO/IRQ								V _{DDIO}
H7	GE1_RX_ER/PCI_AD6/ GPIO25/IRQ15 ^{3, 6}		GPIO/ IRQ	Ethernet 1	PCI			GPIO/ IRQ	Ethernet 1		V _{DDIO}
H8	GE1_CRS/PCI_AD5		PCI	Ethernet 1	PCI			Ethernet 1			V _{DDIO}
H9	GND										GND
H10	V _{DD}										V _{DD}
H11	GND										GND
H12	V _{DD}										V _{DD}
H13	GND										GND
H14	V _{DD}										V _{DD}
H15	V _{DD}										V _{DD}
H16	V _{DD}										V _{DD}
H17	GND										GND
H18	V _{DD}										V _{DD}
H19	GND										GND
H20	V _{DD}										V _{DD}
H21	V _{DD}										V _{DD}
H22	V _{DDDDR}										V _{DDDDR}
H23	MBA0										V _{DDDDR}
H24	MA15										V _{DDDDR}
H25	V _{DDDDR}										V _{DDDDR}
H26	MA9										V _{DDDDR}
H27	MA7										V _{DDDDR}
H28	MCK0										V _{DDDDR}
J1	Reserved ¹										—
J2	GND										GND
J3	V _{DDIO}										V _{DDIO}
J4	STOP_BS										V _{DDIO}
J5	NMI_OUT ⁴										V _{DDIO}
J6	INT_OUT ⁴										V _{DDIO}
J7	SDA/GPIO27 ^{3, 4, 6}		I2C/GPIO								V _{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V _{DDIO}										V _{DDIO}
J9	V _{DD}										V _{DD}
J10	GND										GND
J11	V _{DD}										V _{DD}
J12	GND										GND
J13	V _{DD}										V _{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V _{DD}										V _{DD}
J18	GND										GND
J19	V _{DD}										V _{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V _{DDDDR}										V _{DDDDR}
J25	GND										GND
J26	V _{DDDDR}										V _{DDDDR}
J27	GND										GND
J28	V _{DDDDR}										V _{DDDDR}
K1	Reserved ¹										—
K2	Reserved ¹										—
K3	Reserved ¹										—
K4	Reserved ¹										—
K5	V _{DDPLL2A}										V _{DDPLL2A}
K6	GND										GND
K7	V _{DDPLL0A}										V _{DDPLL0A}
K8	V _{DDPLL1A}										V _{DDPLL1A}
K9	V _{DD}										V _{DD}
K10	GND										GND
K11	V _{DD}										V _{DD}
K12	GND										GND
K13	V _{DD}										V _{DD}
K14	V _{DD}										V _{DD}
K15	V _{DD}										V _{DD}
K16	V _{DD}										V _{DD}
K17	V _{DD}										V _{DD}
K18	GND										GND
K19	V _{DD}										V _{DD}
K20	GND										GND
K21	V _{DD}										V _{DD}
K22	V _{DDDDR}										V _{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
M8	V _{DDIO}										V _{DDIO}
M9	V _{DD}										V _{DD}
M10	GND										GND
M11	V _{DD}										V _{DD}
M12	GND										GND
M13	V _{DD}										V _{DD}
M14	GND										GND
M15	V _{DD}										V _{DD}
M16	GND										GND
M17	V _{DD}										V _{DD}
M18	GND										GND
M19	V _{DD}										V _{DD}
M20	GND										GND
M21	V _{DD}										V _{DD}
M22	V _{DDDDR}										V _{DDDDR}
M23	MCS1										V _{DDDDR}
M24	MA13										V _{DDDDR}
M25	MA2										V _{DDDDR}
M26	MA0										V _{DDDDR}
M27	GND										GND
M28	MCK1										V _{DDDDR}
N1	Reserved ¹										—
N2	V _{DDIO}										V _{DDIO}
N3	TMS										V _{DDIO}
N4	UTP_RD10/PCI_AD14 ⁵		UTOPIA		PCI	UTOPIA					V _{DDIO}
N5	V _{DDIO}		Power								V _{DDIO}
N6	UTP_RADDR1/PCI_AD8		UTOPIA		PCI	UTOPIA					V _{DDIO}
N7	UTP_TD9/PCI_AD31		UTOPIA		PCI	UTOPIA					V _{DDIO}
N8	TMR3/PCI_IRDY/GPIO19 ^{3, 6} /UTP_TEOP		TIMER/GPIO				PCI	TIMER/GPIO		UTOPIA	V _{DDIO}
N9	GND										GND
N10	V _{DDM3}										V _{DDM3}
N11	V _{DD}										V _{DD}
N12	V _{DDM3}										V _{DDM3}
N13	V _{DD}										V _{DD}
N14	V _{DDM3}										V _{DDM3}
N15	V _{DD}										V _{DD}
N16	V _{DDM3}										V _{DDM3}
N17	V _{DD}										V _{DD}
N18	V _{DDM3}										V _{DDM3}
N19	V _{DD}										V _{DD}
N20	V _{DDM3}										V _{DDM3}
N21	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power- On Reset Value	I/O Multiplexing Mode ²								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
T21	GND										GND
T22	V _{DDDDR}										V _{DDDDR}
T23	GND										GND
T24	V _{DDDDR}										V _{DDDDR}
T25	GND										GND
T26	V _{DDDDR}										V _{DDDDR}
T27	GND										GND
T28	V _{DDDDR}										V _{DDDDR}
U1	Reserved ¹										—
U2	UTP_TCLK/PCI_AD29		UTOPIA		PCI	UTOPIA					V _{DDIO}
U3	UTP_TADDR4/PCI_AD27		UTOPIA		PCI	UTOPIA					V _{DDIO}
U4	UTP_TADDR2		UTOPIA								V _{DDIO}
U5	GND										GND
U6	UTP_REN/PCI_AD20		UTOPIA		PCI	UTOPIA					V _{DDIO}
U7	PCI_AD26		PCI								V _{DDIO}
U8	PCI_AD25		PCI								V _{DDIO}
U9	Reserved ¹										V _{DDIO}
U10	V _{DDM3}										V _{DDM3}
U11	GND										GND
U12	V _{DDM3}										V _{DDM3}
U13	GND										GND
U14	V _{DDM3}										V _{DDM3}
U15	GND										GND
U16	V _{DDM3}										V _{DDM3}
U17	GND										GND
U18	V _{DDM3}										V _{DDM3}
U19	GND										GND
U20	V _{DDM3}										V _{DDM3}
U21	GND										GND
U22	GND										GND
U23	MDQ7										V _{DDDDR}
U24	MDQ3										V _{DDDDR}
U25	MDQ4										V _{DDDDR}
U26	MDQ5										V _{DDDDR}
U27	MDQ1										V _{DDDDR}
U28	MDQ0										V _{DDDDR}
V1	Reserved ¹										—
V2	UTP_TD10/ <u>PCI_CBE0</u>		UTOPIA		PCI	UTOPIA					V _{DDIO}
V3	UTP_TADDR3		UTOPIA								V _{DDIO}
V4	UTP_TD1/ <u>PCI_PERR</u>		UTOPIA		PCI		UTOPIA				V _{DDIO}
V5	UTP_TADDR0/PCI_AD23		UTOPIA		PCI	UTOPIA					V _{DDIO}
V6	UTP_TADDR1/PCI_AD24		UTOPIA		PCI	UTOPIA					V _{DDIO}
V7	UTP_TCLAV/PCI_AD28		UTOPIA		PCI	UTOPIA					V _{DDIO}

Figure 8 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKMH}).

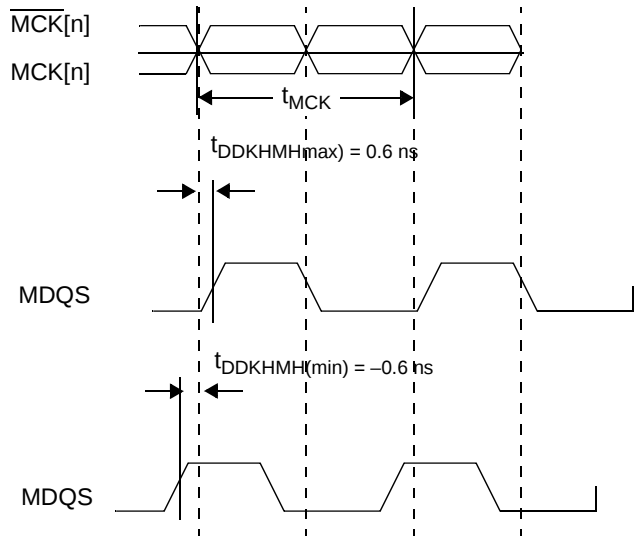


Figure 8. Timing for t_{DDKMH}

Figure 9 shows the DDR SDRAM output timing diagram.

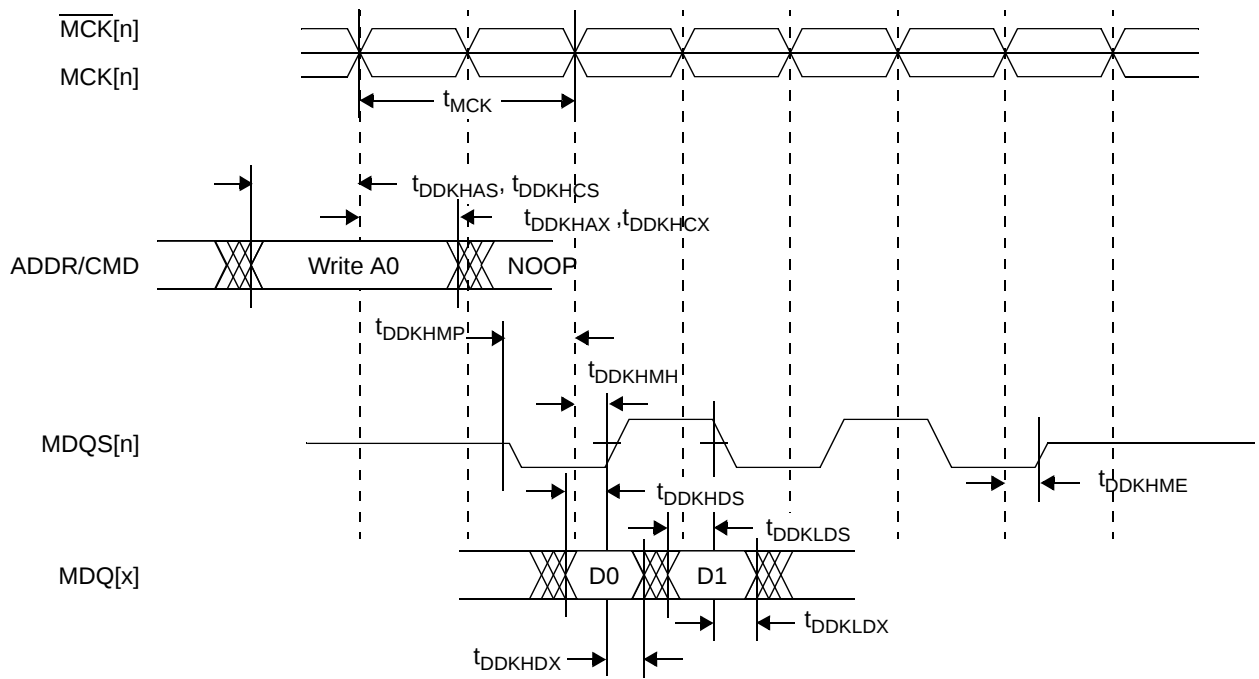


Figure 9. DDR SDRAM Output Timing

Figure 10 provides the AC test load for the DDR bus.

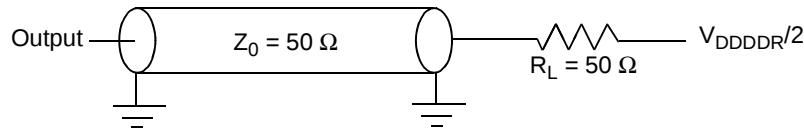


Figure 10. DDR AC Test Load

2.6.5 Serial RapidIO Timing and SGMII Timing

2.6.5.1 AC Requirements for $\overline{\text{SRIO_REF_CLK}}$ and $\overline{\text{SRIO_REF_CLK}}$

Table 24 lists AC signal specifications.

Table 24. SDn_REF_CLK and $\overline{\text{SDn_REF_CLK}}$ AC Signal Specifications

Parameter Description	Symbol	Min	Typical	Max	Units	Comments
REFCLK cycle time	t_{REF}	—	10 (8, 6.4)	—	ns	8 ns applies only to serial RapidIO system with 125-MHz reference clock. 6.4 ns applies only to serial RapidIO systems with a 156.25 MHz reference clock. Note: SGMII uses the 8 ns (125 MHz) value only.

2.6.5.2 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 11 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between voltage levels A and B, where $A > B$.

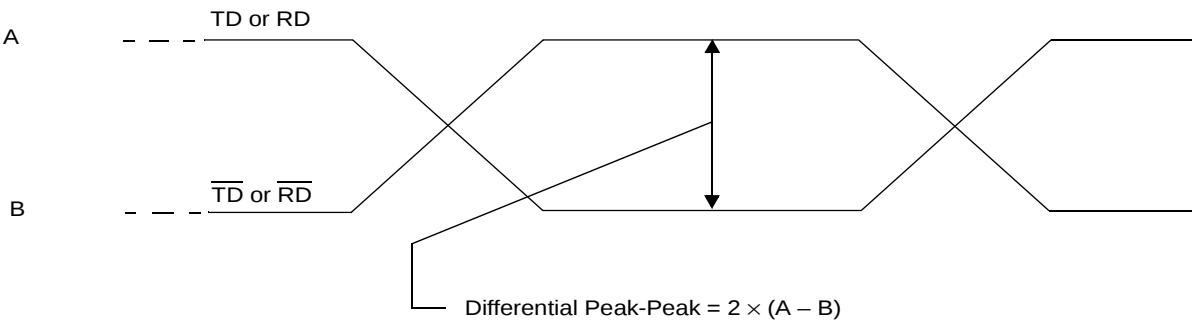


Figure 11. Differential V_{pp} of Transmitter or Receiver

Note: This explanation uses generic TD/ $\overline{\text{TD}}$ /RD/ $\overline{\text{RD}}$ signal names. These correspond to SRIO_TXD/ $\overline{\text{SRIO_TXD}}$ /SRIO_RXD/ $\overline{\text{SRIO_RXD}}$ respectively.

Table 25. Short Run Transmitter AC Timing Specifications—1.25 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	± 100 ppm

Table 26. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV _{PP}	
Deterministic Jitter	J_D		0.17	UI _{PP}	
Total Jitter	J_T		0.35	UI _{PP}	
Multiple Output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	± 100 ppm

Table 27. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV _{PP}	
Deterministic Jitter	J_D		0.17	UI _{PP}	
Total Jitter	J_T		0.35	UI _{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	± 100 ppm

Table 28. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV _{PP}	
Deterministic Jitter	J_D		0.17	UI _{PP}	
Total Jitter	J_T		0.35	UI _{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	± 100 ppm

Table 29. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV _{PP}	
Deterministic Jitter	J_D		0.17	UI _{PP}	
Total Jitter	J_T		0.35	UI _{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 30. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV _{PP}	
Deterministic Jitter	J_D		0.17	UI _{PP}	
Total Jitter	J_T		0.35	UI _{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 12 with the parameters specified in Table 31 when measured at the output pins of the device and the device is driving a $100\ \Omega \pm 5\%$ differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

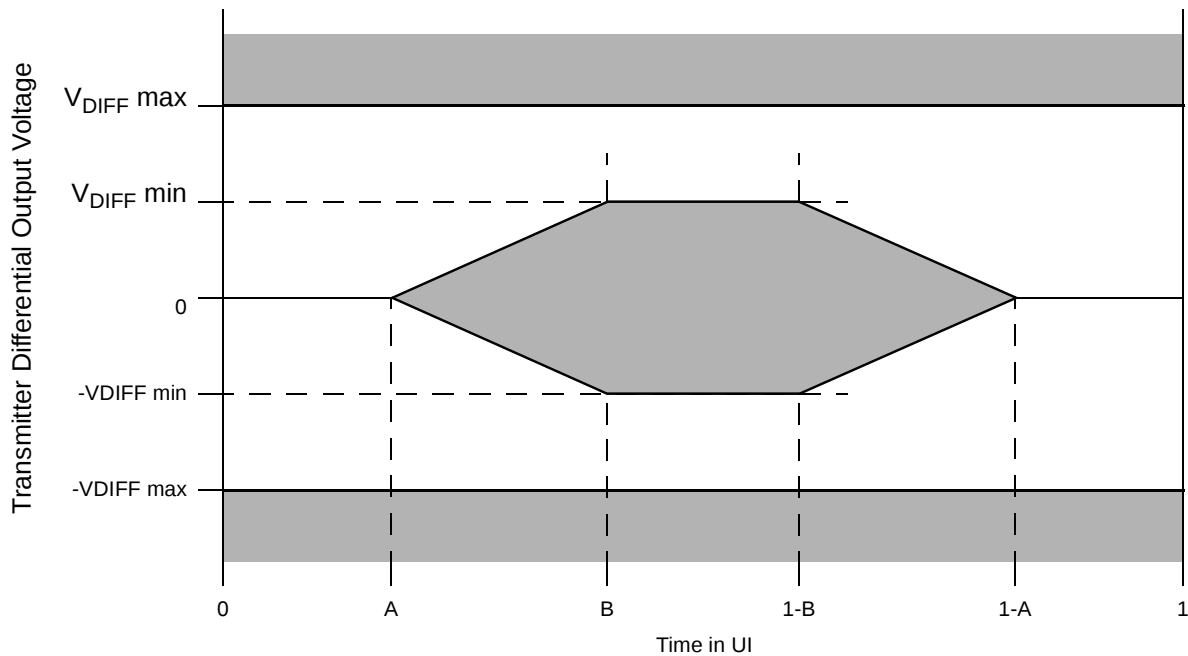


Figure 12. Transmitter Output Compliance Mask

Table 31. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

2.6.5.5 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section. Receiver input impedance shall result in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to $0.8 \times$ baud frequency. This includes contributions from internal circuitry, the package, and any external components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ω resistive for differential return loss and 25 Ω resistive for common mode.

Table 32. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV _{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI _{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI _{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI _{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	800	800	ps	± 100 ppm

Table 33. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV _{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI _{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI _{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI _{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	400	400	ps	± 100 ppm

Table 34. Receiver AC Timing Specifications—3.125 Gbaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV _{PP}	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37		UI _{PP}	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55		UI _{PP}	Measured at receiver
Total Jitter Tolerance	J_T	0.65		UI _{PP}	Measured at receiver. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 13. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.
Multiple Input Skew	S_{MI}		22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER		10^{-12}		
Unit Interval	UI	320	320	ps	±100 ppm

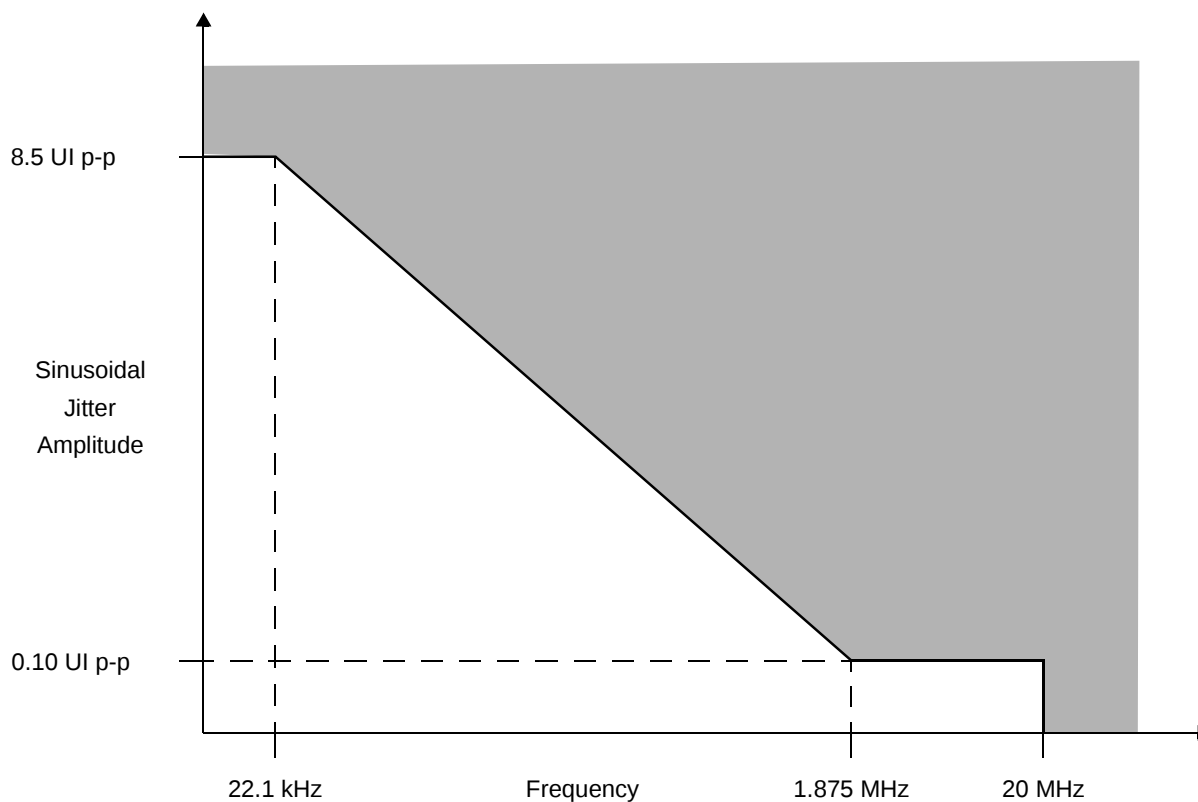


Figure 13. Single Frequency Sinusoidal Jitter Limits

2.6.5.6 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 32, Table 33, and Table 34) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 14 with the parameters specified in Table 35. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a $100\ \Omega \pm 5\%$ differential resistive load.

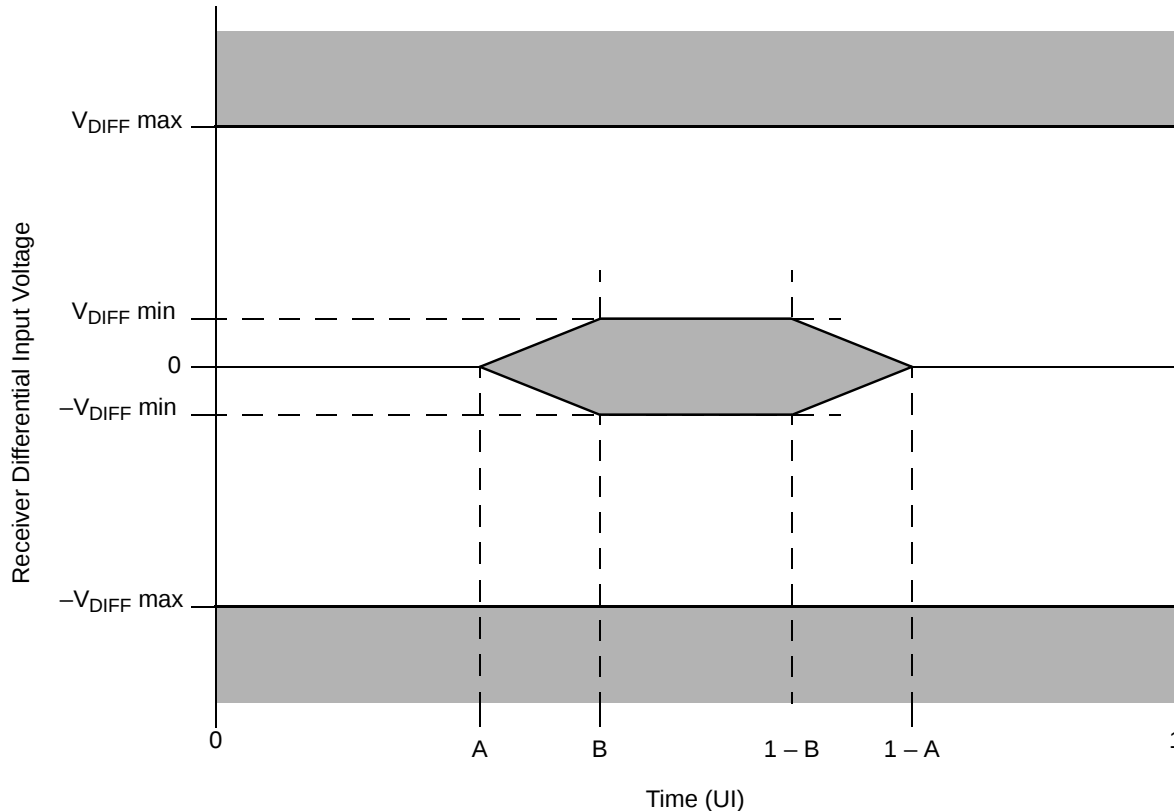


Figure 14. Receiver Input Compliance Mask

Table 35. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

2.6.5.7 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of **IEEE** Std. 802.3ae-2002™, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of **IEEE** Std. 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of **IEEE** Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

Figure 26 provides the AC test load.

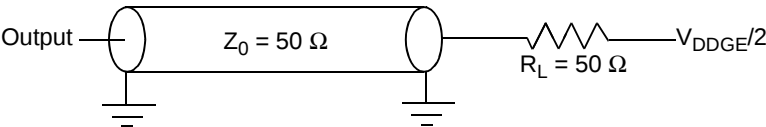


Figure 26. AC Test Load

Figure 27 shows the MII receive AC timing diagram.

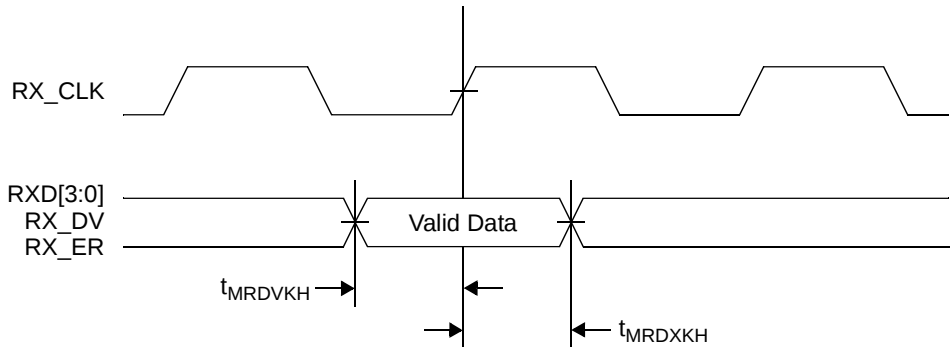


Figure 27. MII Receive AC Timing

2.6.10.4 RMII Transmit and Receive AC Timing Specifications

Table 43 provides the RMII transmit and receive AC timing specifications.

Table 43. RMII Transmit and Receive AC Timing Specifications

Parameter/Condition	Symbol ¹	Min	Max	Unit
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	65	%
REF_CLK to RMII data TXD[1–0], TX_EN delay	$t_{RMTKHDX}$	2	10	ns
RXD[1–0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	ns
RXD[1–0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	ns
Typical REF_CLK clock period (t_{RMX}) is 20 ns				
Notes: 1. Typical REF_CLK clock period (t_{RMX}) is 20 ns 2. Program GCR4 as 0x00001405				

2.6.11 ATM/UTOPIA/POS Timing

Table 47 provides the ATM/UTOPIA/POS input and output AC timing specifications.

Table 47. ATM/UTOPIA/POS AC Timing (External Clock) Specifications

Characteristic	Symbol	Min	Max	Unit
Outputs—External clock delay	t_{UEKHOV}	1	9	ns
Outputs—External clock High Impedance ¹	t_{UEKHOX}	1	9	ns
Inputs—External clock input setup time	t_{UEIVKH}	4		ns
Inputs—External clock input hold time	t_{UEIXKH}	1		ns
Notes: 1. Not tested. Guaranteed by design. 2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. Although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.				

Figure 32 provides the AC test load for the ATM/UTOPIA/POS.

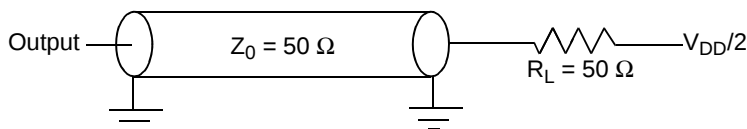


Figure 32. ATM/UTOPIA/POS AC Test Load

Figure 33 shows the ATM/UTOPIA/UTOPIA timing with external clock.

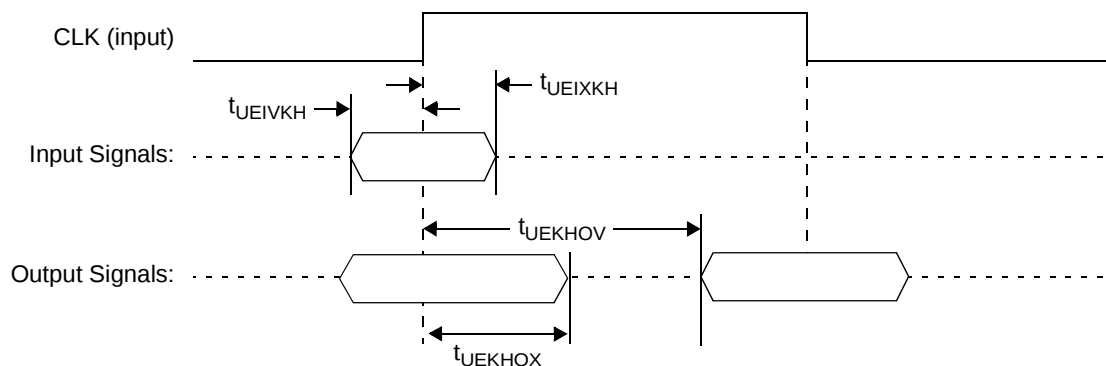


Figure 33. ATM/UTOPIA/POS AC Timing (External Clock)

3.4.2.2 Serial RapidIO Specific Lane Is Not Used

Table 55. Connectivity of Serial RapidIO Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SRIO_IMP_CAL_RX	in use
SRIO_IMP_CAL_TX	in use
SRIO_REF_CLK	in use
SRIO_REF_CLK	in use
SRIO_RXDx	GND _{SXC}
SRIO_RXDx	GND _{SXC}
SRIO_TXDx	NC
SRIO_TXDx	NC
V _{DDRIOPLL}	in use
GND _{RIOPLL}	in use
GND _{SXP}	GND _{SXP}
GND _{SXC}	GND _{SXC}
V _{DDSXP}	1.0 V
V _{DDSXC}	1.0 V
Note: The <i>x</i> indicates the lane number {0,1,2,3} for all unused lanes.	

3.4.3 M3 Memory Related Pins

Table 56. Connectivity of M3 Related Pins When M3 Memory Is Not Used

Signal Name	Pin Connection
M3_RESET	NC
V _{25M3}	GND
V _{DDM3}	GND
V _{DDM3IO}	GND

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
GE2_SGMII_RX	GND _{SXC}
GE2_SGMII_TX	NC
GE2_SGMII_TX	NC
GE2_TCK	NC
GE2_TD[0–3]	NC
GE2_TX_EN	NC

3.4.4.3 GE1 and GE2 Management Pins

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used (that is, V_{DDGE2} is connected to GND), Table 61 lists the recommended management pin connections.

Table 61. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used

Signal Name	Pin Connection
GE_MDC	NC
GE_MDIO	NC

3.4.5 UTOPIA/POS Related Pins

Table 62 lists the board connections of the UTOPIA/POS pins when the entire UTOPIA/POS interface is not used or subset of UTOPIA/POS interface is used. For multiplexing options that select a subset of the UTOPIA/POS interface, use the connections described in Table 62 for those signals that are not selected. Table 62 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 62. Connectivity of UTOPIA/POS Related Pins When UTOPIA/POS Interface Is Not Used

Signal Name	Pin Connection
UTP_IR	GND
UTP_RADDR[0–4]	V_{DDIO}
UTP_RCLAV_PDRPA	NC
UTP_RCLK	GND
UTP_RD[0–15]	GND
UTP_REN	V_{DDIO}
UTP_RPRTY	GND
UTP_RSOC	GND
UTP_TADDR[0–4]	V_{DDIO}
UTP_TCLAV	NC
UTP_TCLK	GND
UTP_TD[0–15]	NC
UTP_TEN	V_{DDIO}
UTP_TPRTY	NC
UTP_TSOC	NC
V_{DDIO}	3.3 V

7 Revision History

Table 66 provides a revision history for this data sheet.

Table 66. Document Revision History

Rev.	Date	Description
0	Feb. 2007	Initial public release.
1	Apr. 2007	- Adds new I/O multiplexing mode 7 that supports POS functionality. - Updates reference voltage supply for pins G5, H7, and H8 in Table 1. - Updates start-up timing recommendations with regard to TRST and M3_RESET in Section 2.7.1. - Adds input clock duty cycles in Table 20. - Updates PCI AC timings in Table 41. - Removes UTOPIA internal clock specifications in Table 52. - Updates JTAG timings in Table 56. - Clarifies connectivity guidelines for Ethernet pins in Section 3.3.4. - Miscellaneous pin connectivity guidelines were updated in Table 71. - Updates name of core subsystem reference manual.
2	June 2007	- Corrected AA4 definition in Table 1. Changed TDM5TD3 to correct name TDM5TDAT. - Removed Figure 35 because the device does not support UTOPIA using an internal clock. Renumbered subsequent figures. - Removed Section 3.5 <i>Thermal Considerations</i>. To be replaced with an application note.
3	Sep 2007	- Updated M3 voltage range in Table 3. - Changed note in Table 7 for PLL power supplies. - DDR voltage designator changed from V_{DD} to V_{DDDDR} in Table 8, Table 10, Section 2.7.4.1, Section 2.7.4.2, and Figure 11. Changed range on I_{OZ} in Table 8 and Table 10. - Deleted text before Table 13 and added note 2 to input pin capacitance. - Deleted text before Table 14, added a 1 to the note, and added note 1 to input pin capacitance. - Deleted Section 2.6.5 on page 32 and renumbered subsequent subsections. - Deleted text before new Section 2.6.5.1. - Added a 1 to the note in Table 15 and added note 1 to input pin capacitance. - Deleted ac voltage rows from Table 16. Added note 1 to input pin capacitance. - Changed output high and low voltage levels in Table 17 and Table 18. - Deleted text before Table 19. - Added clock skew ranges in percent in Table 21. - Changed V_{REF} to MV_{REF} in Table 26. - Changed V_{DD} to V_{DDIO} in Table 41 Updated note 2. - Added note 4 to Table 42. Changed $t_{TDMSHOX}$ value. - Changed V_{DD} to V_{DDGE} in Figure 27 and Figure 30. - Changed the value of the data to clock out skew in Table 51. - Changed EE pin timing in Table 55. - Changed the head for the JTAG timing section, now Section 2.7.15. - Updated JTAG timing for TCK cycle time, TCK high phase, and boundary scan input data hold time in Table 56. - Added new Section 3.3 with guidelines for board layout for clock and timing signals. Renumbered subsequent sections.
4	Sep 2007	- Changed leakage current values in Table 13, Table 14, Table 11, Table 16, Table 17, Table 18, and Table 19 from -10 and $10\ \mu A$ to -30 and $30\ \mu A$. - Change the minimum value of t_{MDDVKH} in Table 45 from 5 ns to 7 ns. - Updated note 1 in Table 45.
5	Oct 2007	- Corrected column numbering in Figure 3 and Figure 4. - Updated SPI signal names in Table 1.
6	Oct 2007	Updated SPI signal names in Table 1.