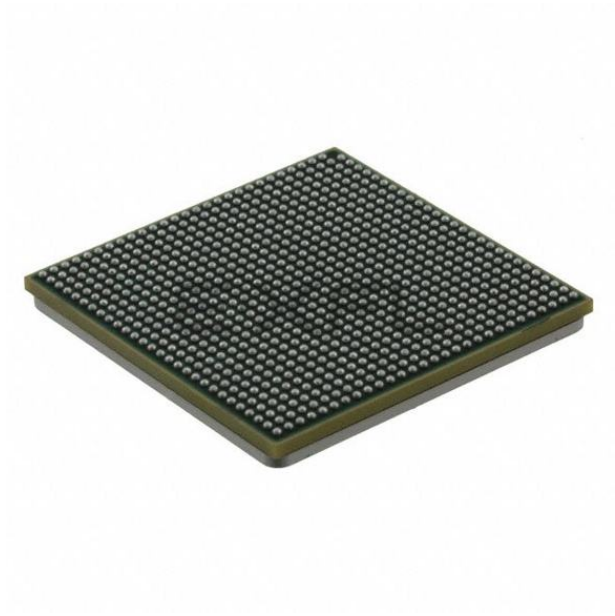


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3400 Core
Interface	Ethernet, I²C, SPI, TDM, UART, UTOPIA
Clock Rate	1GHz
Non-Volatile Memory	External
On-Chip RAM	10.5MB
Voltage - I/O	3.30V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 90°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8144vt1000b

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
J8	V_{DDIO}										V_{DDIO}
J9	V_{DD}										V_{DD}
J10	GND										GND
J11	V_{DD}										V_{DD}
J12	GND										GND
J13	V_{DD}										V_{DD}
J14	GND										GND
J15	GND										GND
J16	GND										GND
J17	V_{DD}										V_{DD}
J18	GND										GND
J19	V_{DD}										V_{DD}
J20	GND										GND
J21	GND										GND
J22	GND										GND
J23	GND										GND
J24	V_{DDDDR}										V_{DDDDR}
J25	GND										GND
J26	V_{DDDDR}										V_{DDDDR}
J27	GND										GND
J28	V_{DDDDR}										V_{DDDDR}
K1	Reserved[1]										—
K2	Reserved[1]										—
K3	Reserved[1]										—
K4	Reserved[1]										—
K5	$V_{DDPLL2A}$										$V_{DDPLL2A}$
K6	GND										GND
K7	$V_{DDPLL0A}$										$V_{DDPLL0A}$
K8	$V_{DDPLL1A}$										$V_{DDPLL1A}$
K9	V_{DD}										V_{DD}
K10	GND										GND
K11	V_{DD}										V_{DD}
K12	GND										GND
K13	V_{DD}										V_{DD}
K14	V_{DD}										V_{DD}
K15	V_{DD}										V_{DD}
K16	V_{DD}										V_{DD}
K17	V_{DD}										V_{DD}
K18	GND										GND
K19	V_{DD}										V_{DD}
K20	GND										GND
K21	V_{DD}										V_{DD}
K22	V_{DDDDR}										V_{DDDDR}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
T21	GND										GND
T22	V_{DDDDR}										V_{DDDDR}
T23	GND										GND
T24	V_{DDDDR}										V_{DDDDR}
T25	GND										GND
T26	V_{DDDDR}										V_{DDDDR}
T27	GND										GND
T28	V_{DDDDR}										V_{DDDDR}
U1	Reserved[1]										—
U2	UTP_TCLK/PCI_AD29		UTOPIA		PCI	UTOPIA					V_{DDIO}
U3	UTP_TADDR4/PCI_AD27		UTOPIA		PCI	UTOPIA					V_{DDIO}
U4	UTP_TADDR2		UTOPIA								V_{DDIO}
U5	GND										GND
U6	$\overline{\text{UTP\_REN}}$/PCI_AD20		UTOPIA		PCI	UTOPIA					V_{DDIO}
U7	PCI_AD26		PCI								V_{DDIO}
U8	PCI_AD25		PCI								V_{DDIO}
U9	Reserved[1]										V_{DDIO}
U10	V_{DDM3}										V_{DDM3}
U11	GND										GND
U12	V_{DDM3}										V_{DDM3}
U13	GND										GND
U14	V_{DDM3}										V_{DDM3}
U15	GND										GND
U16	V_{DDM3}										V_{DDM3}
U17	GND										GND
U18	V_{DDM3}										V_{DDM3}
U19	GND										GND
U20	V_{DDM3}										V_{DDM3}
U21	GND										GND
U22	GND										GND
U23	MDQ7										V_{DDDDR}
U24	MDQ3										V_{DDDDR}
U25	MDQ4										V_{DDDDR}
U26	MDQ5										V_{DDDDR}
U27	MDQ1										V_{DDDDR}
U28	MDQ0										V_{DDDDR}
V1	Reserved[1]										—
V2	UTP_TD10/$\overline{\text{PCI\_CBE0}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
V3	UTP_TADDR3		UTOPIA								V_{DDIO}
V4	UTP_TD1/$\overline{\text{PCI\_PERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
V5	UTP_TADDR0/PCI_AD23		UTOPIA		PCI	UTOPIA					V_{DDIO}
V6	UTP_TADDR1/PCI_AD24		UTOPIA		PCI	UTOPIA					V_{DDIO}
V7	UTP_TCLAV/PCI_AD28		UTOPIA		PCI	UTOPIA					V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
V8	V_{DDIO}										V_{DDIO}
V9	Reserved[1]										V_{DDIO}
V10	GND										GND
V11	V_{DDM3}										V_{DDM3}
V12	GND										GND
V13	V_{DDM3}										V_{DDM3}
V14	GND										GND
V15	V_{DDM3}										V_{DDM3}
V16	GND										GND
V17	V_{DDM3}										V_{DDM3}
V18	GND										GND
V19	V_{DDM3}										V_{DDM3}
V20	GND										GND
V21	GND										GND
V22	V_{DDDDR}										V_{DDDDR}
V23	MDQ2										V_{DDDDR}
V24	V_{DDDDR}										V_{DDDDR}
V25	MDQ6										V_{DDDDR}
V26	GND										GND
V27	V_{DDDDR}										V_{DDDDR}
V28	MDQS0										V_{DDDDR}
W1	Reserved[1]										—
W2	UTP_TD12/$\overline{\text{PCI\_CBE2}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W3	UTP_TD11/$\overline{\text{PCI\_CBE1}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W4	V_{DDIO}										V_{DDIO}
W5	GND										GND
W6	UTP_TD15/$\overline{\text{PCI\_IRDY}}$		UTOPIA		PCI	UTOPIA					V_{DDIO}
W7	UTP_TD0/$\overline{\text{PCI\_SERR}}$		UTOPIA		PCI		UTOPIA				V_{DDIO}
W8	UTP_RSOC/PCI_AD22		UTOPIA		PCI	UTOPIA					V_{DDIO}
W9	Reserved[1]										V_{DDIO}
W10	V_{DDM3}										V_{DDM3}
W11	GND										GND
W12	V_{25M3}										V_{25M3}
W13	GND										GND
W14	V_{DDM3}										V_{DDM3}
W15	V_{25M3}										V_{25M3}
W16	V_{DDM3}										V_{DDM3}
W17	GND										GND
W18	V_{25M3}										V_{25M3}
W19	GND										GND
W20	V_{DDM3}										V_{DDM3}
W21	GND										GND
W22	GND										GND

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AB19	V_{DDM3}										V_{DDM3}
AB20	GND										GND
AB21	GND										GND
AB22	V_{DDDDR}										V_{DDDDR}
AB23	MECC7										V_{DDDDR}
AB24	MECC1										V_{DDDDR}
AB25	MECC4										V_{DDDDR}
AB26	MECC5										V_{DDDDR}
AB27	MECC2										V_{DDDDR}
AB28	ECC_MDQS										V_{DDDDR}
AC1	Reserved[1]										—
AC2	UTP_RD9/RC13	RC13	UTOPIA								V_{DDIO}
AC3	UTP_RD8/RC12	RC12	UTOPIA								V_{DDIO}
AC4	TDM6TCLK/PCI_AD22		TDM			PCI		TDM			V_{DDIO}
AC5	TDM6RSYN/PCI_AD21/ GPIO6/ $\overline{IRQ12}$[3, 6]		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ			V_{DDIO}
AC6	V_{DDIO}										V_{DDIO}
AC7	TDM3TSYN/RC11	RC11	TDM								V_{DDIO}
AC8	PCI_AD23/GPIO7/$\overline{IRQ13}$/ TDM6TDAT[3, 6]/UTP_RMOD		TDM/GPIO/IRQ			PCI		TDM/GPIO/IRQ		UTOPIA	V_{DDIO}
AC9	TDM7TSYN/ PCI_AD4		TDM		PCI			reserved			V_{DDIO}
AC10	V_{DDM3IO}										V_{DDM3IO}
AC11	GND										GND
AC12	V_{DDM3}										V_{DDM3}
AC13	GND										GND
AC14	V_{DDM3}										V_{DDM3}
AC15	GND										GND
AC16	V_{DDM3}										V_{DDM3}
AC17	GND										GND
AC18	V_{DDM3}										V_{DDM3}
AC19	GND										GND
AC20	V_{DDM3IO}										V_{DDM3IO}
AC21	Reserved[1]										—
AC22	MECC6										V_{DDDDR}
AC23	MECC3										V_{DDDDR}
AC24	ECC_MDM										V_{DDDDR}
AC25	V_{DDDDR}										V_{DDDDR}
AC26	MECC0										V_{DDDDR}
AC27	V_{DDDDR}										V_{DDDDR}
AC28	$\overline{ECC\_MDQS}$										V_{DDDDR}
AD1	Reserved[1]										—
AD2	GPIO1[3, 6]		GPIO								V_{DDIO}
AD3	TMR0/GPIO13		TIMER/GPIO								V_{DDIO}

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name	Power-On Reset Value	I/O Multiplexing Mode[2]								Ref. Supply
			0 (000)	1 (001)	2 (010)	3 (011)	4 (100)	5 (101)	6 (110)	7 (111)	
AH17	Reserved[1]										—
AH18	Reserved[1]										—
AH19	Reserved[1]										—
AH20	Reserved[1]										—
AH21	Reserved[1]										—
AH22	Reserved[1]										—
AH23	Reserved[1]										—
AH24	Reserved[1]										—
AH25	Reserved[1]										—
AH26	Reserved[1]										—
AH27	Reserved[1]										—
AH28	Reserved[1]										—

Notes:
1. Reserved signals should be disconnected for compatibility with future revisions of the device.
2. For signals with same functionality in all modes the appropriate cells are empty.
3. The choice between GPIO function and other function is by GPIO registers setup. For configuration details, see **Chapter 23,** *GPIO* in the *MSC8144 Reference Manual*.
4. Open-drain signal.
5. Internal 20 KΩ pull-up resistor.
6. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See **Chapter 23**, *GPIO* of the *MSC8144 Reference Manual* for configuration details.

2.5.6 ATM/UTOPIA/POS DC Electrical Characteristics

Table 13. ATM/UTOPIA/POS DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[1]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.4 V[1]	I_H	–30	30	µA
Output high voltage, I_{OH} = –4 mA	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 4 mA	V_{OL}	—	0.5	V

Notes: **1.** Not tested. Guaranteed by design.

2.5.7 SPI DC Electrical Characteristics

Table 14 provides the SPI DC electrical characteristics.

Table 14. SPI DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}		30	µA
Output high voltage, I_{OH} = –4.0 mA	V_{OH}	2.4	—	V
Output low voltage, I_{OL} = 4.0 mA	V_{OL}	—	0.5	V

2.5.8 GPIO, UART, TIMER, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, JTAG Ports DC Electrical Characteristics

Table 15. GPIO, UART, Timer, EE, STOP_BS, I²C, $\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$, CLKIN, and JTAG Port[1] DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit
Supply voltage 3.3 V	V_{DDIO}	3.135	3.465	V
Input high voltage	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input leakage current, V_{IN} = supply voltage	I_{IN}	–30	30	µA
Tri-state (high impedance off state) leakage current, V_{IN} = supply voltage	I_{OZ}	–30	30	µA
Signal low input current, V_{IL} = 0.4 V[2]	I_L	–30	30	µA
Signal high input current, V_{IH} = 2.0 V[2]	I_H	–30	30	µA
Output high voltage, I_{OH} = –2 mA, except open drain pins	V_{OH}	2.4	3.465	V
Output low voltage, I_{OL}= 3.2 mA	V_{OL}	—	0.4	V

Notes: **1.** This does not include TDI and TMS, which have internal pullup resistors.
2. Not tested. Guaranteed by design.

2.6.4 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.4.1 DDR SDRAM Input Timings

Table 20 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 2.5 V.

Table 20. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V
Note: At recommended operating conditions with V_{DDDDR} of 2.5 ± 5%.				

Table 21 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 21. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.8 ± 5%.				

Table 22 provides the input AC timing specifications for the DDR SDRAM interface.

Table 22. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit
Controller Skew for MDQS—MDQ/MECC/MDM[1]	t_{CISKEW}			
• 400 MHz		–365	365	ps
• 333 MHz		–390	390	ps
• 266 MHz		–428	428	ps
• 200 MHz		–490	490	ps

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.8 V or 2.5 V) ± 5%

Figure 10 provides the AC test load for the DDR bus.

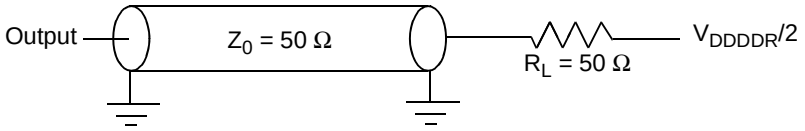


Figure 10. DDR AC Test Load

2.6.5 Serial RapidIO Timing and SGMII Timing

2.6.5.1 AC Requirements for SRIO_REF_CLK and $\overline{\text{SRIO\_REF\_CLK}}$

Table 24 lists AC signal specifications.

Table 24. SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ AC Signal Specifications

Parameter Description	Symbol	Min	Typical	Max	Units	Comments
REFCLK cycle time	t_{REF}	—	10 (8, 6.4)	—	ns	8 ns applies only to serial RapidIO system with 125-MHz reference clock. 6.4 ns applies only to serial RapidIO systems with a 156.25 MHz reference clock. **Note:** SGMII uses the 8 ns (125 MHz) value only.

2.6.5.2 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 11 shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between voltage levels A and B, where A > B.

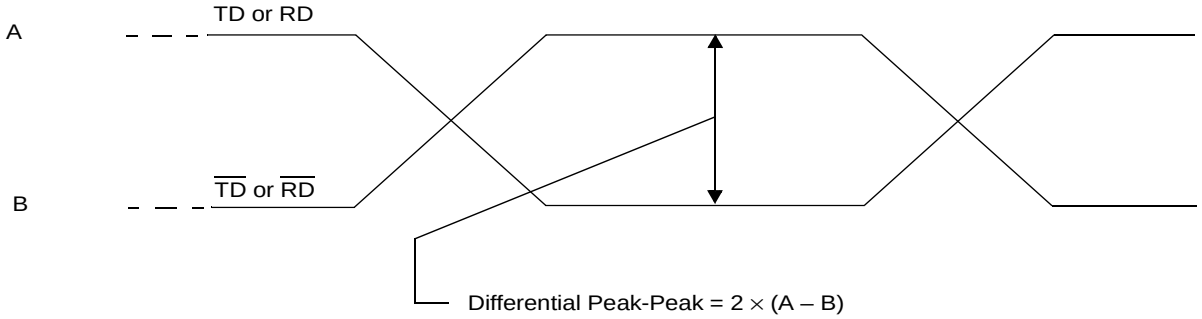


Figure 11. Differential V_{PP} of Transmitter or Receiver

Note: This explanation uses generic TD/$\overline{\text{TD}}$/RD/$\overline{\text{RD}}$ signal names. These correspond to SRIO_TXD/$\overline{\text{SRIO\_TXD}}$/ SRIO_RXD/$\overline{\text{SRIO\_RXD}}$ respectively.

Table 29. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	±100 ppm

Table 30. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage	V_O	-0.40	2.30	V	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV_{PP}	
Deterministic Jitter	J_D		0.17	UI_{PP}	
Total Jitter	J_T		0.35	UI_{PP}	
Multiple output skew	S_{MO}		1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	±100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the transmitter output compliance mask shown in Figure 12 with the parameters specified in Table 31 when measured at the output pins of the device and the device is driving a 100 Ω ±5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the transmitter output compliance mask when pre-emphasis is disabled or minimized.

2.6.5.6 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding bit error rate specification (Table 32, Table 33, and Table 34) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the receiver input compliance mask shown in Figure 14 with the parameters specified in Table 35. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω ±5% differential resistive load.

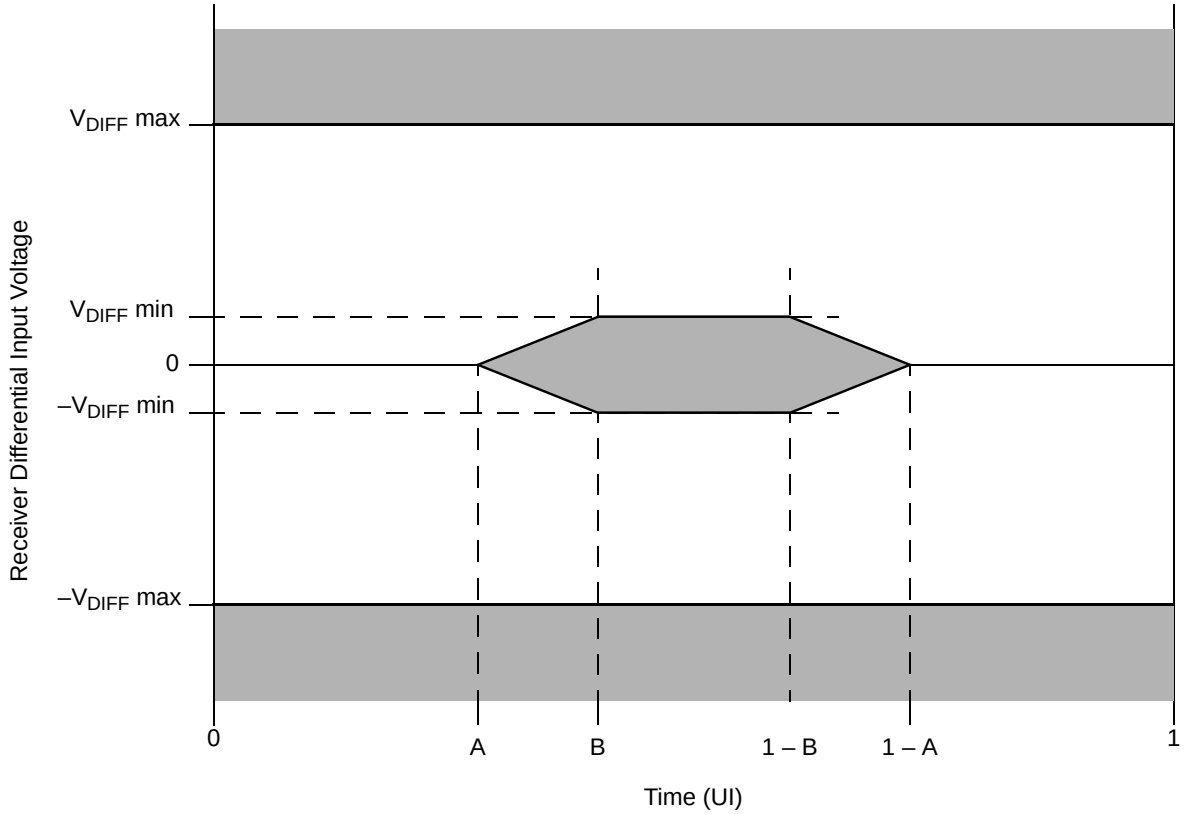


Figure 14. Receiver Input Compliance Mask

Table 35. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

2.6.5.7 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of **IEEE** Std. 802.3ae-2002™, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of **IEEE** Std. 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of **IEEE** Std. 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

Table 36. PCI AC Timing Specifications (continued)

Parameter	Symbol	33 MHz		66 MHz		Unit
		Min	Max	Min	Max	

Notes:
1. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
2. All PCI signals are measured from $0.5 \times V_{DDIO}$ of the rising edge of PCI_CLK_IN to $0.4 \times V_{DDIO}$ of the signal in question for 3.3-V PCI signaling levels.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is in Table 19 and Figure 7

Figure 15 provides the AC test load for the PCI.

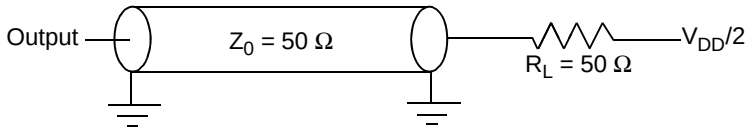


Figure 15. PCI AC Test Load

Figure 16 shows the PCI input AC timing conditions.

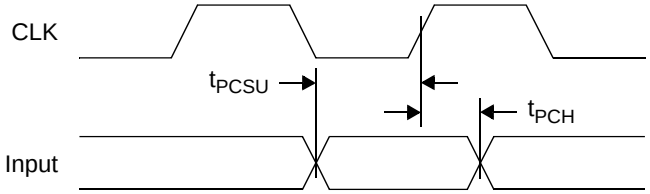


Figure 16. PCI Input AC Timing Measurement Conditions

Figure 17 shows the PCI output AC timing conditions.

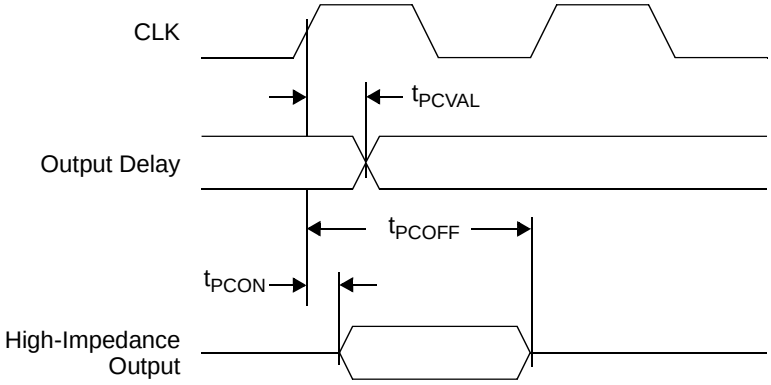


Figure 17. PCI Output AC Timing Measurement Condition

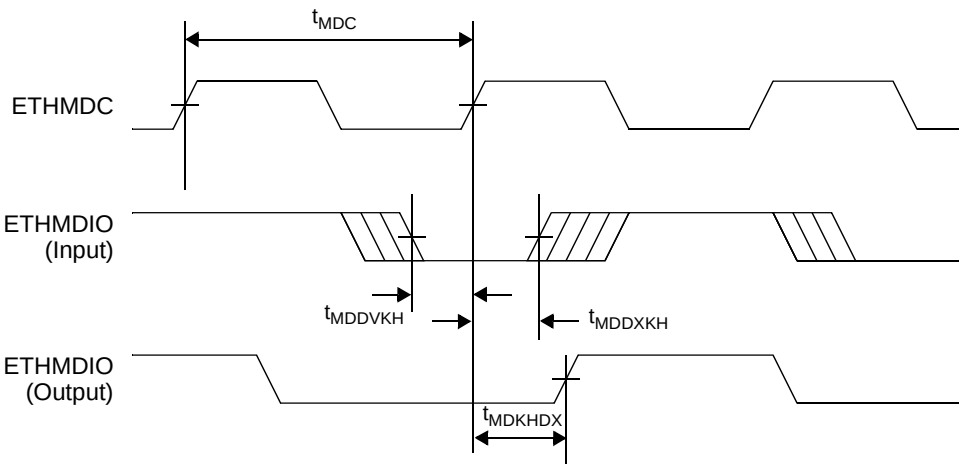


Figure 24. MII Management Interface Timing

2.6.10.2 MII Transmit AC Timing Specifications

Table 41 provides the MII transmit AC timing specifications.

Table 41. MII Transmit AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Max	Unit
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	25	ns

Notes: **1.** Typical TX_CLK period (t_{MTX}) for 10 Mbps is 400 ns and for 100 Mbps is 40 ns.
2. Program GCR4 as 0x00030CC3.

Figure 25 shows the MII transmit AC timing diagram.

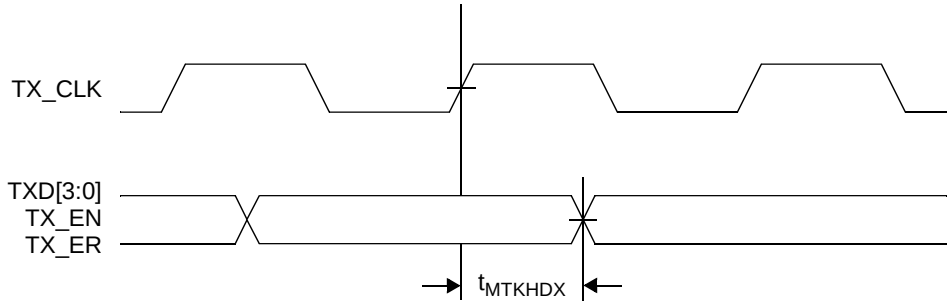


Figure 25. MII Transmit AC Timing

2.6.10.3 MII Receive AC Timing Specifications

Table 42 provides the MII receive AC timing specifications.

Table 42. MII Receive AC Timing Specifications

Parameter/Condition	Symbol [1]	Min	Max	Unit
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	2	—	ns

Notes: **1.** Typical RX_CLK period (t_{MRX}) for 10 Mbps is 400 ns and for 100 Mbps is 40 ns.
2. Program GCR4 as 0x00030CC3.

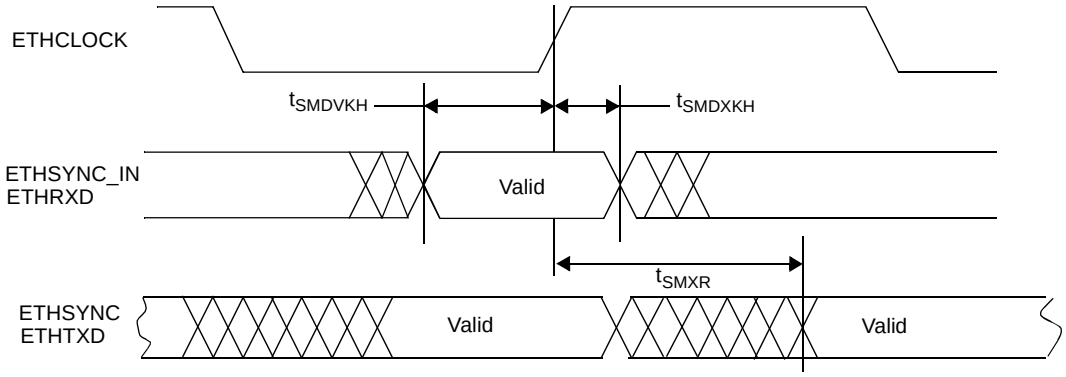


Figure 30. SMII Mode Signal Timing

2.6.10.6 RGMII AC Timing Specifications

Table 45 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 45. RGMII with On-Board Delay AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKEWT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) [2]	t_{SKEWR}	0.9	—	2.6	ns

Notes:
1. At recommended operating conditions with LV_{DD} of 2.5 V +/- 5%.
2. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. GCR4 should be programmed as 0x00001004.

Table 46 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 46. RGMII with No On-Board Delay AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKEWT}	–2.6	—	–0.9	ns
Data to clock input skew (at receiver) [2]	t_{SKEWR}	–0.5	—	0.5	ns

Notes:
1. At recommended operating conditions with LV_{DD} of 2.5 V +/- 5%.
2. This implies that PC board design will require clocks to be routed with no additional trace delay
3. GCR4 should be programmed as 0x0004C130.

Figure 31 shows the RGMII AC timing and multiplexing diagrams.

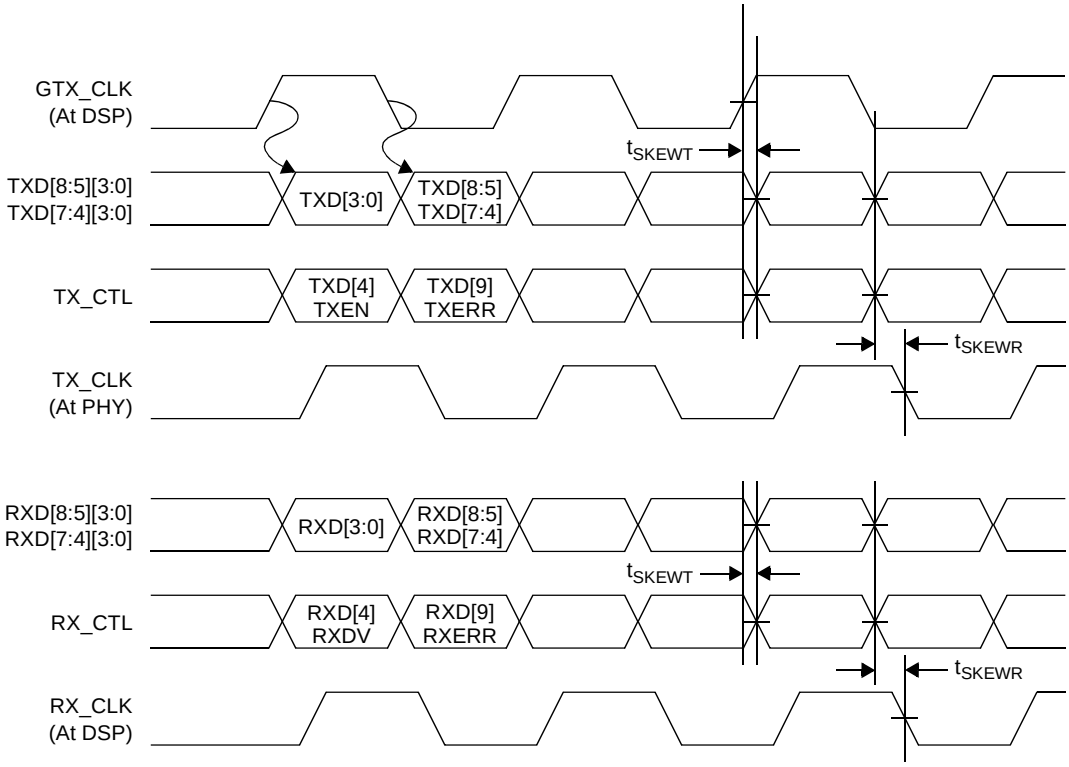


Figure 31. RGMII AC Timing and Multiplexing

2.6.11 ATM/UTOPIA/POS Timing

Table 47 provides the ATM/UTOPIA/POS input and output AC timing specifications.

Table 47. ATM/UTOPIA/POS AC Timing (External Clock) Specifications

Characteristic	Symbol	Min	Max	Unit
Outputs—External clock delay	t_{UEKHOV}	1	9	ns
Outputs—External clock High Impedance[1]	t_{UEKHOX}	1	9	ns
Inputs—External clock input setup time	t_{UEIVKH}	4		ns
Inputs—External clock input hold time	t_{UEIXKH}	1		ns

Notes:
1. Not tested. Guaranteed by design.
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin. Although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 32 provides the AC test load for the ATM/UTOPIA/POS.

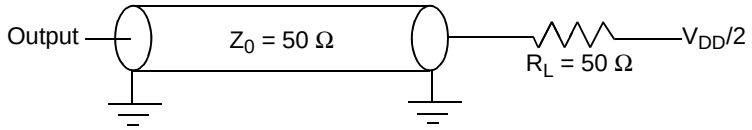


Figure 32. ATM/UTOPIA/POS AC Test Load

Figure 33 shows the ATM/UTOPIA/UTOPIA timing with external clock.

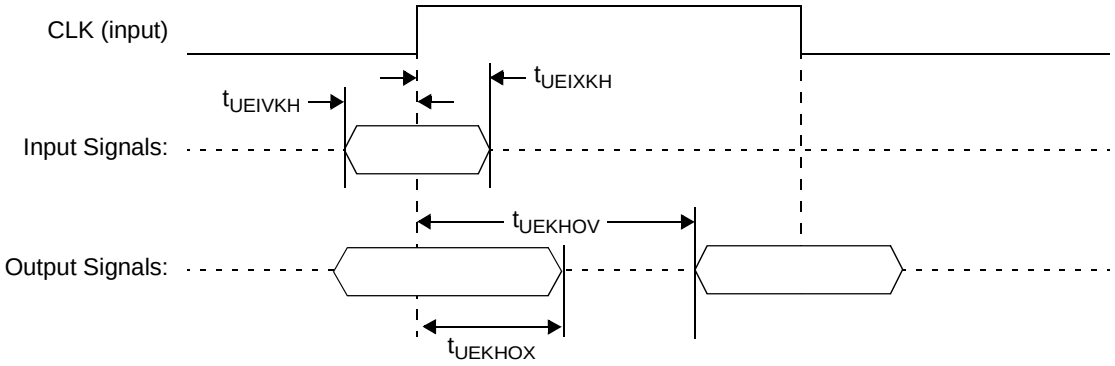


Figure 33. ATM/UTOPIAPOS AC Timing (External Clock)

2.6.14 JTAG Signals

Table 50. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at V_M = 1.6 V	t_{TCKH}	15.0	—	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
$\overline{\text{TRST}}$ assert time	t_{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 38 shows the Test Clock Input Timing Diagram

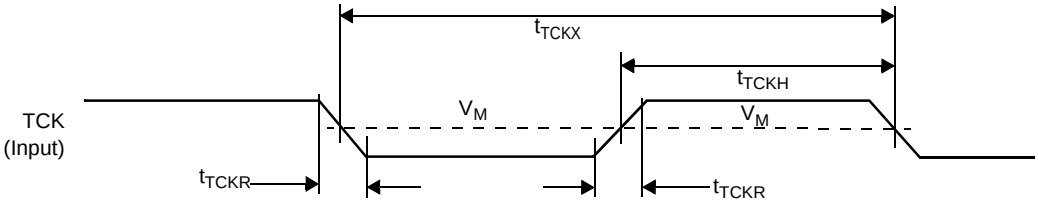


Figure 38. Test Clock Input Timing

Figure 39 shows the boundary scan (JTAG) timing diagram.

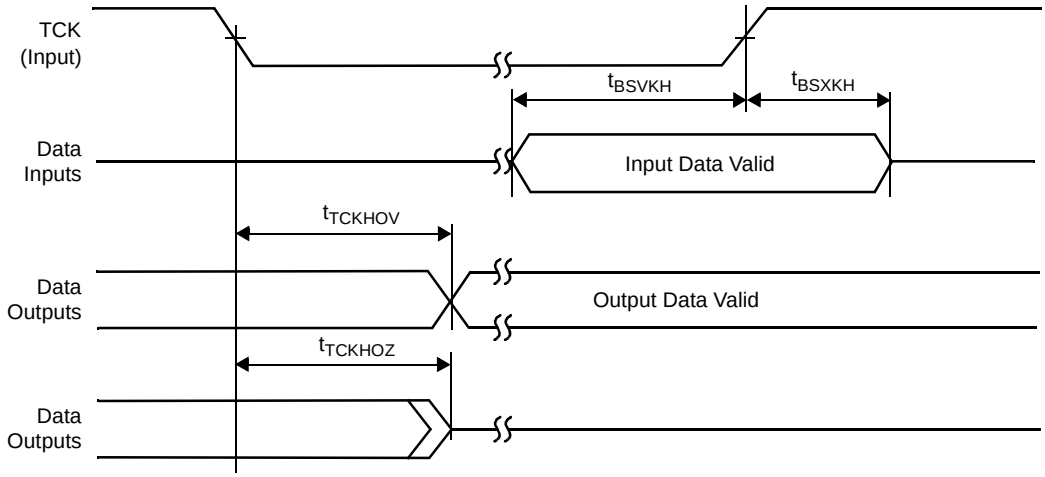


Figure 39. Boundary Scan (JTAG) Timing

Table 58. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required (continued)

Signal Name	Pin Connection
GE1_SGMII_TX	NC
GE1_TD[0-3]	NC
GE1_TX_CLK	GND
GE1_TX_EN	NC
GE1_TX_ER	NC

3.4.4.2 Ethernet Controller 2 (GE2) Related Pins

Note: Table 59 through Table 61 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

3.4.4.2.1 GE2 interface Is Not Used

Table 59 assumes that the GE2 pins are not used for any purpose (including any multiplexed function) and that V_{DDGE2} is tied to GND.

Table 59. Connectivity of GE2 Related Pins When the GE2 Interface Is Not Used

Signal Name	Pin Connection
GE2_RD[0-3]	NC
GE2_RX_CLK	NC
GE2_RX_DV	NC
GE2_RX_ER	NC
GE2_SGMII_RX	GND_{SXC}
$\overline{\text{GE2\_SGMII\_RX}}$	GND_{SXC}
$\overline{\text{GE2\_SGMII\_TX}}$	NC
GE2_SGMII_TX	NC
GE2_TCK	Nc
GE2_TD[0–3]	Nc
GE2_TX_EN	NC

3.4.4.2.2 Subset of GE2 Pins Required

When only a subset of the whole GE2 interface is used, such as for RMII, the unused GE2 pins should be connected as described in Table 60. The table assumes that the unused GE2 pins are not used for any purpose (including any multiplexed functions) and that V_{DDGE2} is tied to either 2.5 V or 3.3 V.

Table 60. Connectivity of GE1 Related Pins When only a subset of the GE1 Interface Is required

Signal Name	Pin Connection
GE2_RD[0-3]	GND
GE2_RX_CLK	GND
GE2_RX_DV	GND
GE2_RX_ER	GND
GE2_SGMII_RX	GND_{SXC}

3.4.8 Miscellaneous Pins

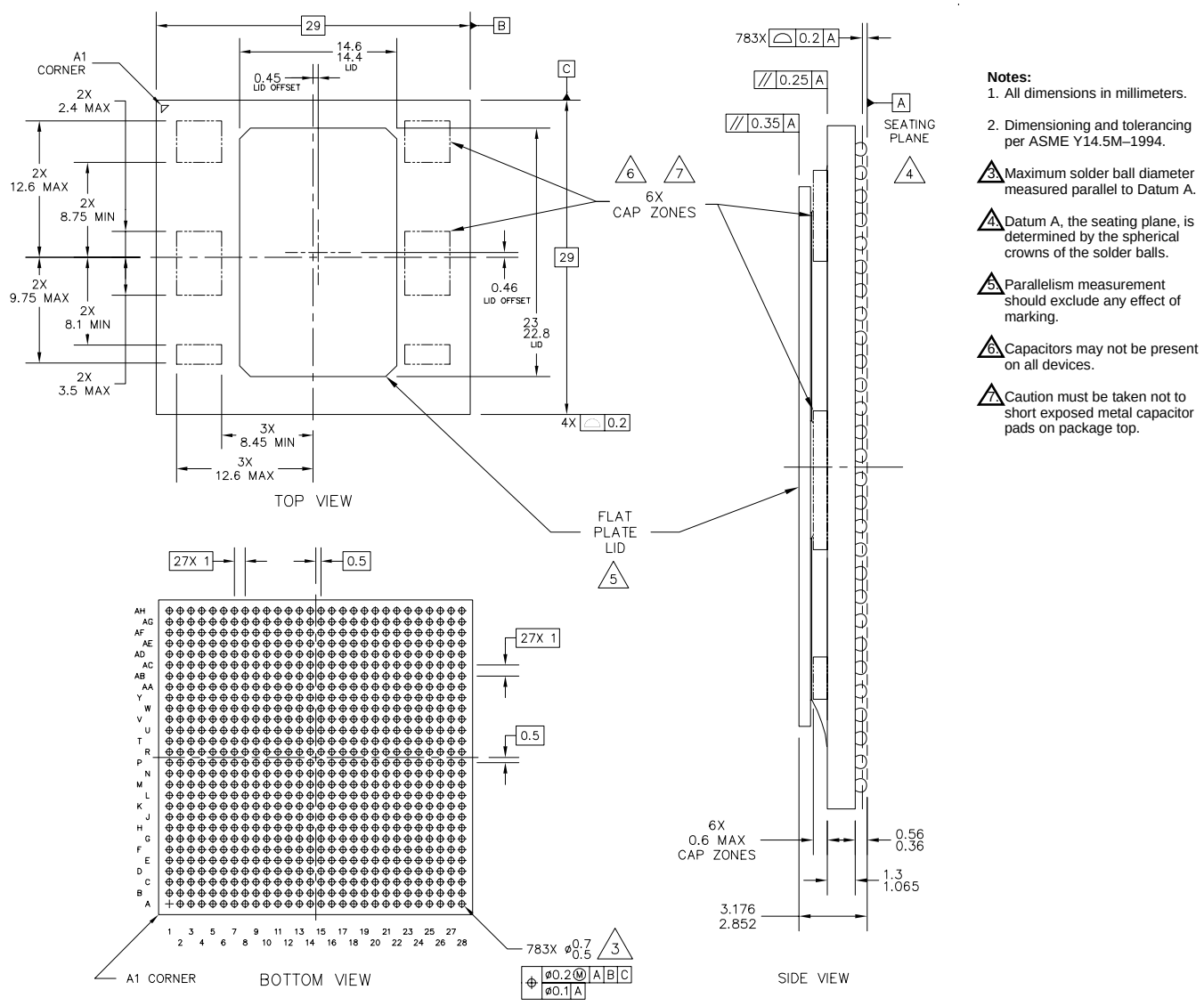
Table 65 lists the board connections for the pins if they are not required by the system design. Table 65 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

Table 65. Connectivity of Individual Pins When They Are Not Required

Signal Name	Pin Connection
CLKOUT	NC
EE0	GND
EE1	NC
GPIO[0–31]	GND
SCL	See the GPIO connectivity guidelines in this table.
SDA	See the GPIO connectivity guidelines in this table.
$\overline{\text{INT\_OUT}}$	NC
$\overline{\text{IRQ}}$[0–15]	See the GPIO connectivity guidelines in this table.
$\overline{\text{NMI}}$	V_{DDIO}
$\overline{\text{NMI\_OUT}}$	NC
RC[0–16]	GND
$\overline{\text{RC\_LDF}}$	NC
STOP_BS	GND
TCK	GND
TDI	GND
TDO	NC
TMR[0–4]	See the GPIO connectivity guidelines in this table.
TMS	GND
$\overline{\text{TRST}}$	GND
URXD	See the GPIO connectivity guidelines in this table.
UTXD	See the GPIO connectivity guidelines in this table.
V_{DDIO}	3.3 V
Note: When using I/O multiplexing mode 5 or 6, tie the TDM7TSYN/PCI_AD4 signal (ball number AC9) to GND.	

Note: For details on configuration, see the *MSC8144 Reference Manual*. For additional information, refer to the *MSC8144 Design Checklist* (AN3202).

5 Package Information



Notes:
1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M–1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement should exclude any effect of marking.
6. Capacitors may not be present on all devices.
7. Caution must be taken not to short exposed metal capacitor pads on package top.

CASE NO. 1842-04

Figure 44. MSC8144 Mechanical Information, 783-ball FC-PBGA Package

6 Product Documentation

- *MSC8144 Technical Data Sheet* (MSC8144). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8144 device.
- *MSC8144 Reference Manual* (MSC8144RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes.* Cover various programming topics related to the StarCore DSP core and the MSC8144 device.
- *SC3400 DSP Core Reference Manual*. Covers the SC3400 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8144 SC3400 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

Table 66 provides a revision history for this data sheet.

Table 66. Document Revision History

Rev.	Date	Description
0	Feb. 2007	• Initial public release.
1	Apr. 2007	• Adds new I/O multiplexing mode 7 that supports POS functionality. • Updates reference voltage supply for pins G5, H7, and H8 in Table 1. • Updates start-up timing recommendations with regard to $\overline{\text{TRST}}$ and $\overline{\text{M3\_RESET}}$ in Section 2.7.1. • Adds input clock duty cycles in Table 20. • Updates PCI AC timings in Table 41. • Removes UTOPIA internal clock specifications in Table 52. • Updates JTAG timings in Table 56. • Clarifies connectivity guidelines for Ethernet pins in Section 3.3.4. • Miscellaneous pin connectivity guidelines were updated in Table 71. • Updates name of core subsystem reference manual.
2	June 2007	• Corrected AA4 definition in Table 1. Changed TDM5TD3 to correct name TDM5TDAT. • Removed Figure 35 because the device does not support UTOPIA using an internal clock. Renumbered subsequent figures. • Removed Section 3.5 *Thermal Considerations*. To be replaced with an application note.
3	Sep 2007	• Updated M3 voltage range in Table 3. • Changed note in Table 7 for PLL power supplies. • DDR voltage designator changed from V_{DD} to V_{DDDDR} in Table 8, Table 10, **Section 2.7.4.1**, **Section 2.7.4.2**, and Figure 11. Changed range on I_{OZ} in Table 8 and Table 10. • Deleted text before Table 13 and added note 2 to input pin capacitance. • Deleted text before Table 14, added a 1 to the note, and added note 1 to input pin capacitance. • Deleted **Section 2.6.5** on page 32 and renumbered subsequent subsections. • Deleted text before new **Section 2.6.5.1**. • Added a 1 to the note in Table 15 and added note 1 to input pin capacitance. • Deleted ac voltage rows from Table 16. Added note 1 to input pin capacitance. • Changed output high and low voltage levels in Table 17 and Table 18. • Deleted text before Table 19. • Added clock skew ranges in percent in Table 21. • Changed V_{REF} to MV_{REF} in Table 26. • Changed V_{DD} to V_{DDIO} in Table 41 Updated note 2. • Added note 4 to Table 42. Changed $t_{TDMSHOX}$ value. • Changed V_{DD} to V_{DDGE} in Figure 27 and Figure 30. • Changed the value of the data to clock out skew in Table 51. • Changed EE pin timing in Table 55. • Changed the head for the JTAG timing section, now **Section 2.7.15**. • Updated JTAG timing for TCK cycle time, TCK high phase, and boundary scan input data hold time in Table 56. • Added new **Section 3.3** with guidelines for board layout for clock and timing signals. Renumbered subsequent sections.
4	Sep 2007	• Changed leakage current values in Table 13, Table 14, Table 11, Table 16, Table 17, Table 18, and Table 19 from –10 and 10 µa to –30 and 30 µa. • Change the minimum value of t_{MDDVKH} in Table 45 from 5 ns to 7 ns. • Updated note 1 in Table 45.
5	Oct 2007	• Corrected column numbering in Figure 3 and Figure 4. • Updated SPI signal names in Table 1.
6	Oct 2007	• Updated SPI signal names in Table 1.