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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	I ² C, IrDA, LINbus, SDIO, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f401ret6

3 Functional overview

3.1 ARM[®] Cortex[®]-M4 with FPU core with embedded Flash and SRAM

The ARM[®] Cortex[®]-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM[®] Cortex[®]-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F401xD/xE devices are compatible with all ARM tools and software.

Figure 3 shows the general block diagram of the STM32F401xD/xE.

Note: Cortex[®]-M4 with FPU is binary compatible with Cortex[®]-M3.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM[®] Cortex[®]-M4 with FPU processors. It balances the inherent performance advantage of the ARM[®] Cortex[®]-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 105 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 84 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.9 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 62 maskable interrupt channels plus the 16 interrupt lines of the Cortex[®]-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.10 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 21 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 81 GPIOs can be connected to the 16 external interrupt lines.

3.11 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 84 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 84 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLL12S) which allows to achieve audio class performance. In this case, the I²S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.12 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using either USART1(PA9/10), USART2(PD5/6), USB OTG FS in device mode (PA11/12) through DFU (device firmware upgrade), I2C1(PB6/7), I2C2(PB10/3), I2C3(PA8/PB4), SPI1(PA4/5/6/7), SPI2(PB12/13/14/15) or SPI3(PA15, PC10/11/12).

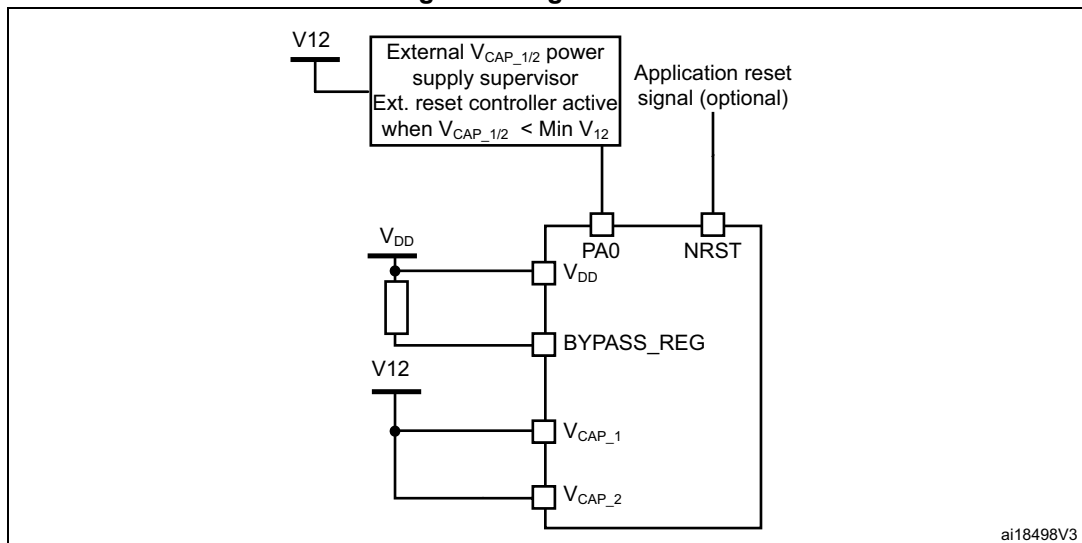
For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

3.13 Power supply schemes

- $V_{DD} = 1.7$ to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through V_{DD} pins. Requires the use of an external power supply supervisor connected to the V_{DD} and PDR_ON pins.
- $V_{DD} = 1.8$ to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 1.7$ to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively, with decoupling technique.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to [Figure 18: Power supply scheme](#) for more details.

Figure 7. Regulator OFF



The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see [Figure 8](#)).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see [Figure 9](#)).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

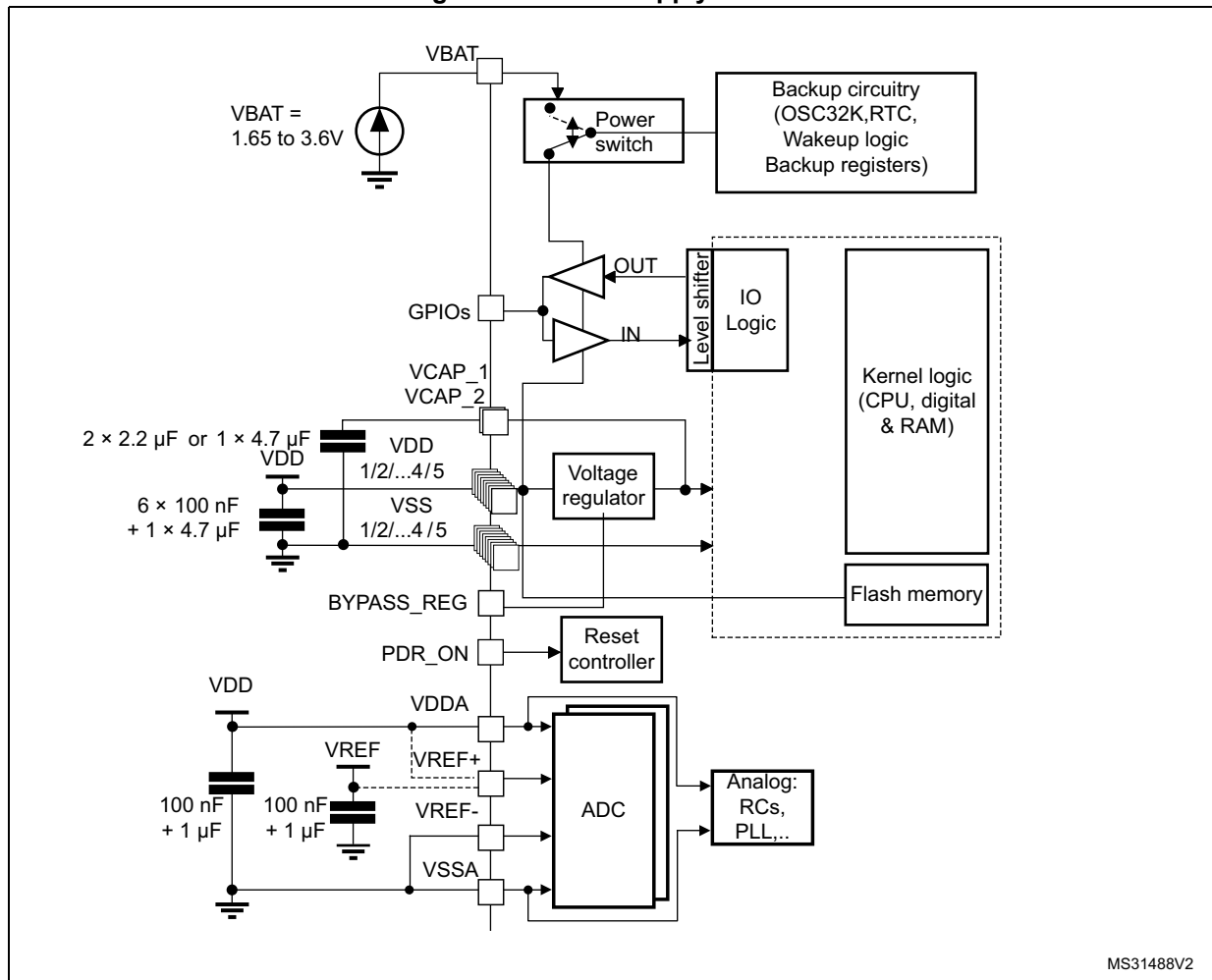
Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application

Table 9. Alternate function mapping (continued)

Port	AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_FS		SDIO			
Port D	PD0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	-	SDIO_ CMD	-	-	EVENT OUT
	PD3	-	-	-	-	SPI2_SCK/ I2S2_CK	-	USART2_ CTS	--	-	-	-	-	-	-	EVENT OUT
	PD4	-	-	-	-	-	-	USART2_ RTS		-	-	-	-	-	-	EVENT OUT
	PD5	-	-	-	-	-	-	USART2_ TX	-	-	-	-	-	-	-	EVENT OUT
	PD6	-	-	-	-	SPI3_MOSI/ I2S3_SD	-	USART2_ RX	-	-	-	-	-	-	-	EVENT OUT
	PD7	-	-	-	-	-	-	USART2_ CK	-	-	-	-	-	-	-	EVENT OUT
	PD8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD12	-	-	TIM4_CH1	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

6.1.6 Power supply scheme

Figure 18. Power supply scheme

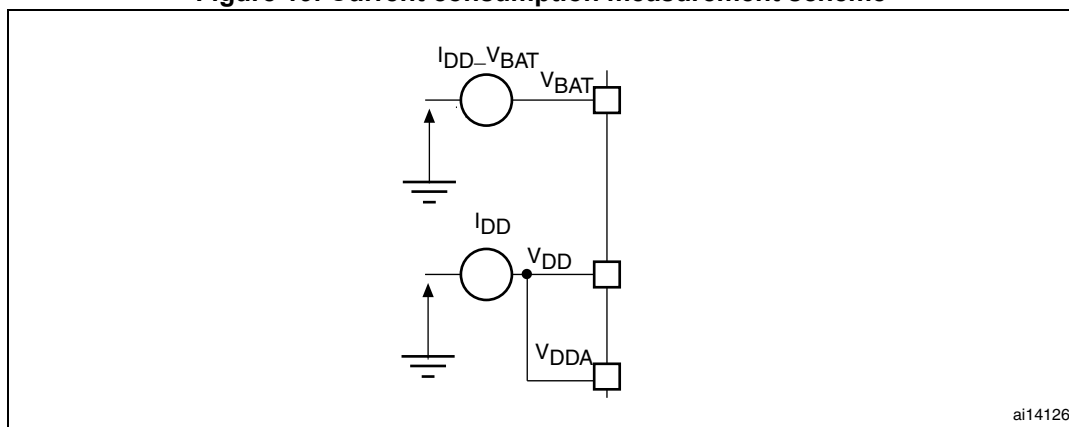


1. To connect PDR_ON pin, refer to [Section 3.14: Power supply supervisor](#).
2. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
3. V_{CAP_2} pad is only available on LQFP100 and UFBGA100 packages.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 19. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 11: Voltage characteristics](#), [Table 12: Current characteristics](#), and [Table 13: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD-VSS}	External main supply voltage (including V_{DDA} , V_{DD} and V_{BAT}) ⁽¹⁾	-0.3	4.0	V
V_{IN}	Input voltage on FT pins ⁽²⁾	$V_{SS}-0.3$	$V_{DD}+4.0$	
	Input voltage on any other pin	$V_{SS}-0.3$	4.0	
	Input voltage for BOOT0	V_{SS}	9.0	mV
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	
$ V_{SSx}-V_{SS} $	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.14: Absolute maximum ratings (electrical sensitivity)		

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to [Table 12](#) for the values of the maximum allowed injected current.

Table 14. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _A	Ambient temperature for 6 suffix version	Maximum power dissipation	-40	-	85	°C
		Low power dissipation ⁽⁸⁾	-40	-	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	-40	-	105	
		Low power dissipation ⁽⁸⁾	-40	-	125	
T _J	Junction temperature range	6 suffix version	-40	-	105	
		7 suffix version	-40	-	125	

1. V_{DD}/V_{DDA} minimum value of 1.7 V with the use of an external power supply supervisor (refer to [Section 3.14.2: Internal reset OFF](#)).
2. When the ADC is used, refer to [Table 66: ADC characteristics](#).
3. If V_{REF+} pin is present, it must respect the following condition: V_{DDA}-V_{REF+} < 1.2 V.
4. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
5. Guaranteed by test in production
6. To sustain a voltage higher than V_{DD}+0.3, the internal Pull-up and Pull-Down resistors must be disabled
7. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
8. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

Table 15. Features depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states (f _{Flashmax})	Maximum Flash memory access frequency with wait states ⁽¹⁾⁽²⁾	I/O operation	Clock output frequency on I/O pins ⁽³⁾	Possible Flash memory operations
V _{DD} = 1.7 to 2.1 V ⁽⁴⁾	Conversion time up to 1.2 Msps	20 MHz ⁽⁵⁾	84 MHz with 4 wait states	- No I/O compensation	up to 30 MHz	8-bit erase and program operations only
V _{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	22 MHz	84 MHz with 3 wait states	- No I/O compensation	up to 30 MHz	16-bit erase and program operations
V _{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	84 MHz with 3 wait states	- I/O compensation works	up to 48 MHz	16-bit erase and program operations
V _{DD} = 2.7 to 3.6 V ⁽⁶⁾	Conversion time up to 2.4 Msps	30 MHz	84 MHz with 2 wait states	- I/O compensation works	- up to 84 MHz when V _{DD} = 3.0 to 3.6 V - up to 48 MHz when V _{DD} = 2.7 to 3.0 V	32-bit erase and program operations

Table 33. Peripheral current consumption (continued)

Peripheral		I _{DD} (typ)	Unit
APB2 (up to 84MHz)	TIM1	5.71	μA/MHz
	TIM9	2.86	
	TIM10	1.79	
	TIM11	2.02	
	ADC1 ⁽²⁾	2.98	
	SPI1	1.19	
	USART1	3.10	
	USART6	2.86	
	SDIO	5.95	
	SPI4	1.31	
	SYSCFG	0.71	

1. I2SMOD bit set in SPI_I2SCFGR register, and then the I2SE bit set to enable I2S peripheral.
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

6.3.7 Wakeup time from low-power modes

The wakeup times given in [Table 34](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 34. Low-power mode wakeup timings⁽¹⁾

Symbol	Parameter	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
t _{WUSLEEP} ⁽²⁾	Wakeup from Sleep mode	-	4	6	CPU clock cycle
t _{WUSTOP} ⁽²⁾	Wakeup from Stop mode, usage of main regulator	-	13.5	14.5	μs
	Wakeup from Stop mode, usage of main regulator, Flash memory in Deep power down mode	-	105	111	
	Wakeup from Stop mode, regulator in low power mode	-	21	33	
	Wakeup from Stop mode, regulator in low power mode, Flash memory in Deep power down mode	-	113	130	
t _{WUSTDBY} ⁽²⁾⁽³⁾	Wakeup from Standby mode	-	314	407	μs

1. Guaranteed by characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. t_{WUSTDBY} maximum value is given at -40 °C.

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 54](#). However, the recommended clock input waveform is shown in [Figure 22](#).

The characteristics given in [Table 35](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 14](#).

Table 35. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency ⁽¹⁾		1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time ⁽¹⁾		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time ⁽¹⁾		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance ⁽¹⁾		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

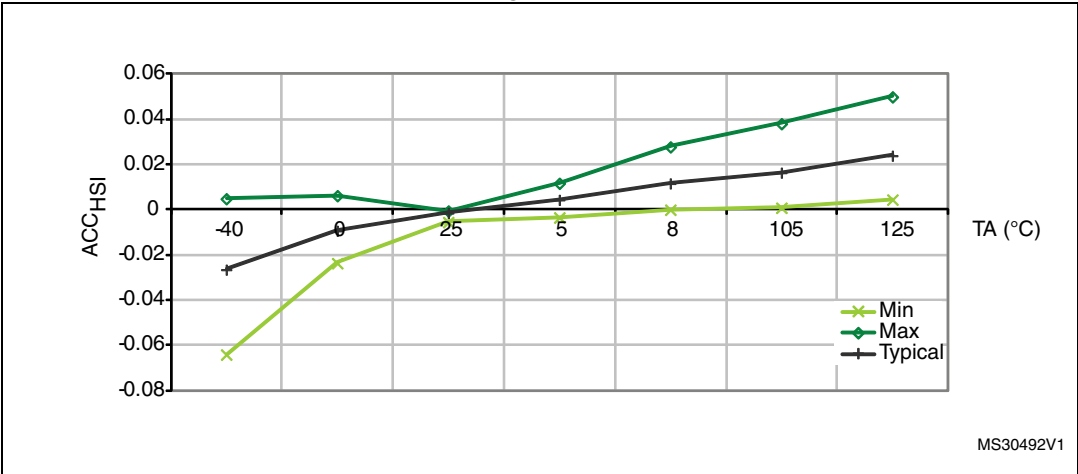
1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 54](#). However, the recommended clock input waveform is shown in [Figure 23](#).

The characteristics given in [Table 36](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 14](#).

Figure 26. ACC_{HSI} versus temperature



1. Guaranteed by characterization, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 40. LSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(2)}$	Frequency	17	32	47	kHz
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	15	40	μs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	0.4	0.6	μA

1. $V_{DD} = 3 V$, $T_A = -40$ to $105\text{ }^{\circ}C$ unless otherwise specified.

2. Guaranteed by characterization, not tested in production.

3. Guaranteed by design, not tested in production.

Table 53. I/O current injection susceptibility⁽¹⁾

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0 pin	-0	NA	mA
	Injected current on NRST pin	-0	NA	
	Injected current on PB3, PB4, PB5, PB6, PB7, PB8, PB9, PC13, PC14, PC15, PH1, PDR_ON, PC0, PC1, PC2, PC3, PD1, PD5, PD6, PD7, PE0, PE2, PE3, PE4, PE5, PE6	-0	NA	
	Injected current on any other FT pin	-5	NA	
	Injected current on any other pins	-5	+5	

1. NA = not applicable.

Note: *It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 54](#) are derived from tests performed under the conditions summarized in [Table 14](#). All I/Os are CMOS and TTL compliant.

Table 54. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IL}	FT, and NRST I/O input low level voltage	1.7 V≤V _{DD} ≤3.6 V	-	-	0.35V _{DD} −0.04 ⁽¹⁾	V
					0.3V _{DD} ⁽²⁾	
	BOOT0 I/O input low level voltage	1.75 V≤V _{DD} ≤3.6 V, −40 °C≤T _A ≤105 °C	-	-	0.1V _{DD} +0.1	
		1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤105 °C	-	-		
V _{IH}	FT and NRST I/O input high level voltage ⁽⁵⁾	1.7 V≤V _{DD} ≤3.6 V	0.45V _{DD} +0.3 ⁽¹⁾	-	-	V
			0.4V _{DD} ⁽²⁾			
	BOOT0 I/O input high level voltage	1.75 V≤V _{DD} ≤3.6 V, −40 °C≤T _A ≤105 °C	0.17V _{DD} +0.7 ⁽¹⁾	-	-	
		1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤105 °C				

Table 55. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$1.3^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-1.3^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +6 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(5)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4^{(5)}$	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 12](#), and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 12](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Guaranteed by characterization results, not tested in production.
5. Guaranteed by design, not tested in production..

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 31](#) and , respectively.

Unless otherwise specified, the parameters given in [Table 56](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 56. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(I/O)out}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	4	
	$t_{f(I/O)out}/$ $t_{r(I/O)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} = 1.7 \text{ V to}$ 3.6 V	-	-	100	ns

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present.

The I²C characteristics are described in [Table 59](#). Refer also to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative.

Table 59. I²C characteristics

Symbol	Parameter	Standard mode I ² C ⁽¹⁾		Fast mode I ² C ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	
t _w (SCLL)	SCL clock low time	4.7	-	1.3	-	μs
t _w (SCLH)	SCL clock high time	4.0	-	0.6	-	
t _{su} (SDA)	SDA setup time	250	-	100	-	ns
t _h (SDA)	SDA data hold time	0	-	0	900 ⁽³⁾	
t _r (SDA) t _r (SCL)	SDA and SCL rise time	-	1000		300	
t _f (SDA) t _f (SCL)	SDA and SCL fall time	-	300	-	300	
t _h (STA)	Start condition hold time	4.0	-	0.6	-	μs
t _{su} (STA)	Repeated Start condition setup time	4.7	-	0.6	-	
t _{su} (STO)	Stop condition setup time	4.0	-	0.6	-	μs
t _w (STO:STA)	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
C _b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{CLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.

I²S interface characteristics

Unless otherwise specified, the parameters given in [Table 62](#) for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 14](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 62. I²S dynamic characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256x F_s ⁽²⁾	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64x F_s	MHz
		Slave data: 32 bits	-	64x F_s	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	6	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	7.5	-	
$t_{su(SD_SR)}$		Slave receiver	2	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD_SR)}$		Slave receiver	0	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	27	
$t_{h(SD_ST)}$		Master transmitter (after enable edge)	-	20	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	20	
$t_{h(SD_MT)}$	Data output hold time	Master transmitter (after enable edge)	2.5	-	

1. Guaranteed by characterization, not tested in production.

2. The maximum value of 256x F_s is 42 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of the reference manual for more details on the sampling frequency (F_s).

f_{MCK} , f_{CK} , and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of $(I2SDIV/(2*I2SDIV+ODD))$ and a maximum value of $(I2SDIV+ODD)/(2*I2SDIV+ODD)$. F_s maximum value is supported for each mode/condition.

Table 66. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{lat}^{(2)}$	Injection trigger conversion latency	$f_{ADC} = 30\text{ MHz}$	-	-	0.100	μs
			-	-	3 ⁽⁵⁾	$1/f_{ADC}$
$t_{latr}^{(2)}$	Regular trigger conversion latency	$f_{ADC} = 30\text{ MHz}$	-	-	0.067	μs
			-	-	2 ⁽⁵⁾	$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	$f_{ADC} = 30\text{ MHz}$	0.100	-	16	μs
			3	-	480	$1/f_{ADC}$
$t_{STAB}^{(2)}$	Power-up time		-	2	3	μs
$t_{CONV}^{(2)}$	Total conversion time (including sampling time)	$f_{ADC} = 30\text{ MHz}$ 12-bit resolution	0.50	-	16.40	μs
		$f_{ADC} = 30\text{ MHz}$ 10-bit resolution	0.43	-	16.34	μs
		$f_{ADC} = 30\text{ MHz}$ 8-bit resolution	0.37	-	16.27	μs
		$f_{ADC} = 30\text{ MHz}$ 6-bit resolution	0.30	-	16.20	μs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$
$f_S^{(2)}$	Sampling rate ($f_{ADC} = 30\text{ MHz}$, and $t_S = 3\text{ ADC cycles}$)	12-bit resolution Single ADC	-	-	2	Msp/s
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msp/s
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msp/s
$I_{VREF+}^{(2)}$	ADC V_{REF} DC current consumption in conversion mode		-	300	500	μA
$I_{VDDA}^{(2)}$	ADC V_{DDA} DC current consumption in conversion mode		-	1.6	1.8	mA

- V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to [Section 3.14.2: Internal reset OFF](#)).
- Guaranteed by characterization, not tested in production.
- V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA} .
- R_{ADC} maximum value is given for $V_{DD}=1.7\text{ V}$, and minimum value for $V_{DD}=3.3\text{ V}$.
- For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in [Table 66](#).

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0,5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

6.3.21 Temperature sensor characteristics

Table 72. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	-	2.5	-	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	-	0.76	-	V
$t_{START}^{(2)}$	Startup time	-	6	10	μs
$T_{S_temp}^{(2)}$	ADC sampling time when reading the temperature (1 $^{\circ}\text{C}$ accuracy)	10	-	-	μs

1. Guaranteed by characterization, not tested in production.

2. Guaranteed by design, not tested in production.

Table 73. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 $^{\circ}\text{C}$, $V_{DDA} = 3.3\text{ V}$	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 $^{\circ}\text{C}$, $V_{DDA} = 3.3\text{ V}$	0x1FFF 7A2E - 0x1FFF 7A2F

6.3.22 V_{BAT} monitoring characteristics

Table 74. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	K Ω
Q	Ratio on V_{BAT} measurement	-	4	-	
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$T_{S_vbat}^{(2)(2)}$	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	μs

1. Guaranteed by design, not tested in production.

2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.23 Embedded reference voltage

The parameters given in [Table 75](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 75. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.18	1.21	1.24	V
$T_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	10	-	-	μs
$V_{RERINT_s}^{(2)}$	Internal reference voltage spread over the temperature range	$V_{DD} = 3\text{ V} \pm 10\text{ mV}$	-	3	5	mV

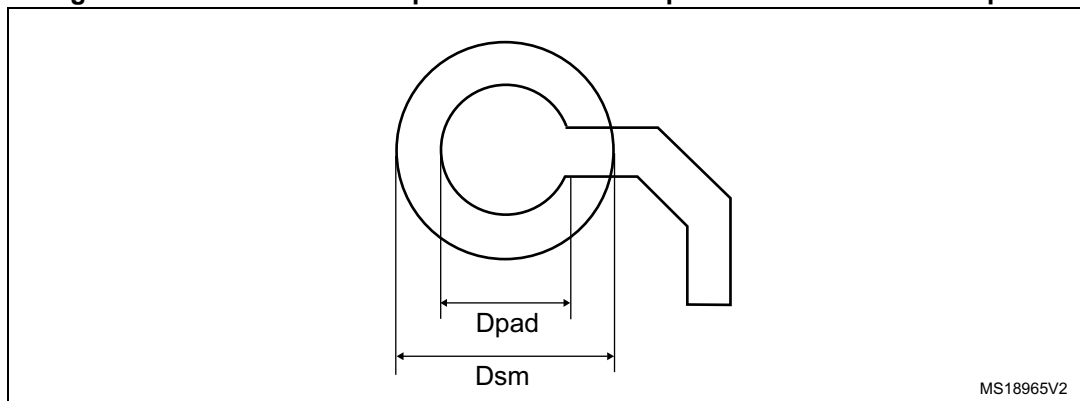
Table 79. STM32F401xCE WLCSP49 wafer level chip size package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
b ⁽³⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.994	3.029	3.064	0.1179	0.1193	0.1206
E	2.994	3.029	3.064	0.1179	0.1193	0.1206
e	-	0.400	-	-	0.0157	-
e1	-	2.400	-	-	0.0945	-
e2	-	2.400	-	-	0.0945	-
F	-	0.3145	-	-	0.0124	-
G	-	0.3145	-	-	0.0124	-
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

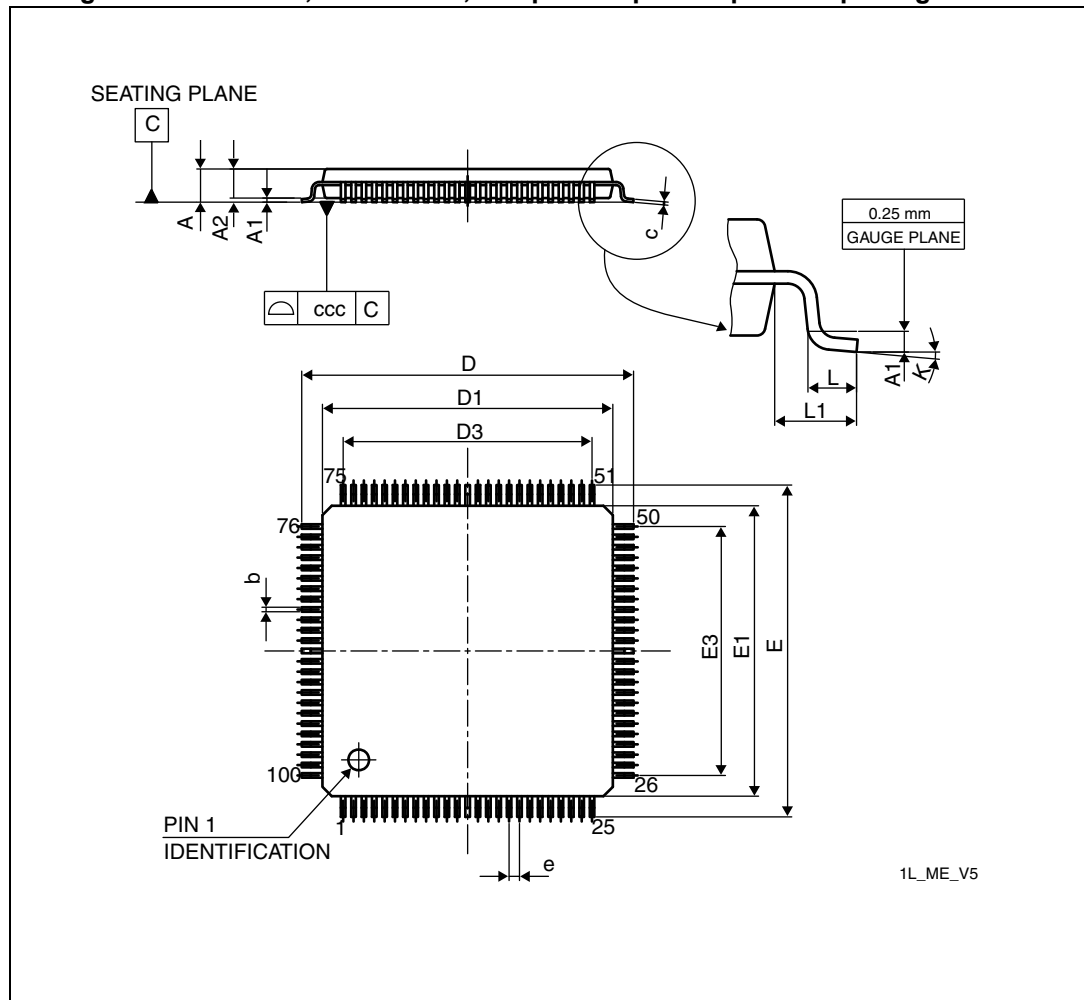
2. Back side coating

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 47. WLCSP49 0.4 mm pitch wafer level chip size recommended footprint

7.1.4 LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package

Figure 55. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

8 Part numbering

Table 86. Ordering information scheme

Example:	STM32	F	401	C	E	Y	6	TR
Device family								
STM32 = ARM-based 32-bit microcontroller								
Product type								
F = General-purpose								
Device subfamily								
401 = 401 family								
Pin count								
C = 48/49 pins								
R = 64 pins								
V = 100 pins								
Flash memory size								
D = 384 Kbytes of Flash memory								
E = 512 Kbytes of Flash memory								
Package								
H = UFBGA								
T = LQFP								
U = UFQFPN								
Y = WLCSP								
Temperature range								
6 = Industrial temperature range, –40 to 85 °C								
Packing								
TR = tape and reel								
No character = tray or tube								