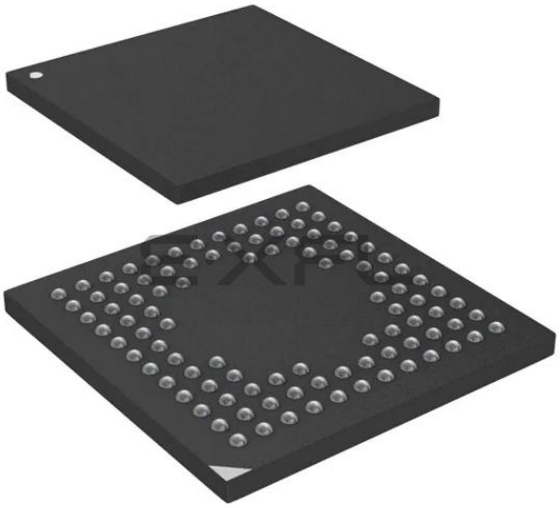

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 84MHz |
| Connectivity | I²C, IrDA, LINbus, SDIO, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 81 |
| Program Memory Size | 512KB (512K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-UFBGA |
| Supplier Device Package | 100-UFBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f401veh6 |

# List of figures

# 1 Introduction

This datasheet provides the description of the STM32F401xD/xE line of microcontrollers.

The STM32F401xD/xE datasheet should be read in conjunction with RM0368 reference manual which is available from the STMicroelectronics website *www.st.com*. It includes all information concerning Flash memory programming.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

## 2.1 Compatibility with STM32F4 series

The STM32F401xD/xE are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F401xD/xE can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

**Figure 1. Compatible board design for LQFP100 package**

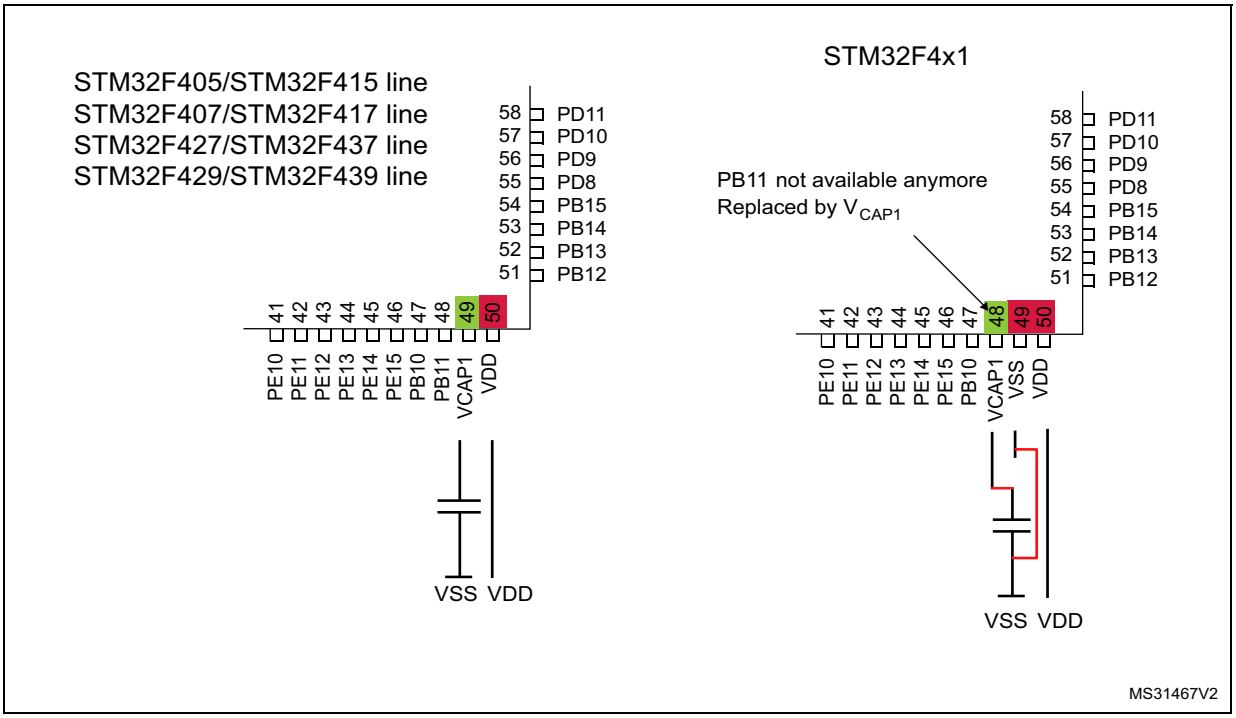
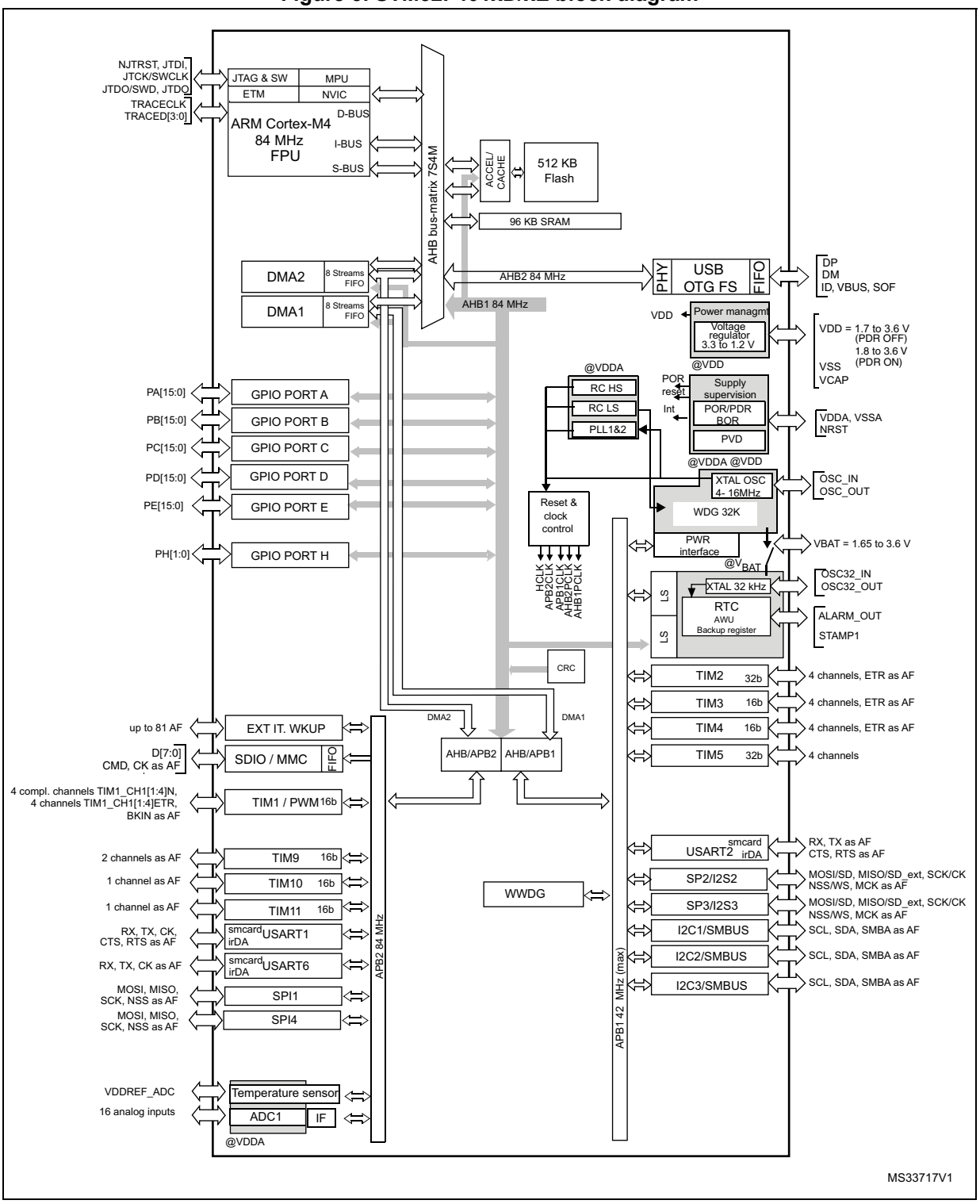


**Figure 3. STM32F401xD/xE block diagram**




1. The timers connected to APB2 are clocked from TIMxCLK up to 84 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 42 MHz.

### 3.15.3 Regulator ON/OFF and internal power supply supervisor availability

**Table 3. Regulator ON/OFF and internal power supply supervisor availability**

| Package | Regulator ON | Regulator OFF | Power supply supervisor ON | Power supply supervisor OFF |
|---|---|---|---|---|
| UFQFPN48 | Yes | No | Yes | No |
| WLCSP49 | Yes | No | Yes<br>PDR_ON set to VDD | Yes<br>PDR_ON external control(1) |
| LQFP64 | Yes | No | Yes | No |
| LQFP100 | Yes | No | Yes | No |
| UFBGA100 | Yes<br>BYPASS_REG set to VSS | Yes<br>BYPASS_REG set to VDD | Yes<br>PDR_ON set to VDD | Yes<br>PDR_ON external control (1) |

1. Refer to *Section 3.14: Power supply supervisor*

## 3.16 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC features a reference clock detection, a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 bytes of user application data when $V_{DD}$ power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.17: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

### 3.19.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 3.20 Inter-integrated circuit interface ($I^2C$)

Up to three $I^2C$ bus interfaces can operate in multimaster and slave modes. They can support the standard (up to 100 kHz) and fast (up to 400 kHz) modes. The I2C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative.They also support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 5*).

**Table 5. Comparison of I2C analog and digital filters**

| | Analog filter | Digital filter |
|---|---|---|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2C peripheral clocks |

## 3.21 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART6).

These three interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 10.5 Mbit/s. The USART2 interface communicates at up to 5.25 bit/s.

USART1 and USART2 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 6. USART feature comparison

| USART name | Standard features | Modem (RTS/CTS) | LIN | SPI master | irDA | Smartcard (ISO 7816) | Max. baud rate in Mbit/s (oversampling by 16) | Max. baud rate in Mbit/s (oversampling by 8) | APB mapping |
|---|---|---|---|---|---|---|---|---|---|
| USART1 | X | X | X | X | X | X | 5.25 | 10.5 | APB2 (max. 84 MHz) |
| USART2 | X | X | X | X | X | X | 2.62 | 5.25 | APB1 (max. 42 MHz) |
| USART6 | X | N.A | X | X | X | X | 5.25 | 10.5 | APB2 (max. 84 MHz) |

## 3.22 Serial peripheral interface (SPI)

The devices feature up to four SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 and SPI4 can communicate at up to 42 Mbit/s, SPI2 and SPI3 can communicate at up to 21 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

## 3.23 Inter-integrated sound ($I^2S$)

Two standard $I^2S$ interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All $I^2Sx$ can be served by the DMA controller.

## 3.24 Audio PLL (PLLI2S)

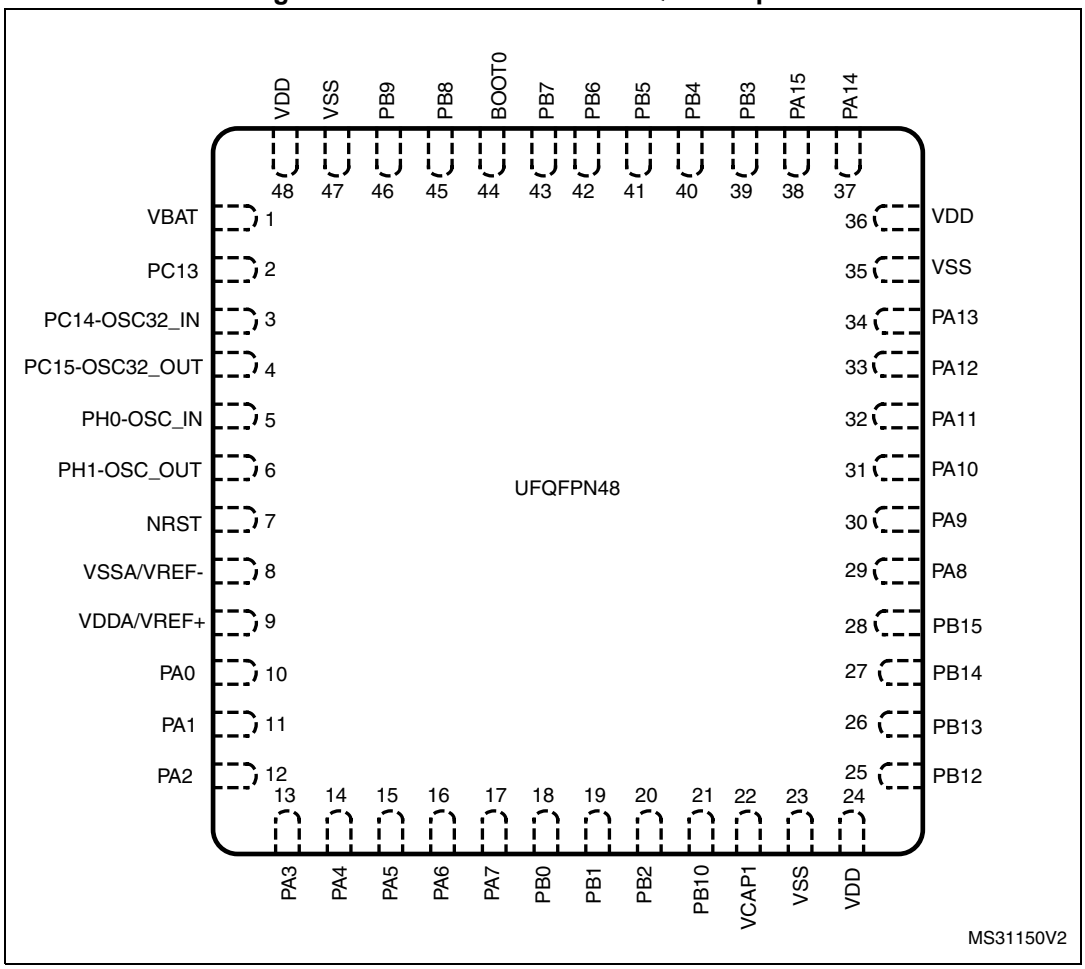
The devices feature an additional dedicated PLL for audio $I^2S$ application. It allows to achieve error-free $I^2S$ sampling clock accuracy without compromising on the CPU performance.

The PLLI2S configuration can be modified to manage an $I^2S$ sample rate change without disabling the main PLL (PLL) used for the CPU.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 kHz to 192 kHz.

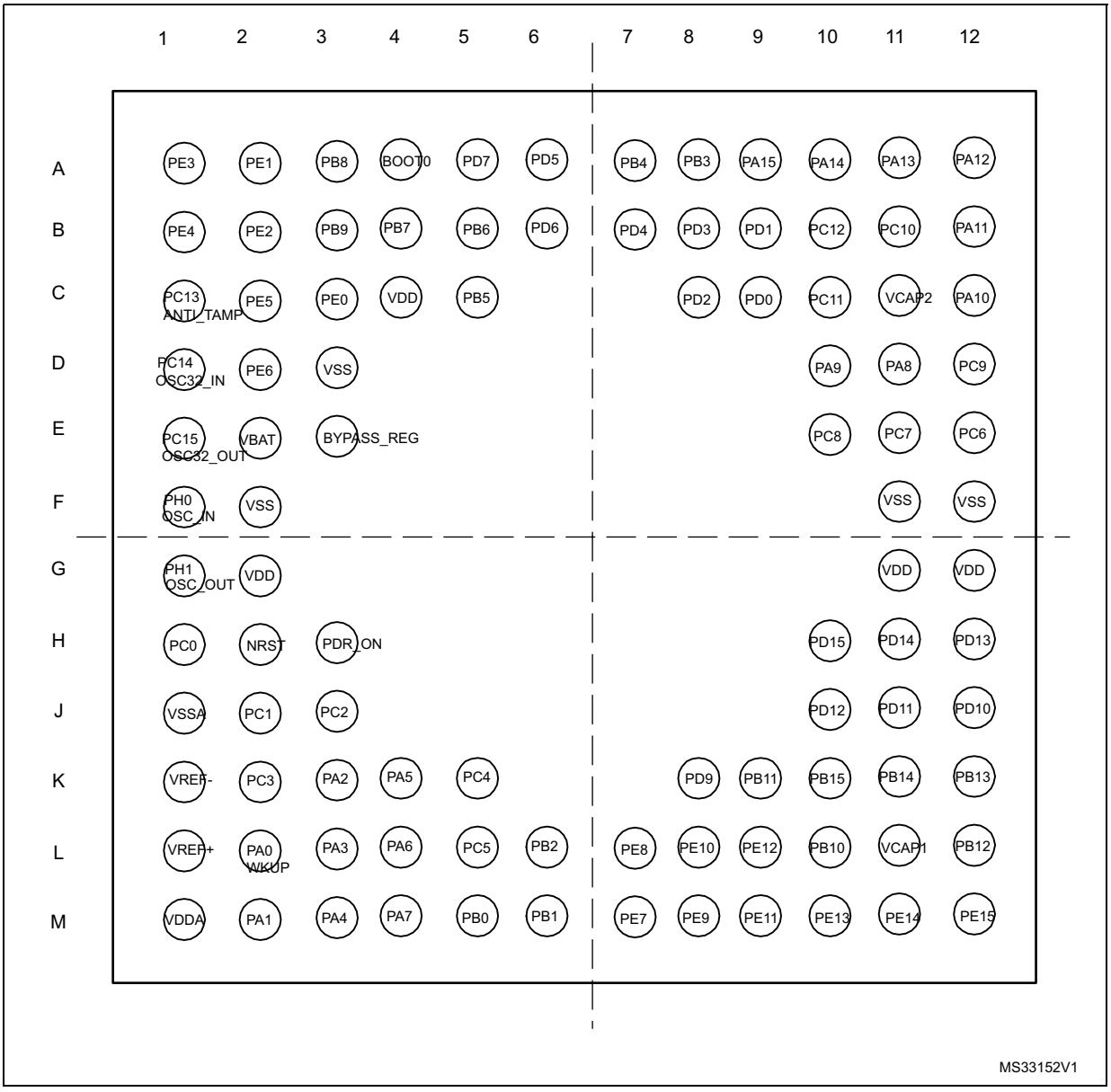
In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

**Figure 11. STM32F401xD/xE UFQFPN48 pinout**




1. The above figure shows the package top view.

**Figure 14. STM32F401xD/xE UFBGA100 pinout**




1. This figure shows the package top view

Table 8. STM32F401xD/xE pin definitions (continued)

| Pin Number | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| UQFN48 | WLCSP49 | LQFP64 | LQFP100 | UFBGA100 | | | | | | |
| 13 | E4 | 17 | 26 | L3 | PA3 | I/O | FT | - | USART2_RX, TIM2_CH4, TIM5_CH4, TIM9_CH2, EVENTOUT | ADC1_IN3 |
| - | - | 18 | 27 | - | VSS | S | - | - | - | - |
| - | - | 19 | 28 | - | VDD | S | - | - | - | - |
| - | - | - | - | E3 | BYPASS_ REG | I | FT | - | - | - |
| 14 | G6 | 20 | 29 | M3 | PA4 | I/O | FT | - | SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT | ADC1_IN4 |
| 15 | F5 | 21 | 30 | K4 | PA5 | I/O | FT | - | SPI1_SCK, TIM2_CH1/TIM2_ETR, EVENTOUT | ADC1_IN5 |
| 16 | F4 | 22 | 31 | L4 | PA6 | I/O | FT | - | SPI1_MISO, TIM1_BKIN, TIM3_CH1, EVENTOUT | ADC1_IN6 |
| 17 | F3 | 23 | 32 | M4 | PA7 | I/O | FT | - | SPI1_MOSI, TIM1_CH1N, TIM3_CH2, EVENTOUT | ADC1_IN7 |
| - | - | 24 | 33 | K5 | PC4 | I/O | FT | - | EVENTOUT | ADC1_IN14 |
| - | - | 25 | 34 | L5 | PC5 | I/O | FT | - | EVENTOUT | ADC1_IN15 |
| 18 | G5 | 26 | 35 | M5 | PB0 | I/O | FT | - | TIM1_CH2N, TIM3_CH3, EVENTOUT | ADC1_IN8 |
| 19 | G4 | 27 | 36 | M6 | PB1 | I/O | FT | - | TIM1_CH3N, TIM3_CH4, EVENTOUT | ADC1_IN9 |
| 20 | G3 | 28 | 37 | L6 | PB2 | I/O | FT | - | EVENTOUT | BOOT1 |
| - | - | - | 38 | M7 | PE7 | I/O | FT | - | TIM1_ETR, EVENTOUT | - |
| - | - | - | 39 | L7 | PE8 | I/O | FT | - | TIM1_CH1N, EVENTOUT | - |
| - | - | - | 40 | M8 | PE9 | I/O | FT | - | TIM1_CH1, EVENTOUT | - |
| - | - | - | 41 | L8 | PE10 | I/O | FT | - | TIM1_CH2N, EVENTOUT | - |
| - | - | - | 42 | M9 | PE11 | I/O | FT | - | SPI4_NSS, TIM1_CH2, EVENTOUT | - |
| - | - | - | 43 | L9 | PE12 | I/O | FT | - | SPI4_SCK, TIM1_CH3N, EVENTOUT | - |
| - | - | - | 44 | M10 | PE13 | I/O | FT | - | SPI4_MISO, TIM1_CH3, EVENTOUT | - |

Table 8. STM32F401xD/xE pin definitions (continued)

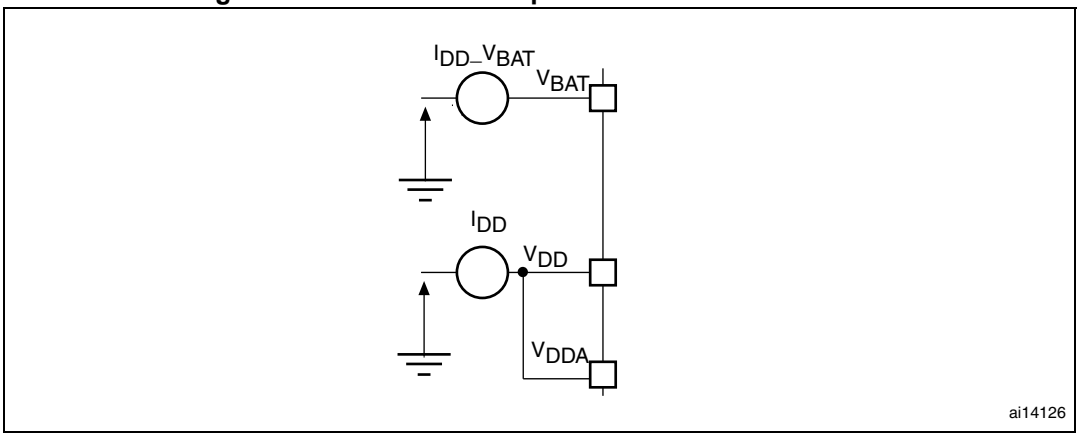
| Pin Number | | | | | Pin name (function after reset)[1] | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| UQFN48 | WLCSP49 | LQFP64 | LQFP100 | UFBGA100 | | | | | | |
| - | - | - | 82 | B9 | PD1 | I/O | FT | - | EVENTOUT | - |
| - | - | 54 | 83 | C8 | PD2 | I/O | FT | - | TIM3_ETR, SDIO_CMD, EVENTOUT | - |
| - | - | - | 84 | B8 | PD3 | I/O | FT | - | SPI2_SCK/I2S2_CK, USART2_CTS, EVENTOUT | - |
| - | - | - | 85 | B7 | PD4 | I/O | FT | - | USART2_RTS, EVENTOUT | - |
| - | - | - | 86 | A6 | PD5 | I/O | FT | - | USART2_TX, EVENTOUT | - |
| - | - | - | 87 | B6 | PD6 | I/O | FT | - | SPI3_MOSI/I2S3_SD, USART2_RX, EVENTOUT | - |
| - | - | - | 88 | A5 | PD7 | I/O | FT | - | USART2_CK, EVENTOUT | - |
| 39 | A3 | 55 | 89 | A8 | PB3 (JTDO-SWO) | I/O | FT | - | JTDO-SWO, SPI1_SCK, SPI3_SCK/I2S3_CK, I2C2_SDA, TIM2_CH2, EVENTOUT | - |
| 40 | A4 | 56 | 90 | A7 | PB4 (NJTRST) | I/O | FT | - | NJTRST, SPI1_MISO, SPI3_MISO, I2S3ext_SD, I2C3_SDA, TIM3_CH1, EVENTOUT | - |
| 41 | B4 | 57 | 91 | C5 | PB5 | I/O | FT | - | SPI1_MOSI, SPI3_MOSI/I2S3_SD, I2C1_SMBA, TIM3_CH2, EVENTOUT | - |
| 42 | C4 | 58 | 92 | B5 | PB6 | I/O | FT | - | I2C1_SCL, USART1_TX, TIM4_CH1, EVENTOUT | - |
| 43 | D4 | 59 | 93 | B4 | PB7 | I/O | FT | - | I2C1_SDA, USART1_RX, TIM4_CH2, EVENTOUT | - |
| 44 | A5 | 60 | 94 | A4 | BOOT0 | I | B | - | - | $V_{PP}$ |
| 45 | B5 | 61 | 95 | A3 | PB8 | I/O | FT | - | I2C1_SCL, TIM4_CH3, TIM10_CH1, SDIO_D4, EVENTOUT | - |
| 46 | C5 | 62 | 96 | B3 | PB9 | I/O | FT | - | SPI2_NSS/I2S2_WS, I2C1_SDA, TIM4_CH4, TIM11_CH1, SDIO_D5, EVENTOUT | - |
| - | - | - | 97 | C3 | PE0 | I/O | FT | - | TIM4_ETR, EVENTOUT | - |
| - | - | - | 98 | A2 | PE1 | I/O | FT | - | EVENTOUT | - |

**Table 10. STM32F401xD register boundary addresses**

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0xE010 0000 - 0xFFFF FFFF | Reserved |
| Cortex®-M4 | 0xE000 0000 - 0xE00F FFFF | Cortex-M4 internal peripherals |
| | 0x5004 0000 - 0xDFFF FFFF | Reserved |
| AHB2 | 0x5000 0000 - 0x5003 FFFF | USB OTG FS |
| AHB1 | 0x4002 6800 - 0x4FFF FFFF | Reserved |
| | 0x4002 6400 - 0x4002 67FF | DMA2 |
| | 0x4002 6000 - 0x4002 63FF | DMA1 |
| | 0x4002 5000 - 0x4002 4FFF | Reserved |
| | 0x4002 3C00 - 0x4002 3FFF | Flash interface register |
| | 0x4002 3800 - 0x4002 3BFF | RCC |
| | 0x4002 3400 - 0x4002 37FF | Reserved |
| | 0x4002 3000 - 0x4002 33FF | CRC |
| | 0x4002 2000 - 0x4002 2FFF | Reserved |
| | 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| | 0x4002 1400 - 0x4002 1BFF | Reserved |
| | 0x4002 1000 - 0x4002 13FF | GPIOE |
| | 0x4002 0C00 - 0x4002 0FFF | GPIOD |
| | 0x4002 0800 - 0x4002 0BFF | GPIOC |
| | 0x4002 0400 - 0x4002 07FF | GPIOB |
| | 0x4002 0000 - 0x4002 03FF | GPIOA |

### 6.1.7 Current consumption measurement

**Figure 19. Current consumption measurement scheme**




## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 11. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | External main supply voltage (including $V_{DDA}$, $V_{DD}$ and $V_{BAT}$)(1) | –0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on FT pins(2) | $V_{SS}$–0.3 | $V_{DD}$+4.0 | |
| | Input voltage on any other pin | $V_{SS}$–0.3 | 4.0 | |
| | Input voltage for BOOT0 | $V_{SS}$ | 9.0 | |
| $\lvert\Delta V_{DDx}\rvert$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{SSX} - V_{SS}\rvert$ | Variations between all the different ground pins | - | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)* | | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum value must always be respected. Refer to *Table 12* for the values of the maximum allowed injected current.

*Figure 28* and *Figure 29* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is $f_{PLL\_OUT}$ nominal.

$T_{mode}$ is the modulation period.

md is the modulation depth.

**Figure 28. PLL output clock waveforms in center spread mode**

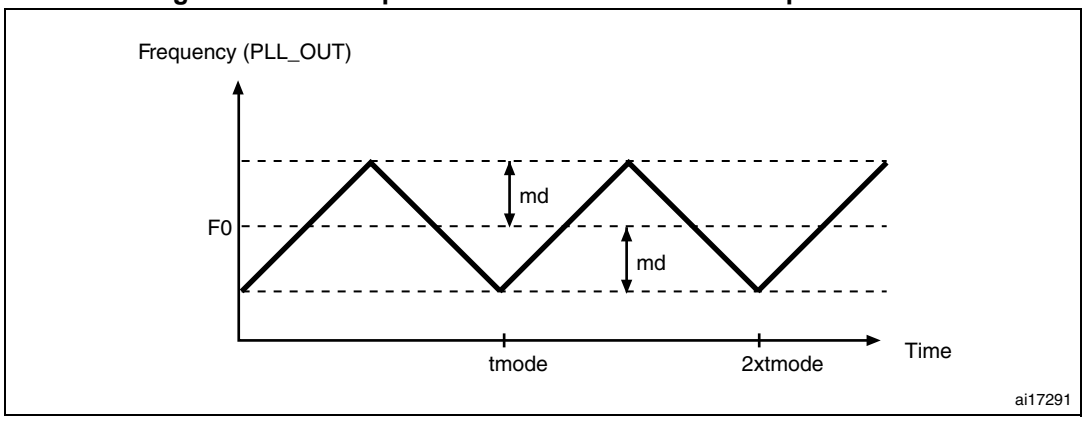
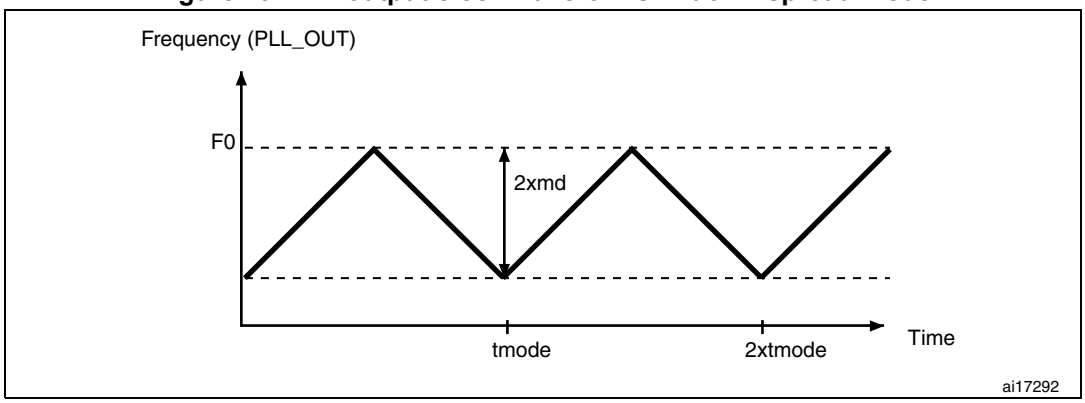



**Figure 29. PLL output clock waveforms in down spread mode**




## 6.3.12 Memory characteristics

### Flash memory

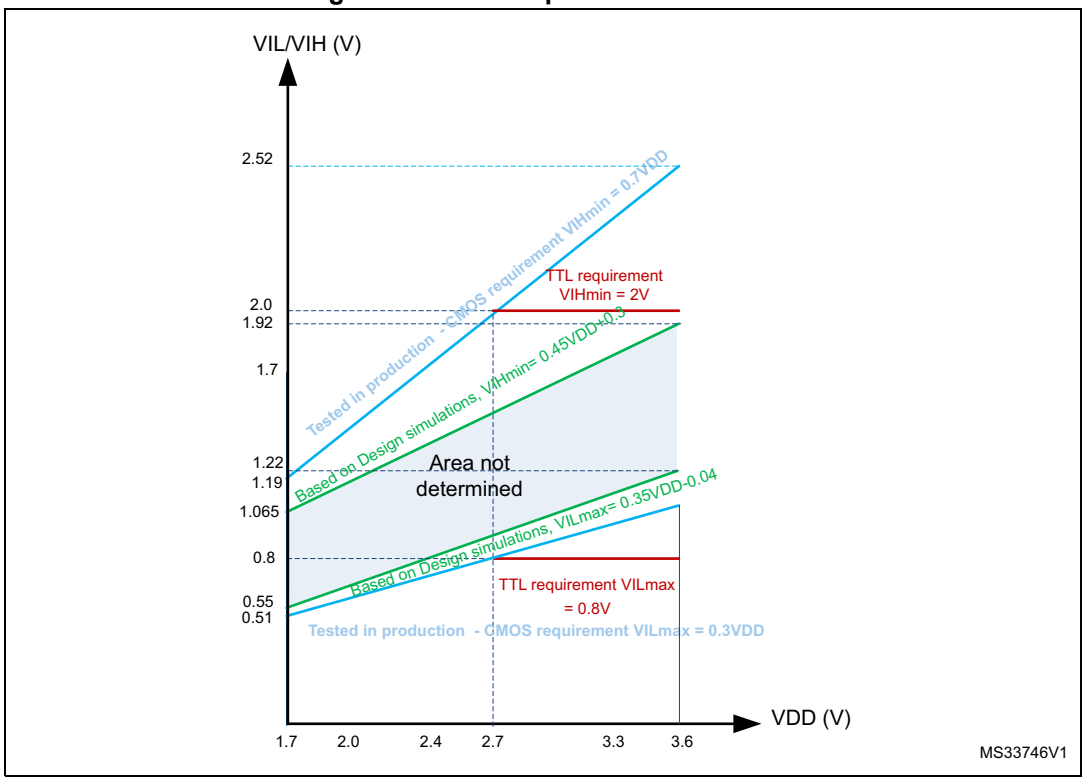
The characteristics are given at $T_A$ = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

**Table 44. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Write / Erase 8-bit mode, $V_{DD}$ = 1.7 V | - | 5 | - | mA |
| | | Write / Erase 16-bit mode, $V_{DD}$ = 2.1 V | - | 8 | - | |
| | | Write / Erase 32-bit mode, $V_{DD}$ = 3.3 V | - | 12 | - | |

**Figure 30. FT I/O input characteristics**




### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed $V_{OL}/V_{OH}$) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 12*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 12*).

### Output voltage levels

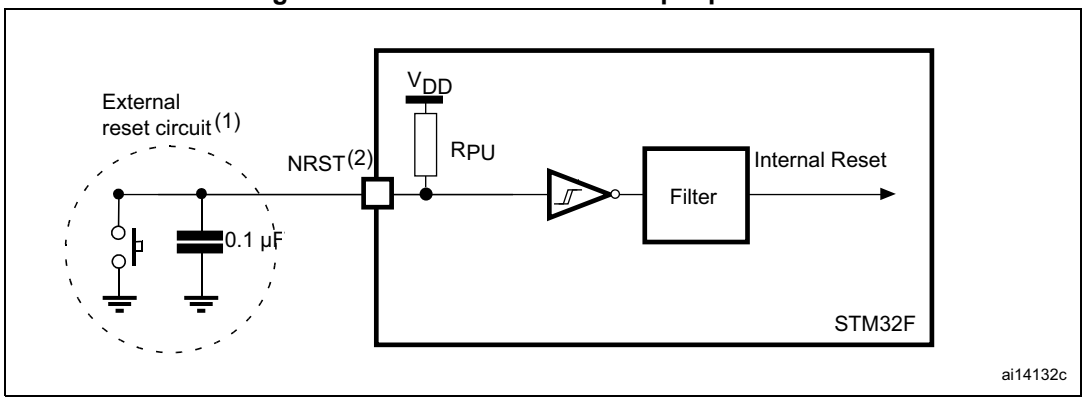
Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 14*. All I/Os are CMOS and TTL compliant.

**Table 56. I/O AC characteristics[1][2] (continued)**

| OSPEEDRy [1:0] bit value[1] | Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 01 | $f_{max(IO)out}$ | Maximum frequency[3] | $C_L$ = 50 pF, $V_{DD}$ ≥ 2.70 V | - | - | 25 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ ≥ 1.7 V | - | - | 12.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 50 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 20 | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 50 pF, $V_{DD}$ ≥2.7 V | - | - | 10 | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ ≥ 1.7 V | - | - | 20 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 6 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 10 | |
| 10 | $f_{max(IO)out}$ | Maximum frequency[3] | $C_L$ = 40 pF, $V_{DD}$ ≥ 2.70 V | - | - | 50[4] | MHz |
| | | | $C_L$ = 40 pF, $V_{DD}$ ≥ 1.7 V | - | - | 25 | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 100[4] | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 1.7 V | - | - | 50[4] | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 40 pF, $V_{DD}$≥ 2.70 V | - | - | 6 | ns |
| | | | $C_L$ = 40 pF, $V_{DD}$≥ 1.7 V | - | - | 10 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 2.70 V | - | - | 4 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 1.7 V | - | - | 6 | |
| 11 | $F_{max(IO)out}$ | Maximum frequency[3] | $C_L$ = 30 pF, $V_{DD}$ ≥ 2.70 V | - | - | 100[4] | MHz |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥ 1.7 V | - | - | 50[4] | |
| | | | $C_L$ = 10 pF, $V_{DD}$ ≥ 2.70 V | - | - | 180[4] | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 1.7 V | - | - | 100[4] | |
| | $t_{f(IO)out}$/ $t_{r(IO)out}$ | Output high to low level fall time and output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ ≥ 2.70 V | - | - | 4 | ns |
| | | | $C_L$ = 30 pF, $V_{DD}$ ≥ 1.7 V | - | - | 6 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 2.70 V | - | - | 2.5 | |
| | | | $C_L$ = 10 pF, $V_{DD}$≥ 1.7 V | - | - | 4 | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | - | - | ns |

1. Guaranteed by characterization, not tested in production.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 31*.
4. For maximum frequencies above 50 MHz and $V_{DD}$ > 2.4 V, the compensation cell should be used.

**Figure 32. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 57*. Otherwise the reset is not taken into account by the device.

## 6.3.18 TIM timer characteristics

The parameters given in *Table 58* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 58. TIMx characteristics(1)(2)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 84 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 11.9 | - | ns |
| | | AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 84 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | | 11.9 | - | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK}$ = 84 MHz | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | | 0 | 42 | MHz |
| $Res_{TIM}$ | Timer resolution | | - | 16/32 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | $f_{TIMxCLK}$ = 84 MHz | 0.0119 | 780 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count with 32-bit counter | | - | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 84 MHz | - | 51.1 | S |

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design, not tested in production.
3. The maximum timer frequency on APB1 is 42 MHz and on APB2 is up to 84 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

**Table 75. Embedded internal reference voltage (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{Coeff}$(2) | Temperature coefficient | - | - | 30 | 50 | ppm/°C |
| $t_{START}$(2) | Startup time | - | - | 6 | 10 | µs |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production

**Table 76. Internal reference voltage calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| $V_{REFIN\_CAL}$ | Raw data acquired at temperature of 30 °C $V_{DDA}$ = 3.3 V | 0x1FFF 7A2A - 0x1FFF 7A2B |

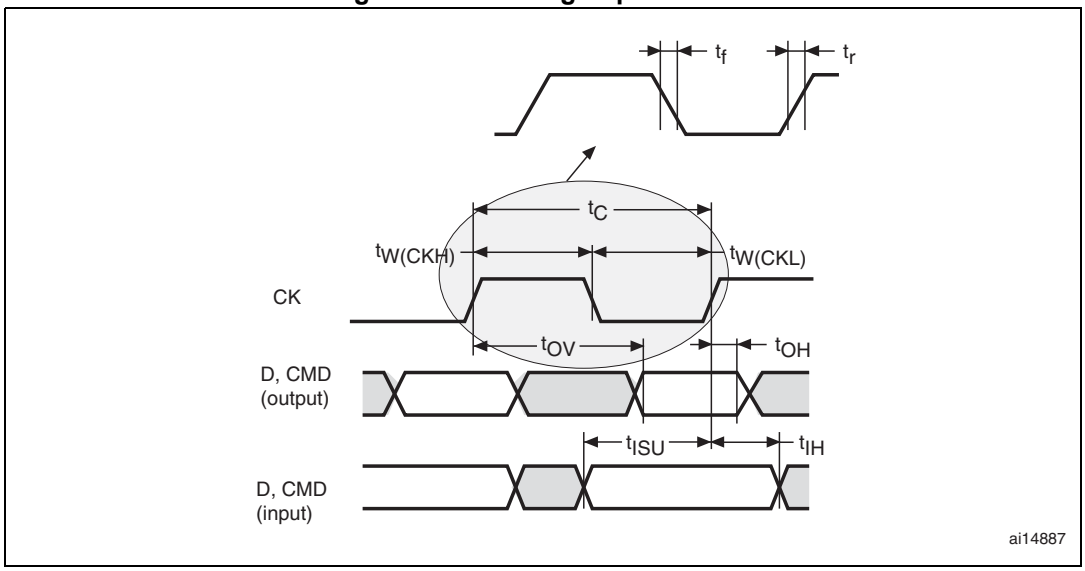
## 6.3.24 SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 77* for the SDIO/MMC interface are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output characteristics.

**Figure 44. SDIO high-speed mode**



# 7 Package characteristics

## 7.1 Package mechanical data

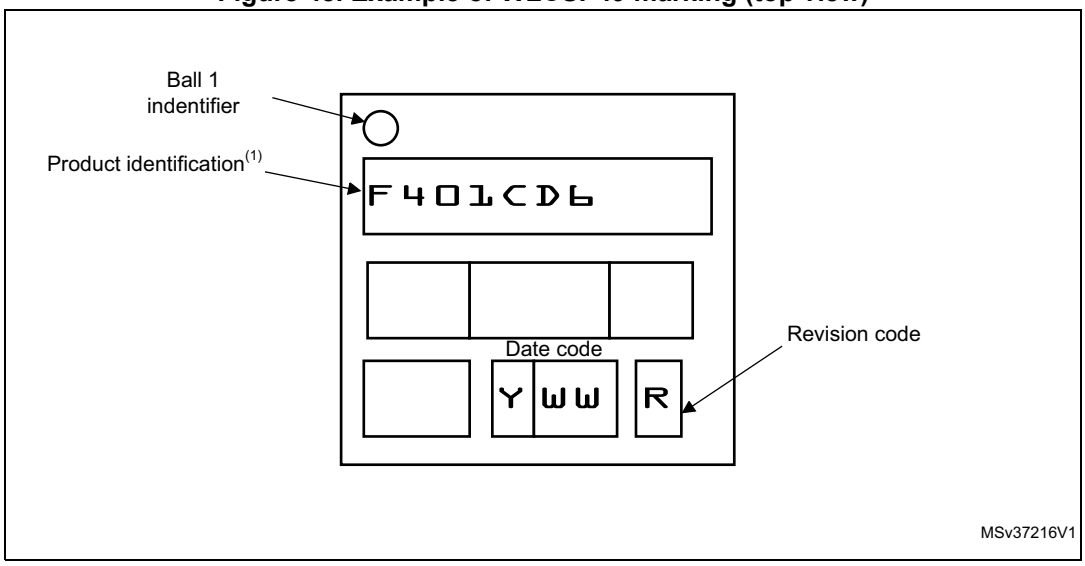
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

**Table 80. WLCSP49 recommended PCB design rules (0.4 mm pitch)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 mm |
| Dpad | 260 µm max. (circular)<br>220 µm recommended |
| Dsm | 300 µm min. (for 260 µm diameter pad) |
| PCB pad design | Non-solder mask defined via underbump allowed |

## Device marking

**Figure 48. Example of WLCSP49 marking (top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.