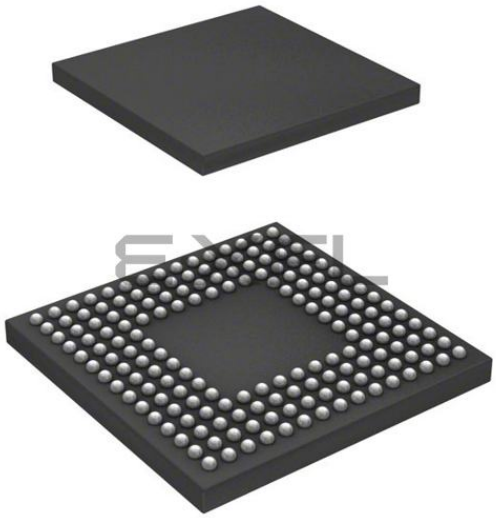
Renesas Electronics America Inc - R4F2113NBG#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LPC, SCI
Peripherals	POR, PWM, WDT
Number of I/O	130
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f2113nbg-u0

(10) PCS0 to PSC3 (Port CS) (V850ES/SA2) … 3-state I/O
PCS0 to PCS5 (Port CS) (V850ES/SA3) … 3-state I/O

[V850ES/SA2]

Port CS is a 4-bit I/O port that can be set to the input or output mode in 1-bit units.
Besides functioning as I/O port pins, in the control mode PCS0 to PSC3 also operate as the control signal output pins when the memory and peripheral I/O are expanded externally.

(a) Port mode

PCS0 to PSC3 can be set to the input or output mode in 1-bit units by using port mode register CM (PMCS).

(b) Control mode

(i) $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ (chip select) … Output

These are the chip select signals for the SRAM, external ROM, and external peripheral I/O area.
The $\overline{\text{CSn}}$ signal is assigned to memory block n (n = 0 to 3).
Each of these signals is active while the bus cycle accessing the corresponding memory block is being executed, and inactive in the idle state (TI).

[V850ES/SA3]

Port CS is an 8-bit I/O port that can be set to the input or output mode in 1-bit units.
Besides functioning as I/O port pins, in the control mode PCS0 to PSC3 also operate as the control signal output pins when the memory and peripheral I/O are expanded externally.

(a) Port mode

PCS0 to PCS7 can be set to the input or output mode in 1-bit units by using port mode register CS (PMCS).

(b) Control mode

(i) $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ (chip select) … Output

These are the chip select signals for the SRAM, external ROM, and external peripheral I/O area.
The $\overline{\text{CSn}}$ signal is assigned to memory block n (n = 0 to 3).
Each of these signals is active while the bus cycle accessing the corresponding memory block is being executed, and inactive in the idle state (TI).

- Interrupt/exception table

  The V850ES/SA2 and V850ES/SA3 speed up the interrupt response time by fixing handler addresses corresponding to interrupts/exceptions.

  A collection of these handler addresses is called an interrupt/exception table, which is mapped to the internal ROM area. When an interrupt/exception is acknowledged, execution jumps to a handler address and the program in the area starting from that address is executed. Table 3-3 shows the interrupt/exception sources and corresponding addresses.

Table 3-3. Interrupt/Exception Table

First Address of Interrupt/Exception Table	Interrupt/Exception Source	First Address of Interrupt/Exception Table	Interrupt/Exception Source
00000000H	RESET	00000180H	INTTM3
00000010H	NMI	00000190H	INTTM4
00000020H	INTWDT	000001A0H	INTTM5
00000040H	TRAP0n (n = 0 to F)	000001B0H	INTCSI0
00000050H	TRAP1n (n = 0 to F)	000001C0H	INTIIC[Note 1]
00000060H	ILGOP/DBG0	000001D0H	INTCSI1
00000080H	INTWDTM	000001E0H	INTSRE0
00000090H	INTP0	000001F0H	INTSR0
000000A0H	INTP1	00000200H	INTST0
000000B0H	INTP2	00000210H	INTCSI2
000000C0H	INTP3	00000220H	INTSRE1
000000D0H	INTP4	00000230H	INTSR1
000000E0H	INTP5	00000240H	INTST1
000000F0H	INTP6	00000250H	INTCSI3
00000100H	INTRTC	00000260H	INTCSI4[Note 2]
00000110H	INTCC00	00000270H	INTAD
00000120H	INTCC01	00000280H	INTDMA0
00000130H	INTOVF0	00000290H	INTDMA1
00000140H	INTCC10	000002A0H	INTDMA2
00000150H	INTCC11	000002B0H	INTDMA3
00000160H	INTOVF1	000002C0H	INTROV
00000170H	INTTM2	000002D0H	INTBRG

Notes 1. μPD703200Y, 703201, 703204, 70F3201Y, and 70F3204Y only

2. V850ES/SA3 only

(2) Registers

(a) Port register 4 (P4)

Port register 4 (P4) is an 8-bit register that controls reading the pin level and writing the output level. This register can be read or written in 8-bit or 1-bit units.

After reset: Undefined R/W Address: FFFFF408H

	7	6	5	4	3	2	1	0
P4	0	P46	P45	P44	P43	P42	P41	P40

P4n	Controls output data (in output mode) (n = 0 to 6)
0	Outputs 0.
1	Outputs 1.

Remarks 1. In input mode: When port 4 (P4) is read, the pin level at that time is read. When written, the data written to P4 is written. The input pin is not affected.

In output mode: When port 4 (P4) is read, the value of P4 is read. When a value is written to P4, it is immediately output.

2. After reset, an undefined value (pin input level) is read from P4 in the input mode. When P4 is read in the output mode, 00H (value of the output latch) is read.

(b) Port mode register 4 (PM4)

This is an 8-bit register that specifies the input or output mode.

This register can be read or written in 8-bit or 1-bit units.

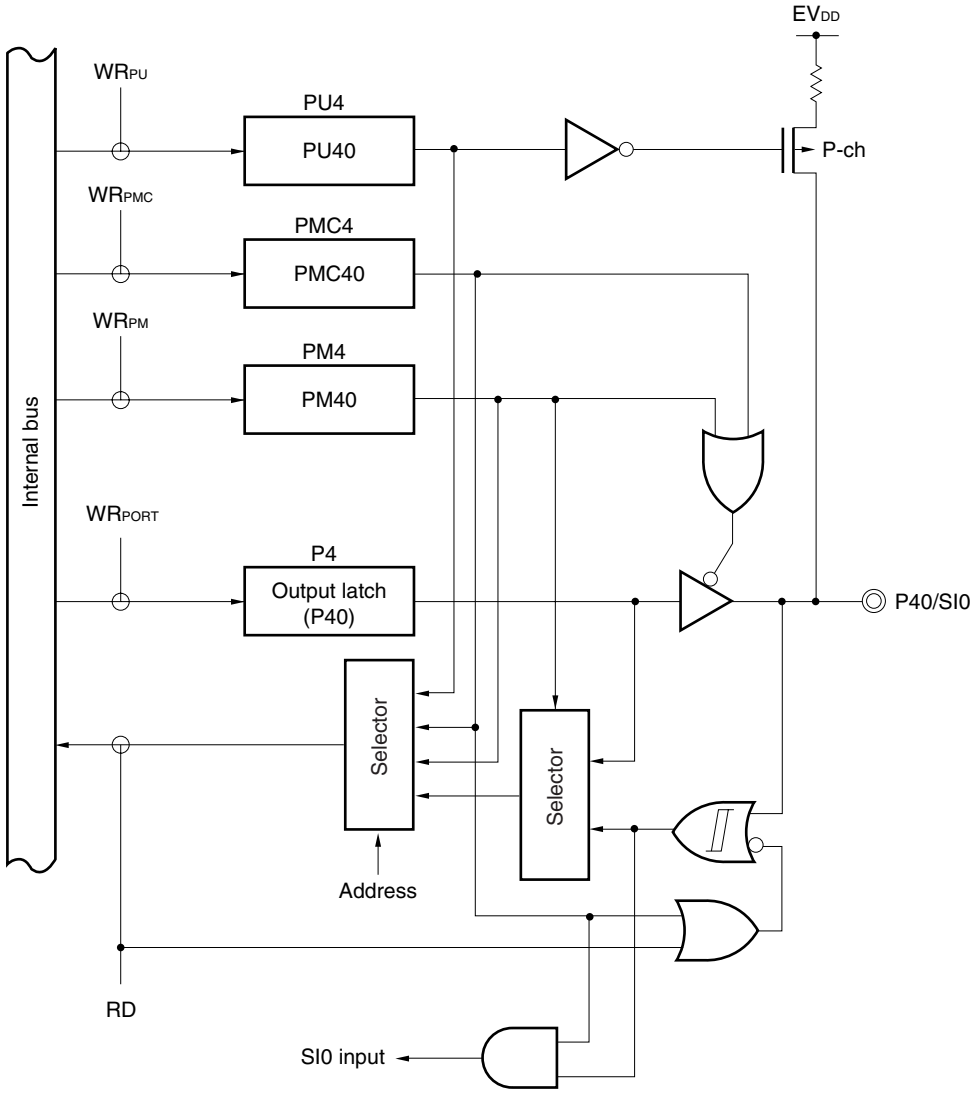
After reset: FFH R/W Address: FFFFF428H

	7	6	5	4	3	2	1	0
PM4	1	PM46	PM45	PM44	PM43	PM42	PM41	PM40

PM4n	Controls input/output mode (n = 0 to 6)
0	Output mode
1	Input mode

(3) Block diagram

Figure 4-11. Block Diagram of P40



Caution This pin does not have hysteresis characteristics in the port mode.
It has hysteresis characteristics only when an input-pin alternate function is used.

Remark P4: Port register 4
PM4: Port mode register 4
PMC4: Port mode control register 4
PU4: Pull-up resistor option register 4

(h) External interrupt rising edge specification register 9 (INTR9)

This 16-bit register specifies detection of the rising edge of the external interrupt pins.

It can be read or written only in 16-bit units. If the higher 8 bits of the INTR9 register are used as INTR9H and the lower 8 bits as INTR9L, however, INTR9H and INTR9L can be manipulated in 8-bit or 1-bit units.

Caution Set the port mode after clearing the INTF9n and INTR9n bits to 0 when switching from the external interrupt function (alternate function) to the port function because an edge may be detected.

After reset: 0000H R/W Address: INTR9 FFFFFC32H, INTR9L FFFFFC32H

	15	14	13	12	11	10	9	8
INTR9	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
(INTR9L)	0	0	0	0	INTR93	INTR92	0	0

Remark For how to specify a valid edge, refer to **Table 4-11**.

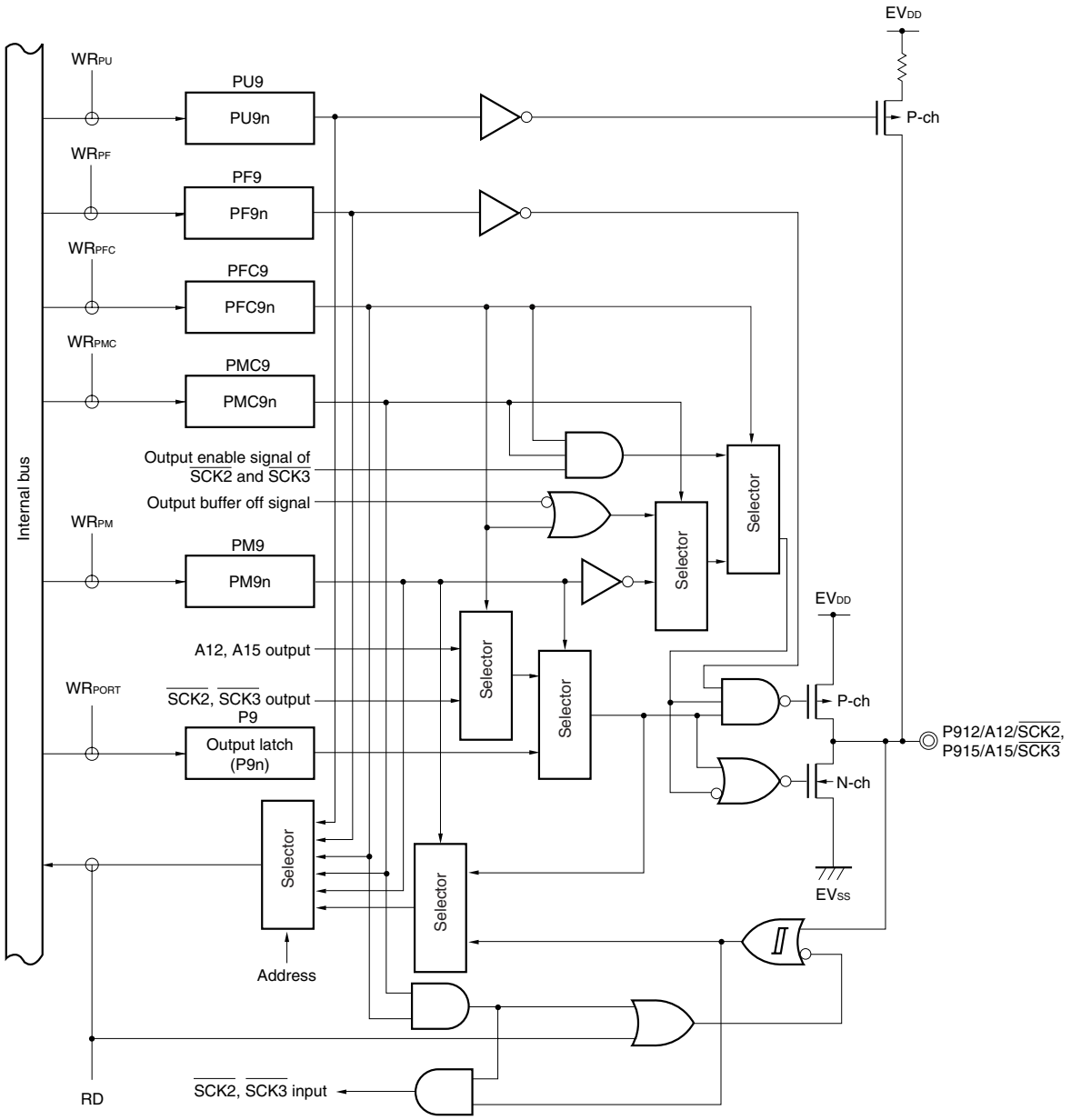
Table 4-11. Specifying Valid Edge

INTF9n	INTR9n	Specifies valid edge (n = 2 or 3).
0	0	Detects no edge.
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

Caution When INTP5 and INTP6 are not used, be sure to clear INTF9n and INTR9n to "00".

Remark n = 2 or 3: Control of INTP5 or INTP6 pin

Figure 4-23. Block Diagram of P912 and P915



Caution These pins do not have hysteresis characteristics in the port mode.
They have hysteresis characteristics only when an input-pin alternate function is used.

Remarks 1. P9: Port register 9
PM9: Port mode register 9
PMC9: Port mode control register 9
PFC9: Port function control register 9
PF9: Port function register 9
PU9: Pull-up resistor option register 9
Output buffer off signal: Signal that is active in the IDLE/STOP mode or during bus hold

2. n = 12 or 15

5.3.1 Chip select control function

Of the 64 MB (linear) address space, the lower 16 MB (0000000H to 0FFFFFFH) include four chip select functions, $\overline{CS0}$ to $\overline{CS3}$. The areas that can be selected by $\overline{CS0}$ to $\overline{CS3}$ are fixed.

By using these chip select functions, the memory block can be divided to enable effective use of the memory space. The allocation of the memory blocks is shown in the table below.

	V850ES/SA2	V850ES/SA3
$\overline{CS0}$	0000000H to 01FFFFFH (2 MB)	0000000H to 01FFFFFH (2 MB)
$\overline{CS1}$	0200000H to 03FFFFFH (2 MB)	0200000H to 03FFFFFH (2 MB)
$\overline{CS2}$	0400000H to 07FFFFFH (4 MB)	0400000H to 07FFFFFH (4 MB)
$\overline{CS3}$	0800000H to 0BFFFFFH (4 MB)	0800000H to 0FFFFFFH (8 MB)

5.4 External Bus Interface Mode Control Function

The V850ES/SA2 and V850ES/SA3 include the following two external bus interface modes.

- Multiplexed bus mode
- Separate bus mode

These two modes can be selected by using the external bus interface mode control register (EXIMC).

(1) External bus interface mode control register (EXIMC)

This register can be read or written in 8-bit or 1-bit units.

This register is cleared to 00H after reset.

After reset: 00H R/W Address: FFFFFFBEH

	7	6	5	4	3	2	1	0
EXIMC	0	0	0	0	0	0	0	SMSEL

SMSEL	Mode selection
0	Multiplexed bus mode
1	Separate bus mode

8.4.2 Operation as external event counter (8 bits)

The external event counter counts the number of clock pulses input to the TIn pin from an external source by using 8-bit timer counter n (TMn).

Each time the valid edge specified by timer clock selection register n (TCLn) is input to the TIn pin, the TMn register is incremented. Either the rising edge or the falling edge can be specified as the valid edge.

When the count value of the TMn register matches the value of 8-bit timer compare register n (CRn), the TMn register is cleared to 0 and an interrupt request signal (INTTMn) is generated.

Setting method

<1> Set each register.

- TCLn register: Selects the TIn input edge.
  Falling edge of TIn pin → TLCn = 00H
  Rising edge of TIn pin → TCLn = 01H
- CRn register: Compare value (N)
- TMCn register: Stops count operation, selects the mode in which clear & start occurs on a match between the TMn register and CRn register, disables timer output F/F inversion operation, and disables timer output.
  (TMCn register = 0000xx00B, ×: don't care)

<2> When the TMCEn bit of the TMCn register is set to 1, the counter counts the number of pulses input from TIn.

<3> When the values of the TMn register and CRn register match, INTTMn is generated (TMn register is cleared to 00H).

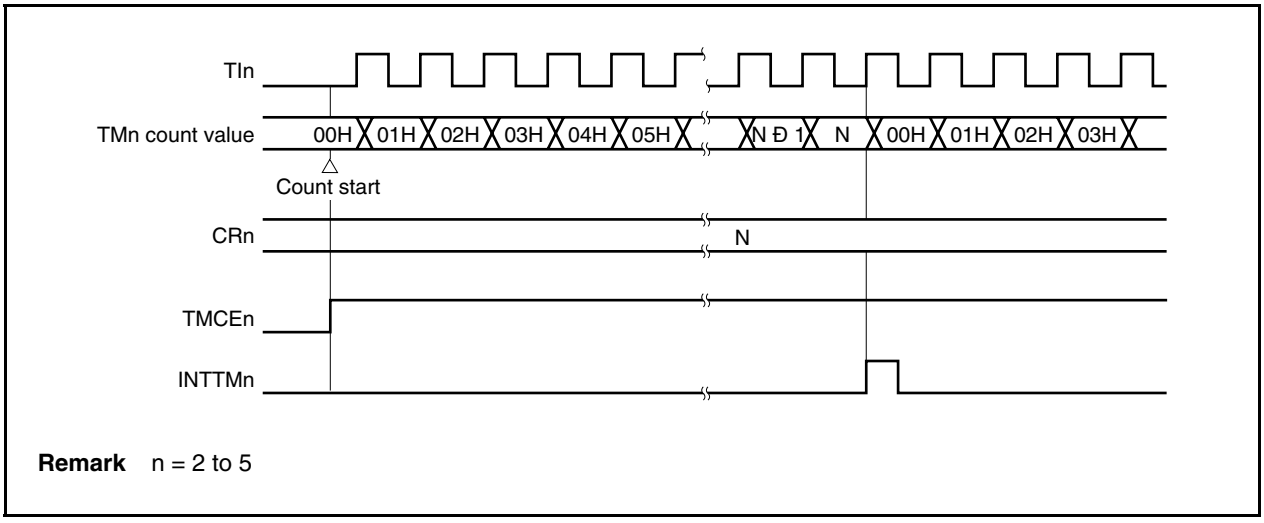
<4> Then, INTTMn is generated each time the values of the TMn register and CRn register match.

INTTMn is generated when the valid edge of TIn is input N + 1 times: N = 00 to FFH

Caution During external event counter operation, do not rewrite the value of the CRn register.

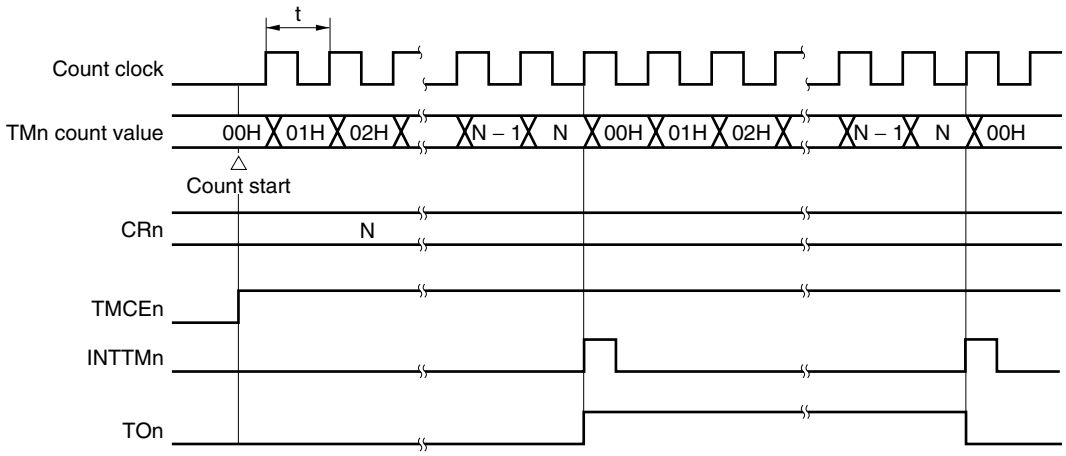
Remark n = 2 to 5

Figure 8-3. Timing of External Event Counter Operation (with Rising Edge Specified)



Remark n = 2 to 5

Figure 8-4. Timing of Square-Wave Output Operation



Note The initial value of the TOn output can be set using the LVSn and LVRn bits of the TMCn register.

Remark n = 0, 1

(2) RTC control register 1 (RTCC1)

The RTCC1 register is an 8-bit register that controls the operation of the real-time counter. This register can be read or written in 8-bit or 1-bit units.

This register is set to 8xH after reset.

After reset: 8xH[Note 1] R/W Address: FFFFF6E1H

	<7>	6	5	4	3	2	1	<0>
RTCC1	RTCE	INTS3	INTS2	INTS1	INTS0	0	0	RTCF[Note 2]

RTCE	Enables/disables RTC count-up operation
0	Disables RTC count operation.
1	Enables RTC count operation.

INTS3	INTS2	INTS1	INTS0	Specifies interrupt request signal generation timing
0	0	0	0	Does not generate interrupt request signal.
0	0	0	1	Generates interrupt request signal every 0.015625 second.
0	0	1	0	Generates interrupt request signal every 0.03125 second.
0	0	1	1	Generates interrupt request signal every 0.0625 second.
0	1	0	0	Generates interrupt request signal every 0.125 second.
0	1	0	1	Generates interrupt request signal every 0.25 second.
0	1	1	0	Generates interrupt request signal every 0.5 second.
0	1	1	1	Generates interrupt request signal every 1 second.
1	0	0	0	Generates interrupt request signal every 1 minute.
1	0	0	1	Generates interrupt request signal every 1 hour.
1	0	1	0	Generates interrupt request signal every 1 day.
Other than above				Setting prohibited

RTCF	RTC operation flag
0	Count operation is stopped
1	Count-up operation is in progress.

Notes 1. 80H or 81H, depending on the value of the RTCF bit.

2. The RTCF bit is a read-only bit.

Remark The timing of generating an interrupt request set by the INTS3 to INTS0 bits is determined by the setting of the CKS bit of the RTCC0 register, as follows.

When CKS bit = 0 f_{XT} = 32.768 kHz

When CKS bit = 1 f_{BRG} = 32.768 kHz

(3) Asynchronous serial interface transmission status register n (ASIFn)

The ASIFn register, which consists of 2 status flag bits, indicates the status during transmission.

By writing the next data to the TXBn register after data is transferred from the TXBn register to the transmit shift register, transmit operations can be performed continuously without suspension even during an interrupt interval. When transmission is performed continuously, data should be written after referencing the TXBFn bit of the ASIFn register to prevent writing to the TXBn register by mistake.

This register is read-only, in 8-bit or 1-bit units.

This register is cleared to 00H after reset.

After reset: 00H R Address: ASIF0 FFFFFA05H, ASIF1 FFFFFA15H

	7	6	5	4	3	2	<1>	<0>
ASIFn (n = 0, 1)	0	0	0	0	0	0	TXBFn	TXSFn

TXBFn	Transmit buffer data flag
0	Data to be transferred next to the TXBn register does not exist (when the ASIMn register's POWERn or TXEn bit is 0, or when data has been transferred to the transmit shift register)
1	Data to be transferred next exists in the TXBn register (data exists in the TXBn register when the TXBn register has been written to)
• When transmission is performed continuously, data should be written to the TXBn register after confirming that this flag is 0. If writing to the TXBn register is performed when this flag is 1, transmit data cannot be guaranteed.	

TXSFn	Transmit shift register data flag (indicating the transmission status of UARTn)
0	Initial status or a waiting transmission (when the ASIMn register's UARTCAEn or TXEn bit is set to 0, or following transfer completion, the next data transfer from the TXBn register is not performed)
1	Transmission in progress (when data has been transferred from the TXBn register)
• When the transmission unit is initialized, initialization should be executed after confirming that this flag is 0 following the occurrence of a transmission completion interrupt. If initialization is performed when this flag is 1, transmit data cannot be guaranteed.	

13.4 Interrupt Requests

The following three types of interrupt requests are generated from UARTn.

- Reception error interrupt (INTSREn)
- Reception completion interrupt (INTSRn)
- Transmission completion interrupt (INTSTn)

The default priorities among these three types of interrupt requests is, from high to low, reception error interrupt, reception completion interrupt, and transmission completion interrupt.

Table 13-1. Generated Interrupts and Default Priorities

Interrupt	Priority
Reception error	1
Reception completion	2
Transmission completion	3

(1) Reception error interrupt (INTSREn)

When reception is enabled, a reception error interrupt is generated according to the logical OR of the three types of reception errors explained for the ASISn register. Whether a reception error interrupt (INTSREn) or a reception completion interrupt (INTSRn) is generated when an error occurs can be specified using the ISRMn bit of the ASIMn register.

When reception is disabled, no reception error interrupt is generated.

(2) Reception completion interrupt (INTSRn)

When reception is enabled, a reception completion interrupt is generated when data is shifted in to the receive shift register and transferred to the receive buffer register (RXBn).

A reception completion interrupt request can be specified to be generated in place of a reception error interrupt using the ISRMn bit of the ASIMn register even when a reception error has occurred.

When reception is disabled, no reception completion interrupt is generated.

(3) Transmission completion interrupt (INTSTn)

A transmission completion interrupt is generated when one frame of transmit data containing 7-bit or 8-bit characters is shifted out from the transmit shift register.

(b) Baud rate generator control register n (BRGCn)

The BRGCn register is an 8-bit register that controls the baud rate (serial transfer speed) of UARTn.

This register can be read or written in 8-bit units.

This register is set to FFH after reset.

Caution If the MDLn7 to MDLn0 bits are to be overwritten, the TXEn and RXEn bits should be set to 0 in the ASIMn register first.

After reset: FFH R/W Address: BRGC0 FFFFFA07H, BRGC1 FFFFFA17H

	7	6	5	4	3	2	1	0
BRGCn (n = 0, 1)	MDLn7	MDLn6	MDLn5	MDLn4	MDLn3	MDLn2	MDLn1	MDLn0

MD Ln7	MD Ln6	MD Ln5	MD Ln4	MD Ln3	MD Ln2	MD Ln1	MD Ln0	Division value (k)	Serial clock
0	0	0	0	0	×	×	×	–	Setting prohibited
0	0	0	0	1	0	0	0	8	$f_{CKSR}/8$
0	0	0	0	1	0	0	1	9	$f_{CKSR}/9$
0	0	0	0	1	0	1	0	10	$f_{CKSR}/10$
:	:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	1	0	250	$f_{CKSR}/250$
1	1	1	1	1	0	1	1	251	$f_{CKSR}/251$
1	1	1	1	1	1	0	0	252	$f_{CKSR}/252$
1	1	1	1	1	1	0	1	253	$f_{CKSR}/253$
1	1	1	1	1	1	1	0	254	$f_{CKSR}/254$
1	1	1	1	1	1	1	1	255	$f_{CKSR}/255$

Remarks 1. f_{CKSR}: Frequency [Hz] of base clock (Clock) selected by TPSn3 to TPSn0 bits of CKSRn register

2. k: Value set by MDLn7 to MDLn0 bits (k = 8, 9, 10, ..., 255)

3. The baud rate is the output clock for the 8-bit counter divided by 2

4. ×: Don't care

15.2 Configuration

I²C includes the following hardware.

Table 15-1. Configuration of I²C

Item	Configuration
Registers	IIC shift register (IIC) Slave address register (SVA)
Control registers	IIC control register (IICC) IIC status register (IICS) IIC clock selection register (IICCL) IIC function expansion register (IICX)

(1) IIC shift register (IIC)

The IIC register is used to convert 8-bit serial data to 8-bit parallel data and to convert 8-bit parallel data to 8-bit serial data. The IIC register can be used for both transmission and reception.

Write and read operations to the IIC register are used to control the actual transmit and receive operations.

The IIC register can be read or written in 8-bit units.

This register is cleared to 00H after reset.

(2) Slave address register (SVA)

The SVA register sets local addresses when in slave mode.

The SVA register can be read or written in 8-bit units.

This register is cleared to 00H after reset.

(3) SO latch

The SO latch is used to retain the SDA pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request when the address received by this register matches the address value set to slave address register (SVA) or when an extension code is received.

(5) Clock selector

This selects the sampling clock to be used.

15.8 Address Match Detection Method

When in I²C bus mode, the master device can select a particular slave device by transmitting the corresponding slave address.

Address match detection is performed automatically by hardware. An interrupt request (INTIIC) occurs when a local address has been set to the slave address register (SVA) and when the address set to SVA matches the slave address sent by the master device, or when an extension code has been received.

15.9 Error Detection

In I²C bus mode, the status of the serial data bus (SDA) during data transmission is captured by the IIC shift register (IIC) of the transmitting device, so the IIC data prior to transmission can be compared with the transmitted IIC data to enable detection of transmission errors. A transmission error is judged as having occurred when the compared data values do not match.

15.10 Extension Code

(1) When the higher 4 bits of the receive address are either 0000 or 1111, the extension code flag (EXC) is set for extension code reception and an interrupt request (INTIIC) is issued at the falling edge of the eighth clock.
The local address stored in the slave address register (SVA) is not affected.

(2) If 11110xx0 is set to SVA by a 10-bit address transfer and 11110xx0 is transferred from the master device, the results are as follows. Note that the INTIIC signal occurs at the falling edge of the eighth clock.

Higher four bits of data match: EXC = 1[Note]
Seven bits of data match: COI = 1[Note]

Note EXC: Bit 5 of IIC status register (IICS)
COI: Bit 4 of IIC status register (IICS)

(3) Since the processing after the interrupt request occurs differs according to the data that follows the extension code, such processing is performed by software.
For example, when operation as a slave is not desired after the extension code is received, set bit 6 (LREL) of the IIC control register (IICC) to 1 and the CPU will enter the next communication wait state.

Table 15-4. Extension Code Bit Definitions

Slave Address	R/W Bit	Description
0000 000	0	General call address
0000 000	1	Start byte
0000 001	×	CBUS address
0000 010	×	Address that is reserved for different bus format
1111 0xx	×	10-bit slave address specification

16.3 Control Registers

16.3.1 DMA source address registers 0 to 3 (DSA0 to DSA3)

These registers are used to set the DMA source addresses (28 bits each) for DMA channel n (n = 0 to 3). They are divided into two 16-bit registers, DSAnH and DSAnL.

(1) DMA source address registers 0H to 3H (DSA0H to DSA3H)

These registers can be read or written in 16-bit units.

After reset: Undefined R/W Address: DSA0H FFFFF082H, DSA1H FFFFF08AH, DSA2H FFFFF092H, DSA3H FFFFF09AH

	15	14	13	12	11	10	9	8
DSAnH	IR	0	0	0	0	0	SA25	SA24

7	6	5	4	3	2	1	0
SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16

(n = 0 to 3)

IR	DMA source address specification
0	External memory, on-chip peripheral I/O
1	Internal RAM

SA25 to SA16	Sets the DMA source addresses (A25 to A16). During DMA transfer, it stores the next DMA transfer source address.

(2) DMA source address registers 0L to 3L (DSA0L to DSA3L)

These registers can be read or written in 16-bit units.

After reset: Undefined R/W Address: DSA0L FFFFF080H, DSA1L FFFFF088H, DSA2L FFFFF090H, DSA3L FFFFF098H

	15	14	13	12	11	10	9	8
DSAnL	SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8

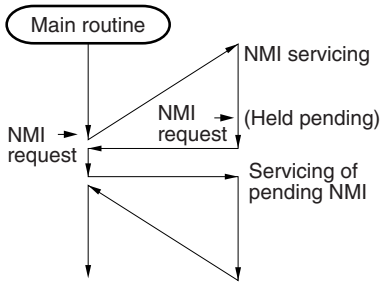
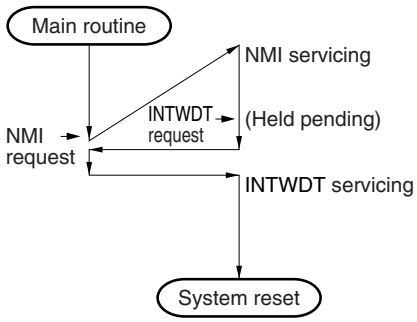
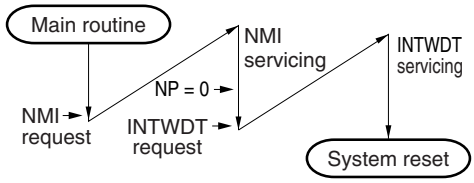
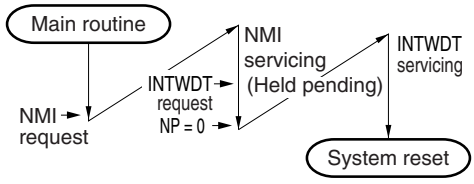
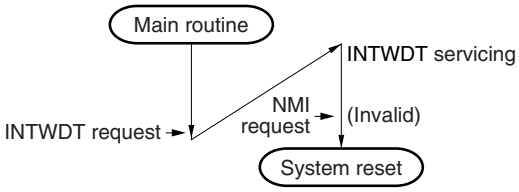
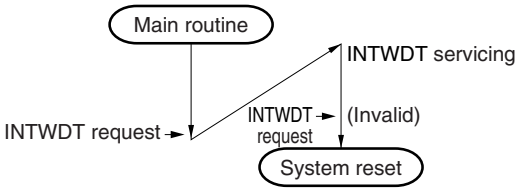
7	6	5	4	3	2	1	0
SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0

(n = 0 to 3)

SA15 to SA0	Sets the DMA source addresses (A15 to A0). During DMA transfer, it stores the next DMA transfer source address.

Figure 17-1. Non-Maskable Interrupt Request Acknowledgment Operation (2/2)

(b) Non-maskable interrupt request generated during non-maskable interrupt servicing

Non-maskable interrupt being serviced	Non-maskable interrupt request generated during non-maskable interrupt servicing	
	NMI	INTWDT
NMI	• NMI request generated during NMI servicing 	• INTWDT request generated during NMI servicing (NP = 1 retained before INTWDT request)  • INTWDT request generated during NMI servicing (NP = 0 set before INTWDT request)  • INTWDT request generated during NMI servicing (NP = 0 set after INTWDT request) 
INTWDT	• NMI request generated during INTWDT servicing 	• INTWDT request generated during INTWDT servicing 

17.8 Periods in Which Interrupts Are Not Acknowledged by CPU

An interrupt is acknowledged by the CPU while an instruction is being executed. However, no interrupt will be acknowledged between an interrupt request non-sample instruction and the next instruction (interrupt is held pending).

The interrupt request non-sample instructions are as follows.

- EI instruction
- DI instruction
- LDSR reg2, 0x5 instruction (for PSW)
- The store instruction for the command register (PRCMD)
- The load, store, or bit manipulation instructions for the following interrupt-related registers.
  Interrupt control register (xxICn), interrupt mask registers 0 to 2 (IMR0 to IMR2), in-service priority register (ISPR)

(2) Releasing HALT mode by $\overline{\text{RESET}}$ pin input and reset by watchdog timer

The same operation as the normal reset operation is performed.

Table 18-3. Operation Status in HALT Mode

Setting of HALT Mode / Item		Operation Status	
		When Subclock Is Not Used	When Subclock Is Used
Main clock oscillator		Oscillation enabled	
Subclock oscillator		–	Oscillation enabled
CPU		Stops operation	
DMA		Operable	
Interrupt controller		Operable	
ROM correction		Stops operation	
16-bit timer/event counters (TM0, TM1)		Operable	
8-bit timer/event counters (TM2 to TM5)		Operable	
Real-timer counter		Operable when divided f_X/BRG output is selected as count clock	Operable
Watchdog timer		Operable	
Serial interface	CSI0 to CSI4	Operable	
	I^2C[Note 1]	Operable	
	UART0, UART1	Operable	
A/D converter		Operable	
D/A converter		Normal mode: Stops operation (output is retained)[Note 2] Real-time output mode: Operable	
External bus interface		Refer to **CHAPTER 5 BUS CONTROL FUNCTION**.	
Port function		Retains status before HALT mode was set.	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the HALT mode was set.	

Notes 1. μPD703200Y, 703201Y, 703204Y, 70F3201Y, and 70F3204Y only

2. If the HALT mode is set immediately after the D/A conversion has started (during conversion), the operation continues until the D/A conversion is completed, when the D/A conversion is completed, the output is retained.

(5) Symbols used in flag operations

Symbol	Explanation
(Blank)	No change
0	Clear to 0
×	Set or cleared in accordance with the results.
R	Previously saved values are restored.

(6) Condition codes

Condition Name (cond)	Condition Code (cccc)	Condition Formula	Explanation
V	0 0 0 0	OV = 1	Overflow
NV	1 0 0 0	OV = 0	No overflow
C/L	0 0 0 1	CY = 1	Carry Lower (Less than)
NC/NL	1 0 0 1	CY = 0	No carry Not lower (Greater than or equal)
Z	0 0 1 0	Z = 1	Zero
NZ	1 0 1 0	Z = 0	Not zero
NH	0 0 1 1	(CY or Z) = 1	Not higher (Less than or equal)
H	1 0 1 1	(CY or Z) = 0	Higher (Greater than)
S/N	0 1 0 0	S = 1	Negative
NS/P	1 1 0 0	S = 0	Positive
T	0 1 0 1	—	Always (Unconditional)
SA	1 1 0 1	SAT = 1	Saturated
LT	0 1 1 0	(S xor OV) = 1	Less than signed
GE	1 1 1 0	(S xor OV) = 0	Greater than or equal signed
LE	0 1 1 1	((S xor OV) or Z) = 1	Less than or equal signed
GT	1 1 1 1	((S xor OV) or Z) = 0	Greater than signed