Renesas Electronics America Inc - R4F2113NFT#U0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LPC, SCI
Peripherals	POR, PWM, WDT
Number of I/O	114
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f2113nft-u0

(10) PCS0 to PSC3 (Port CS) (V850ES/SA2) … 3-state I/O
PCS0 to PCS5 (Port CS) (V850ES/SA3) … 3-state I/O

[V850ES/SA2]

Port CS is a 4-bit I/O port that can be set to the input or output mode in 1-bit units.
Besides functioning as I/O port pins, in the control mode PCS0 to PSC3 also operate as the control signal output pins when the memory and peripheral I/O are expanded externally.

(a) Port mode

PCS0 to PSC3 can be set to the input or output mode in 1-bit units by using port mode register CM (PMCS).

(b) Control mode

(i) $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ (chip select) … Output

These are the chip select signals for the SRAM, external ROM, and external peripheral I/O area.
The $\overline{\text{CSn}}$ signal is assigned to memory block n (n = 0 to 3).
Each of these signals is active while the bus cycle accessing the corresponding memory block is being executed, and inactive in the idle state (TI).

[V850ES/SA3]

Port CS is an 8-bit I/O port that can be set to the input or output mode in 1-bit units.
Besides functioning as I/O port pins, in the control mode PCS0 to PSC3 also operate as the control signal output pins when the memory and peripheral I/O are expanded externally.

(a) Port mode

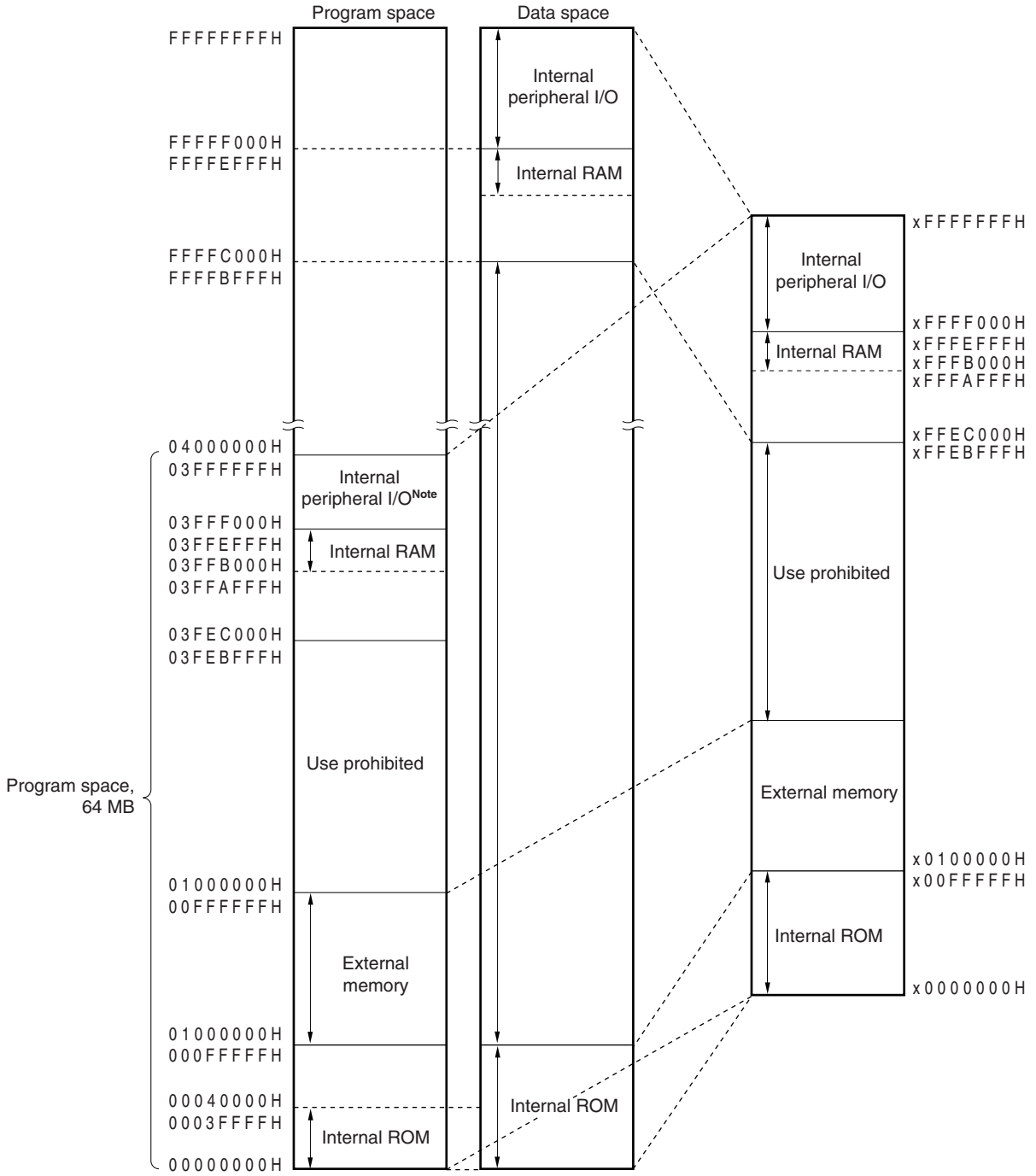
PCS0 to PCS7 can be set to the input or output mode in 1-bit units by using port mode register CS (PMCS).

(b) Control mode

(i) $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ (chip select) … Output

These are the chip select signals for the SRAM, external ROM, and external peripheral I/O area.
The $\overline{\text{CSn}}$ signal is assigned to memory block n (n = 0 to 3).
Each of these signals is active while the bus cycle accessing the corresponding memory block is being executed, and inactive in the idle state (TI).

Figure 3-11. Recommended Memory Map

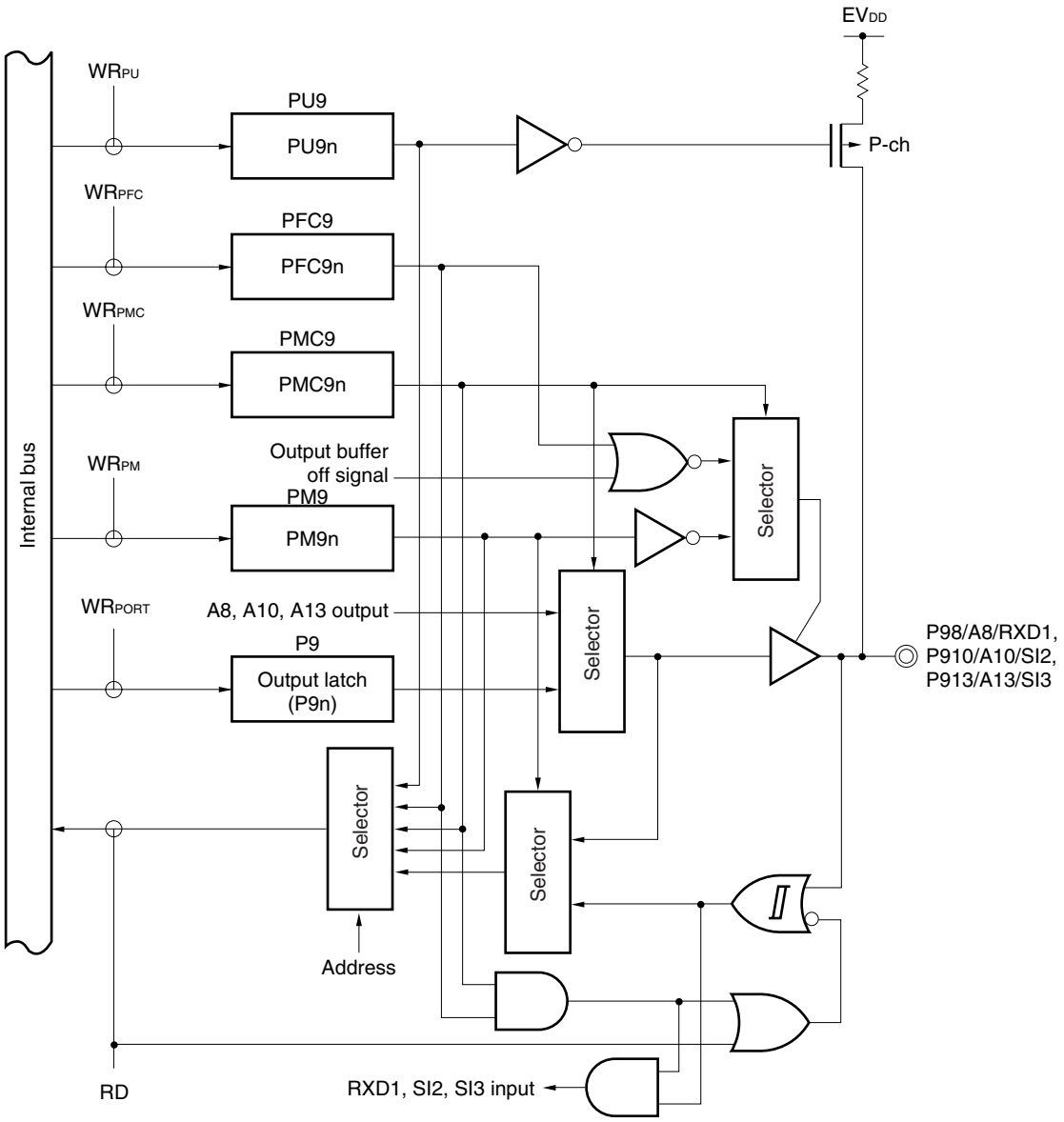


Note Access to this area is prohibited. To access the internal I/O in this area, specify addresses FFFF000H to FFFFFFFH.

Remarks 1. ↕ indicates the recommended area.

2. This figure is the recommended memory map of the μPD703204.

Figure 4-21. Block Diagram of P98, P910, and P913



Caution These pins do not have hysteresis characteristics in the port mode.
They have hysteresis characteristics only when an input-pin alternate function is used.

Remarks 1. P9: Port register 9
PM9: Port mode register 9
PMC9: Port mode control register 9
PF9: Port function register 9
PU9: Pull-up resistor option register 9
Output buffer off signal: Signal that is active in the IDLE/STOP mode or during bus hold

2. n = 8, 10, 13

4.3.13 Port DL

Port DL can be set to the input or output mode in 1-bit units.

The number of I/O port bits of each product is the same.

Commercial Name	Number of I/O Port Bits
V850ES/SA2	16-bit I/O port
V850ES/SA3	16-bit I/O port

(1) Functions of port DL

- ○ Input/output data can be specified in 1-bit units by using port register DL (PDL).
- ○ Can be set to the input or output mode in 1-bit units by using port mode register DL (PMDL).
- ○ Can be set to the port mode or control mode (alternate function) in 1-bit units by using port mode control register DL (PMCDL).

Port DL has an alternate function as the following pins.

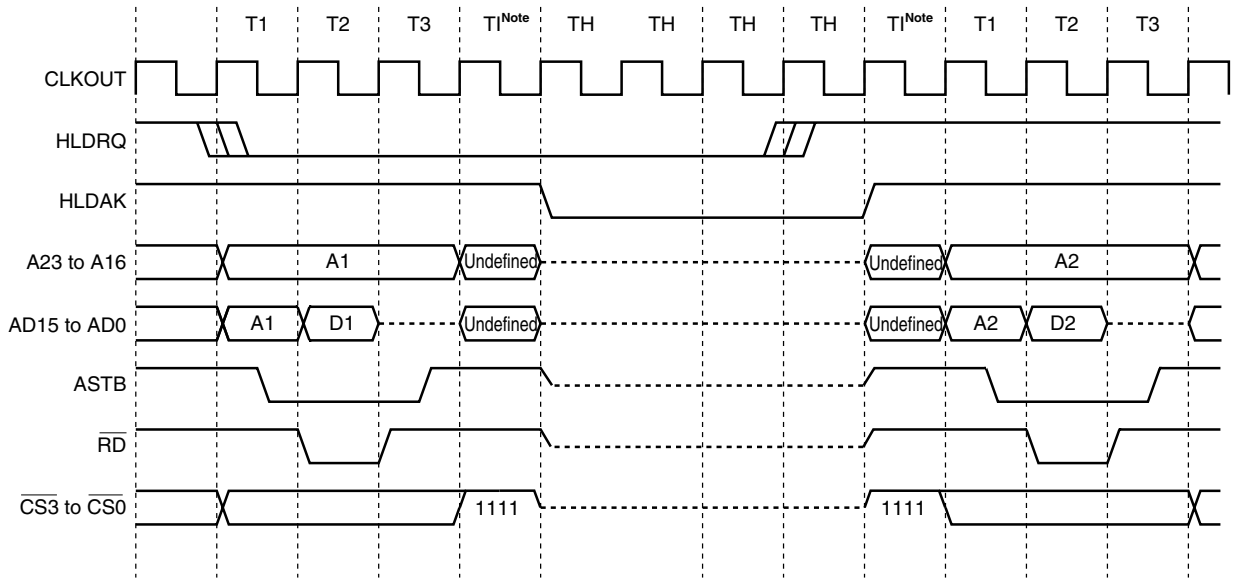
Table 4-17. Alternate-Function Pins of Port DL

Pin Name		Alternate-Function Pin	I/O	PULL[Note 1]	Remark
Port DL	PDL0	AD0	I/O	None	–
	PDL1	AD1			
	PDL2	AD2			
	PDL3	AD3			
	PDL4	AD4			
	PDL5	AD5/FLMD1[Note 2]			
	PDL6	AD6			
	PDL7	AD7			
	PDL8	AD8			
	PDLDL	AD9			
	PDL10	AD10			
	PDL11	AD11			
	PDL12	AD12			
	PDL13	AD13			
	PDL14	AD14			
	PDL15	AD15			

Notes 1. Software pull-up function

2. Because these pins are used for setting in the flash programming mode, they do not have to be manipulated by using a port control register. For details, refer to **CHAPTER 21 FLASH MEMORY** (μPD70F3201, 70F3201Y, 70F3204, and 70F3204Y only).

Figure 5-8. Multiplexed Bus Hold Timing (Bus Size: 16 Bits, 16-Bit Access)



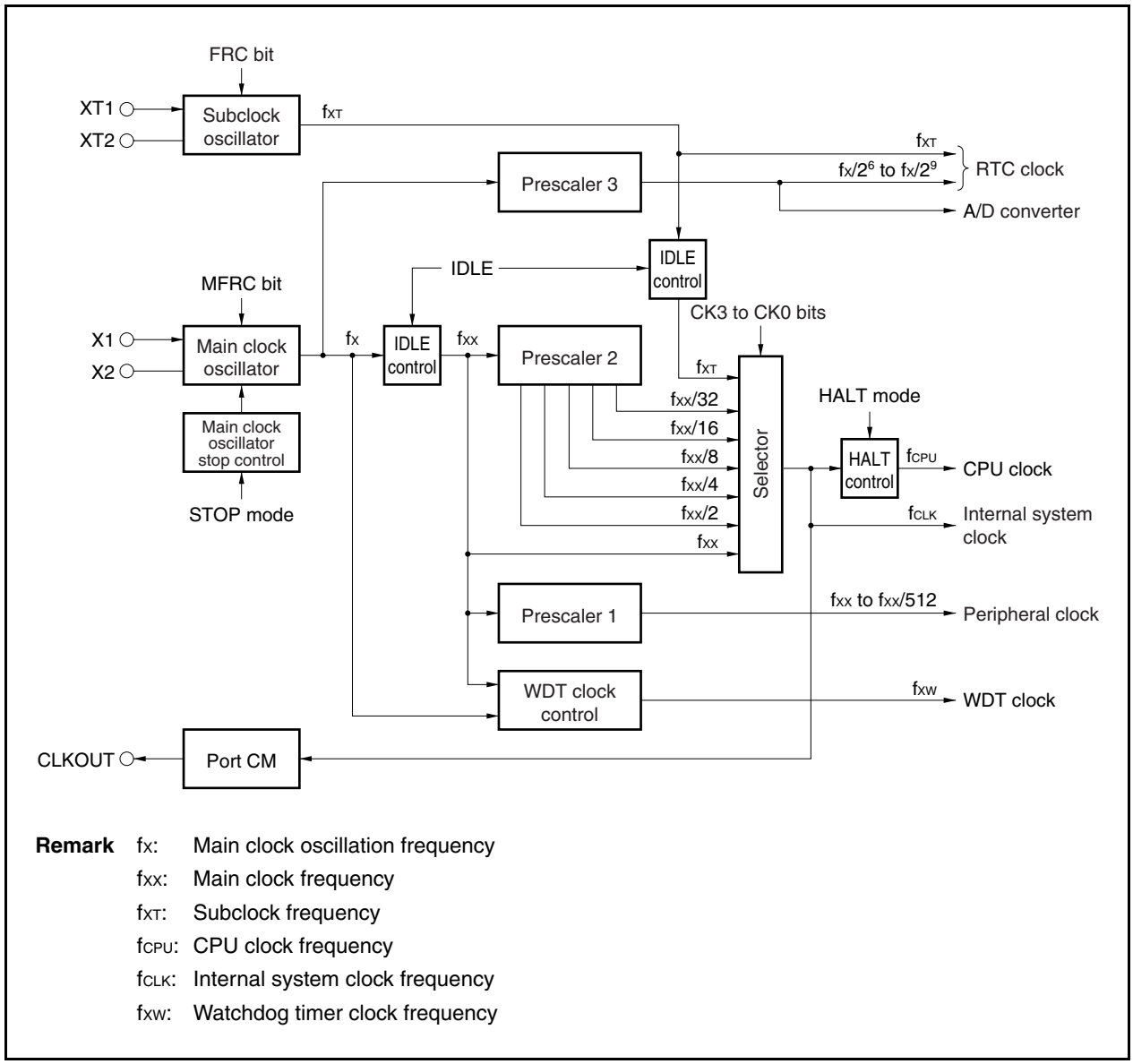
Note This idle state (TI) does not depend on the BCC register settings.

Remarks 1. Refer to **Table 2-3** for the pin statuses in the bus hold mode.

2. The broken lines indicate high impedance.

6.2 Configuration

Figure 6-1. Clock Generator



Remark f_X: Main clock oscillation frequency
f_{XX}: Main clock frequency
f_{XT}: Subclock frequency
f_{CPU}: CPU clock frequency
f_{CLK}: Internal system clock frequency
f_{XW}: Watchdog timer clock frequency

(1) A/D converter mode register (ADM)

This register sets the conversion time of the analog input signal to be converted into a digital signal as well as conversion start and stop.

The ADM register can be read or written in 8-bit or 1-bit units.

This register is cleared to 00H after reset.

After reset: 00H R/W Address: FFFFF200H

	<7>	6	5	4	3	2	1	0
ADM	ADCSB[Note 1]	0	FR3[Note 2]	FR2[Note 2]	FR1	FR0	0	0

ADCS[Note 1]	A/D conversion control
0	Stops conversion
1	Enables conversion

FR3[Note 2]	FR2[Note 2]	Number of A/D conversion clocks
0	0	19 clocks
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Setting prohibited

FR1	FR0	A/D conversion clock
0	0	$f_{XX}/16$
0	1	$f_{XX}/8$
1	0	$f_{XX}/4$
1	1	Clock of prescaler 3 (f_{BRG})

Notes 1. f_{BRG} output (refer to **6.5 Prescaler 3**) is alternated with the main clock divider of the real-time counter. To use f_{BRG} output as the conversion clock of the A/D converter, therefore, clear the CKS bit of RTC control register 0 (RTCC0) (refer to **9.2 (1)**) to 0.

An A/D conversion operation can be used to output the f_{BRG} clock in the IDLE mode. To reduce the power consumption, clear the CE bit of the prescaler mode register (PRSM) (refer to **6.5.1 (1)**) and ADCS bit of the ADM register to 0.

2. Be sure to clear the FR3 and FR2 bits to 00.

Caution Be sure to clear bits 6, 1, and 0 to 0.

Remark Refer to **Tables 11-2** and **11-3** for examples of setting the A/D conversion time.

(7) Receive data noise filter

The RXDn signal is sampled at the rising edge of the prescaler output base clock (Clock). If the same sampling value is obtained twice, the match detector output changes, and this output is sampled as input data. Therefore, data not exceeding one clock width is judged to be noise and is not delivered to the internal circuit (see **Figure 13-12**). Refer to **13.6 (1) (a) Base clock (Clock)** regarding the base clock.

Also, since the circuit is configured as shown in Figure 13-11, internal processing during a receive operation is delayed by up to 2 clocks according to the external signal status.

Figure 13-11. Noise Filter Circuit

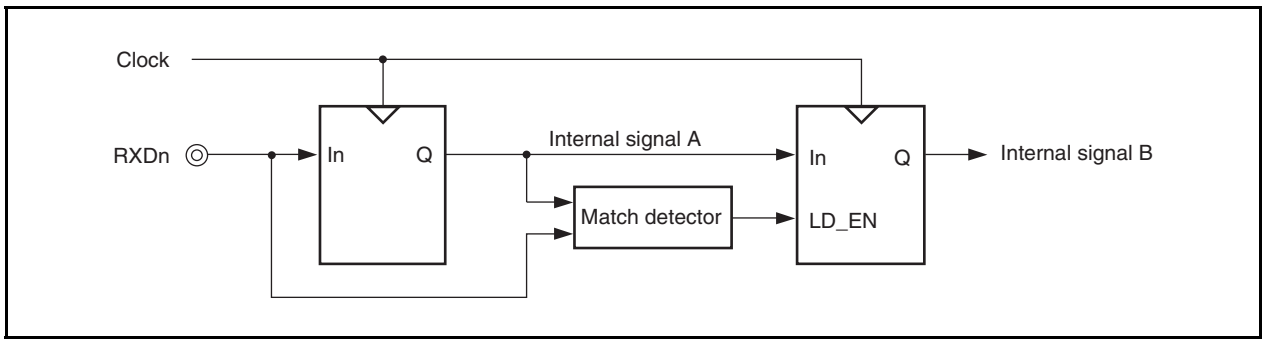
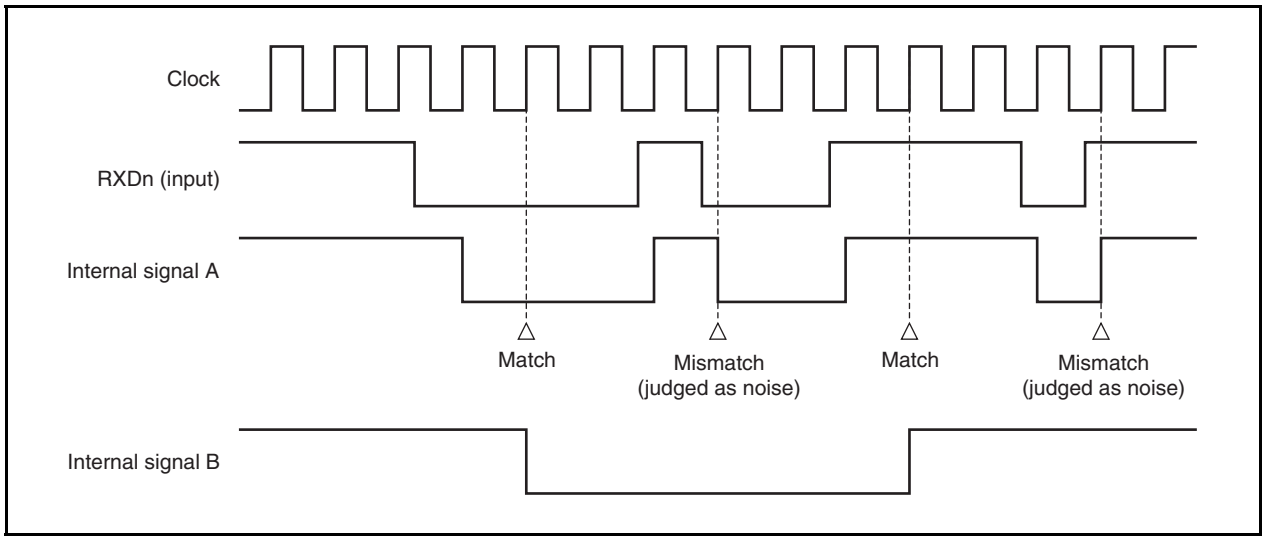


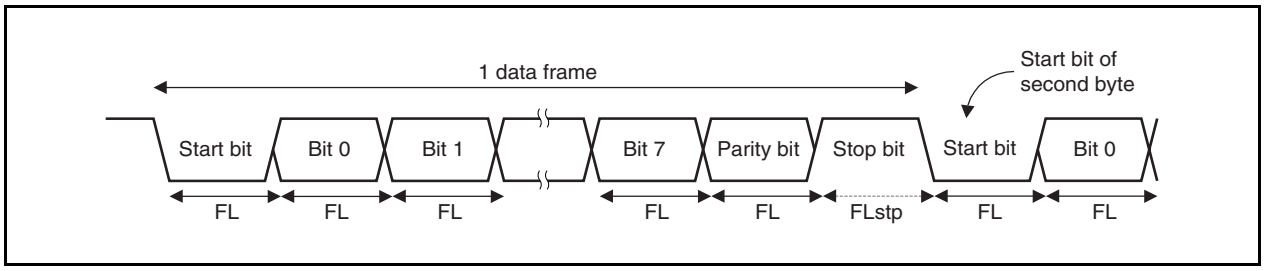
Figure 13-12. Timing of RXDn Signal Judged as Noise



(5) Transfer rate during continuous transmission

During continuous transmission, the transfer rate from a stop bit to the next start bit is extended two clocks of the base clock (Clock) longer than normal. However, on the reception side, the transfer result is not affected since the timing is initialized by the detection of the start bit.

Figure 13-15. Transfer Rate During Continuous Transmission



Representing the 1-bit data length by FL, the stop bit length by FLstp, and the base clock frequency by f_{CKSR} yields the following equation.

$$FLstp = FL + 2/f_{CKSR}$$

Therefore, the transfer rate during continuous transmission is as follows.

$$\text{Transfer rate} = 11 \times FL + 2/f_{CKSR}$$

14.1.2 Switching modes between CSI1 and UART0

CSI1 and UART0 of the V850ES/SA2 and V850ES/SA3 share pins, and therefore these interfaces cannot be used at the same time. Select CSI1 or UART0 in advance by using port mode control register 3 (PMC3) and port function control register 3 (PFC3) (refer to **4.3.3 Port 3**).

Caution CSI1 or UART0 transmission/reception operations are not guaranteed if the mode is changed during transmission or reception. Be sure to disable the operation of the unit that is not used.

Figure 14-2. Selecting CSI1 or UART0 Mode

After reset: 00H R/W Address: FFFFF446H

	7	6	5	4	3	2	1	0
PMC3	0	0	0	0	0	PMC32	PMC31	PMC30

After reset: 00H R/W Address: FFFFF466H

	7	6	5	4	3	2	1	0
PFC3	0	0	0	0	0	0	PFC31	PFC30

PMC3n	PFC3n	Operation mode
0	×	Port I/O mode
1	0	CSI1 mode
1	1	UART0 mode

Remarks 1. n = 0, 1

2. × = Don't care

14.2 Configuration

CSIn is controlled by the clocked serial interface mode register (CSIMn). Transmit/receive data can be written to or read from the SIOn register.

(1) Clocked serial interface mode register n (CSIMn)

The CSIMn register is an 8-bit register for specifying the operation of CSIn.

(2) Clocked serial interface clock selection register n (CSICn)

The CSICn register is an 8-bit register for controlling the transmit operation of CSIn.

(3) Serial I/O shift register n (SIOn)

The SIOn register is an 8-bit register for converting between serial data and parallel data. SIOn is used for both transmission and reception.

Data is shifted in (reception) or shifted out (transmission) beginning at either the MSB side or the LSB side.

Actual transmit/receive operations are controlled by reading or writing SIOn.

(a) Transfer rate selection example

CKSn2	CKSn1	CKSn0	Baud Rate (bps)					
			20 MHz Operation	17 MHz Operation	13.5 MHz Operation	10 MHz Operation	8 MHz Operation	4 MHz Operation
0	0	0	Setting prohibited	Setting prohibited	Setting prohibited	5,000,000	4,000,000	2,000,000
0	0	1	5,000,000	4,250,000	3,375,000	2,500,000	2,000,000	1,000,000
0	1	0	2,500,000	2,125,000	1,687,500	1,250,000	1,000,000	500,000
0	1	1	1,250,000	1,062,500	843,750	625,000	500,000	250,000
1	0	0	625,000	531,250	421,875	312,500	250,000	125,000
1	0	1	312,500	265,625	210,938	156,250	125,000	62,500

(2/4)

WREL	Wait cancellation control
0	Wait not canceled
1	Wait canceled. This setting is automatically cleared after wait is canceled.

Condition for clearing (WREL = 0)[Note]	Condition for setting (WREL = 1)
• Automatically cleared after execution • After reset	• Set by instruction

SPIE	Enable/disable generation of interrupt request when stop condition is detected
0	Disabled
1	Enabled

Condition for clearing (SPIE = 0)[Note]	Condition for setting (SPIE = 1)
• Cleared by instruction • After reset	• Set by instruction

WTIM	Control of wait and interrupt request generation
0	Interrupt request is generated at the eighth clockÕs falling edge. Master mode: After output of eight clocks, clock output is set to low level and wait is set. Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.
1	Interrupt request is generated at the eighth clockÕs falling edge. Master mode: After output of eight clocks, clock output is set to low level and wait is set. Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.

This bitÕs setting is invalid during an address transfer and is valid as the transfer is completed. When in master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after an $\overline{\text{ACK}}$ signal is issued. When the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.

Condition for clearing (WTIM = 0)[Note]	Condition for setting (WTIM = 1)
• Cleared by instruction • After reset	• Set by instruction

Note This flag's signal is invalid when IICE = 0.

(4) IIC function expansion register (IICX)

The IICX register is used to set the function expansion of I²C (valid only in high-speed mode).

The IICX register can be read or written in 8-bit or 1-bit units. Set the CLX bit in combination with the SMC, CL1, and CL0 bits of the IIC clock selection register (IICCL) (see **Table 15-2 Transfer Clock Setting**).

This register is cleared to 00H after reset.

After reset: 00H R/W Address: FFFFFD85H

	7	6	5	4	3	2	1	0
IICX	0	0	0	0	0	0	0	CLX

(5) I²C transfer clock setting method

The I²C transfer clock frequency (f_{SCL}) is calculated using the following expression.

$$f_{SCL} = 1/(m \times T + t_R + t_F)$$

m = 12, 18, 24, 48, 86, 88, 172 (see **Table 15-2 Transfer Clock Setting**.)

T: $1/f_{XX}$

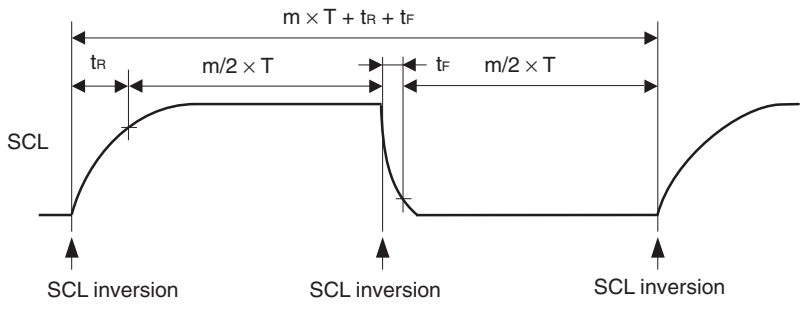
t_R: SCL rise time

t_F: SCL fall time

For example, the I²C transfer clock frequency (f_{SCL}) when f_{XX} = 16 MHz, m = 172, t_R = 200 ns, and t_F = 50 ns is calculated using the following expression.

$$f_{SCL} = 1/(172 \times 62.5 \text{ ns} + 200 \text{ ns} + 50 \text{ ns}) \cong 90.9 \text{ kHz}$$

Figure 15-4. I²C Transfer Clock Frequency (f_{SCL})



The transfer clock is set using a combination of the SMC, CL1, and CL0 bits of IIC clock select register (IICCL), the CLX bit of IIC function expansion register (IICX).

(4) Operation without communication

(a) Start ~ Code ~ Data ~ Data ~ Stop

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP
								Δ1

Δ 1: IICS = 00000001B

Remark Δ: Generated only when SPIE = 1

(5) Arbitration loss operation (operation as slave after arbitration loss)

(a) When arbitration loss occurs during transmission of slave address data

<1> When WTIM = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP
				▲1	▲2		▲3	Δ4

▲1: IICS = 0101X110B (Example: When ALD is read during interrupt servicing)

▲2: IICS = 0001X000B

▲3: IICS = 0001X000B

Δ 4: IICS = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE = 1
X: Don't care

<2> When WTIM = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP
				▲1		▲2	▲3	Δ4

▲1: IICS = 0101X110B (Example: When ALD is read during interrupt servicing)

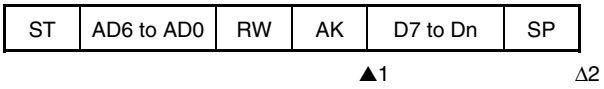
▲2: IICS = 0001X100B

▲3: IICS = 0001XX00B

Δ 4: IICS = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE = 1
X: Don't care

(e) When loss occurs due to stop condition during data transfer



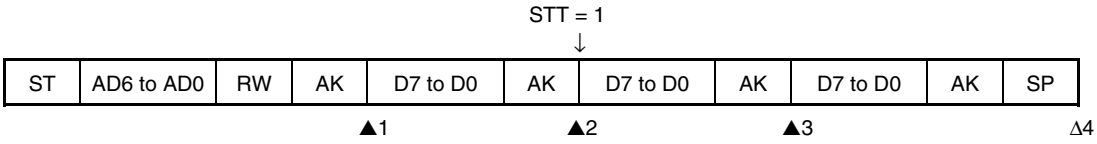
▲1: IICS = 1000X110B

Δ 2: IICS = 01000001B

Remark ▲: Always generated
Δ: Generated only when SPIE = 1
X: Don't care
Dn = D6 to D0

(f) When arbitration loss occurs due to low-level data when attempting to generate a restart condition

When WTIM = 1



▲1: IICS = 1000X110B

▲2: IICS = 1000XX00B

▲3: IICS = 01000100B (Example: When ALD is read during interrupt servicing)

Δ 4: IICS = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE = 1
X: Don't care

15.7 Interrupt Request (INTIIC) Generation Timing and Wait Control

The setting of bit 3 (WTIM) of the IIC control register (IICC) determines the timing by which INTIIC is generated and the corresponding wait control, as shown below.

Table 15-3. INTIIC Signal Generation Timing and Wait Control

WTIM	During Slave Device Operation			During Master Device Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 Notes 1, 2	8 Note 2	8 Note 2	9	8	8
1	9 Notes 1, 2	9 Note 2	9 Note 2	9	9	9

Notes 1. The slave device's INTIIC signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to slave address register (SVA).
At this point, $\overline{ACK}$ is output regardless of the value set to bit 2 (ACKE) of the IICC register. For a slave device that has received an extension code, the INTIIC signal occurs at the falling edge of the eighth clock.

2. If the received address does not match the contents of slave address register (SVA), neither the INTIIC signal nor a wait occurs.

Remark The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

(1) During address transmission/reception

- Slave device operation: The interrupt and wait timing are determined regardless of the WTIM bit.
- Master device operation: The interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM bit.

(2) During data reception

- Master/slave device operation: The interrupt and wait timing are determined according to the WTIM bit.

(3) During data transmission

- Master/slave device operation: The interrupt and wait timing are determined according to the WTIM bit.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

- By setting bit 5 (WREL) of the IIC control register (IICC) to 1
- By writing to the IIC shift register (IIC)
- By start condition setting (bit 1 (STT) of IIC control register (IICC) = 1)
- By stop condition setting (bit 0 (SPT) of IIC control register (IICC) = 1)

When an 8-clock wait has been selected (WTIM = 0), the output level of $\overline{ACK}$ must be determined prior to wait cancellation.

(5) Stop condition detection

INTIIC signal is generated when a stop condition is detected.

16.3.3 DMA byte count registers 0 to 3 (DBC0 to DBC3)

These 16-bit registers are used to set the byte transfer count for DMA channels n (n = 0 to 3). They store the remaining transfer count during DMA transfer.

These registers can be read or written in 16-bit units.

Remark If the DBCn register is read during DMA transfer after a terminal count has occurred without the register being overwritten, the value set immediately before the DMA transfer will be read out (0000H will not be read, even if DMA transfer has ended).

After reset: Undefined R/W Address: DBC0 FFFFF0C0H, DBC1 FFFFF0C2H, DBC2 FFFFF0C4H, DBC3 FFFFF0C6H

DBCn

15	14	13	12	11	10	9	8
BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8

7	6	5	4	3	2	1	0
BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0

(n = 0 to 3)

BC15 to BC0	Byte transfer count setting or remaining byte transfer count during DMA transfer
0000H	Byte transfer count 1 or remaining byte transfer count
0001H	Byte transfer count 2 or remaining byte transfer count
:	:
FFFFH	Byte transfer count 65,536 (2^{16}) or remaining byte transfer count

DC characteristics

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = EV_{DD} = 2.2 to 2.7 V, V_{SS} = AV_{SS} = EV_{SS} = 0 V) (2/3)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note] V850ES/SA2 (μPD70F3201, μPD70F3201Y) V850ES/SA3 (μPD70F3204, μPD70F3204Y)	I_{DD1}	Normal operation All peripheral functions operating	V_{DD} = 2.2 to 2.7 V@2 to 20 MHz			0.8 × f_{XX} + 2.5	1.58 × f_{XX} + 6.0	mA
				f_{XX} = 2 MHz		4.1	9.2	mA
				f_{XX} = 4 MHz		5.7	12.3	mA
				f_{XX} = 8 MHz		8.9	18.6	mA
				f_{XX} = 10 MHz		10.5	21.8	mA
				f_{XX} = 12 MHz		12.1	25.0	mA
				f_{XX} = 17 MHz		16.1	31.9	mA
				f_{XX} = 20 MHz		18.5	37.6	mA
	I_{DD2}	HALT mode All peripheral functions operating	V_{DD} = 2.2 to 2.7 V@2 to 20 MHz			0.37 × f_{XX} + 2.0	0.7 × f_{XX} + 3.0	mA
				f_{XX} = 2 MHz		2.7	4.4	mA
				f_{XX} = 4 MHz		3.5	5.8	mA
				f_{XX} = 8 MHz		5.0	8.6	mA
				f_{XX} = 10 MHz		6.2	10.0	mA
				f_{XX} = 12 MHz		6.9	11.4	mA
				f_{XX} = 17 MHz		8.2	14.9	mA
				f_{XX} = 20 MHz		9.4	17.0	mA
	I_{DD3}	IDLE mode RTC operation	V_{DD} = 2.2 to 2.7 V@2 to 20 MHz			40 × f_{XX} + 300	70 × f_{XX} + 500	μA
				f_{XX} = 2 MHz		380	640	μA
				f_{XX} = 4 MHz		460	780	μA
				f_{XX} = 8 MHz		620	1060	μA
				f_{XX} = 10 MHz		700	1200	μA
				f_{XX} = 12 MHz		780	1340	μA
				f_{XX} = 17 MHz		980	1690	μA
				f_{XX} = 20 MHz		1100	1900	μA
	I_{DD4}	STOP mode	Sub oscillator, Only RTC operates	T_A = 25°C		4	20	μA
				T_A = 85°C		–	60	μA
			Sub oscillator stopped (XT1 = V_{SS})	T_A = 25°C		1	10	μA
				T_A = 85°C		–	50	μA
	I_{DD5}	Subclock operation mode (f_{XT} = 32.768 kHz)				150	250	μA
	I_{DD6}	Sub-IDLE mode (f_{XT} = 32.768 kHz) Main clock oscillator stopped, RTC operates		T_A = 25°C		4	20	μA
				T_A = 85°C		–	60	μA

Note The typical value of V_{DD} is 2.5 V. The value does not include the current consumed at the output buffer.

Remark f_{XX}: Main clock frequency (MHz)

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Symbol	Name	Unit	Page
DDA1H	DMA destination address register 1H	DMAC	411
DDA1L	DMA destination address register 1L	DMAC	411
DDA2H	DMA destination address register 2H	DMAC	411
DDA2L	DMA destination address register 2L	DMAC	411
DDA3H	DMA destination address register 3H	DMAC	411
DDA3L	DMA destination address register 3L	DMAC	411
DMAIC0	Interrupt control register	INTC	441
DMAIC1	Interrupt control register	INTC	441
DMAIC2	Interrupt control register	INTC	441
DMAIC3	Interrupt control register	INTC	441
DSA0H	DMA source address register 0H	DMAC	410
DSA0L	DMA source address register 0L	DMAC	410
DSA1H	DMA source address register 1H	DMAC	410
DSA1L	DMA source address register 1L	DMAC	410
DSA2H	DMA source address register 2H	DMAC	410
DSA2L	DMA source address register 2L	DMAC	410
DSA3H	DMA source address register 3H	DMAC	410
DSA3L	DMA source address register 3L	DMAC	410
DTFR0	DMA trigger factor register 0	DMAC	415
DTFR1	DMA trigger factor register 1	DMAC	415
DTFR2	DMA trigger factor register 2	DMAC	415
DTFR3	DMA trigger factor register 3	DMAC	415
DWC0	Data wait control register 0	BCU	188
ECR	Interrupt source register	CPU	58
EIPC	Interrupt status saving register	CPU	57
EIPSW	Interrupt status saving register	CPU	57
EXIMC	External bus interface mode control register	BCU	180
FEPC	NMI status saving register	CPU	58
FEPSW	NMI status saving register	CPU	58
HOUR	Hour count register	RTC	263
HOURB	Hour count setting register	RTC	264
IIC	IIC shift register	I^2C	363
IICC	IIC control register	I^2C	353
IICCL	IIC clock select register	I^2C	361
IICIC	Interrupt control register	INTC	441
IICS	IIC status register	I^2C	358
IICX	IIC function expansion register	I^2C	362
IMR0	Interrupt mask register 0	INTC	442
IMR0H	Interrupt mask register 0H	INTC	442
IMR0L	Interrupt mask register 0L	INTC	442
IMR1	Interrupt mask register 1	INTC	442
IMR1H	Interrupt mask register 1H	INTC	442
IMR1L	Interrupt mask register 1L	INTC	442
IMR2	Interrupt mask register 2	INTC	442

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Symbol	Name	Unit	Page
TCL5	Timer clock selection register 5	Timer	243
TM0	Timer 0	Timer	214
TM1	Timer 1	Timer	214
TM2	Timer counter 2	Timer	241
TM3	Timer counter 3	Timer	241
TM4	Timer counter 4	Timer	241
TM5	Timer counter 5	Timer	241
TMC00	Timer control register 00	Timer	217
TMC01	Timer control register 01	Timer	219
TMC10	Timer control register 10	Timer	217
TMC11	Timer control register 11	Timer	217
TMC2	Timer mode control register 2	Timer	244
TMC3	Timer mode control register 3	Timer	244
TMC4	Timer mode control register 4	Timer	244
TMC5	Timer mode control register 5	Timer	244
TMIC2	Interrupt control register	INTC	441
TMIC3	Interrupt control register	INTC	441
TMIC4	Interrupt control register	INTC	441
TMIC5	Interrupt control register	INTC	441
TXB0	Transmit buffer register 0	UART	309
TXB1	Transmit buffer register 1	UART	309
VSWC	System wait control register	BCU	87
WDCS	Watchdog timer clock selection register	WDT	272
WDTIC	Interrupt control register	INTC	441
WDTM	Watchdog timer mode register	WDT	273, 444
WEEK	Week count register	RTC	265
WEEKB	Week count setting register	RTC	265