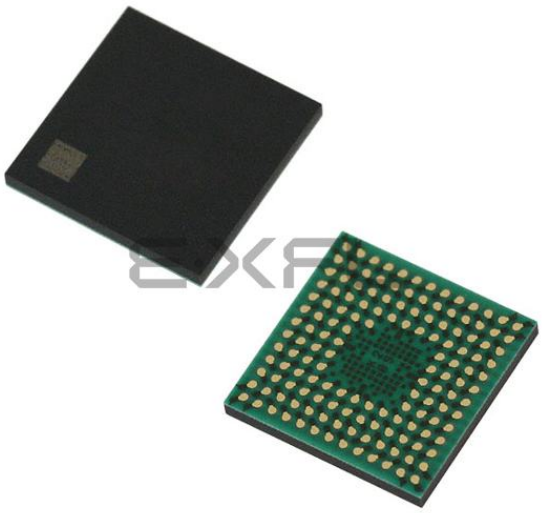
Renesas Electronics America Inc - R4F2113NLG#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LPC, SCI
Peripherals	POR, PWM, WDT
Number of I/O	114
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r4f2113nlg-u0

CONTENTS

(2/2)

Pin No.	Name	Pin No.	Name	Pin No.	Name
G11	EV_{SS}	K13	PDL3/AD3	M7	PCS4
G12	PDL10/AD10	L1	P93/A3/INTP6	M8	PCM0/$\overline{WAIT}$
G13	EV_{DD}	L2	P94/A4/TO2	M9	PCM2/$\overline{HLDAK}$
H1	V_{SS}	L3	P911/A11/SO2	M10	PCT3
H2	V_{DD}	L4	P914/A14/SO3	M11	PCT4/$\overline{RD}$
H3	XT2	L5	P915/A15/$\overline{SCK3}$	M12	PCT7
H11	PDL8/AD8	L6	EV_{DD}	M13	PDL0/AD0
H12	IC/FLMD0[Notes 1, 2]	L7	PCS0/$\overline{CS0}$	N1	P96/A6/TO4
H13	PDL9/AD9	L8	PCS2/$\overline{CS2}$	N2	P98/A8/RXD1
J1	P20/SI4	L9	PCM4	N3	P910/A10/SI2
J2	P91/A1	L10	PCT2	N4	P912/A12/$\overline{SCK2}$
J3	P90/A0	L11	PCT0/$\overline{WR0}$	N5	PCS7
J11	PDL5/AD5/FLMD1[Note 1]	L12	PDL1/AD1	N6	PCS6
J12	PDL7/AD7	L13	PDL2/AD2	N7	PCS1/$\overline{CS1}$
J13	PDL6/AD6	M1	P95/A5/TO3	N8	PCS3/$\overline{CS3}$
K1	P22/$\overline{SCK4}$	M2	P97/A7/TO5	N9	PCM5
K2	P92/A2/INTP5	M3	P99/A9/TXD1	N10	PCM3/$\overline{HLDRQ}$
K3	P21/SO4	M4	P913/A13/SI3	N11	PCT1/$\overline{WR1}$
K11	PCM1/CLKOUT	M5	EV_{SS}	N12	PCT5
K12	PDL4/AD4	M6	PCS5	N13	PCT6/ASTB

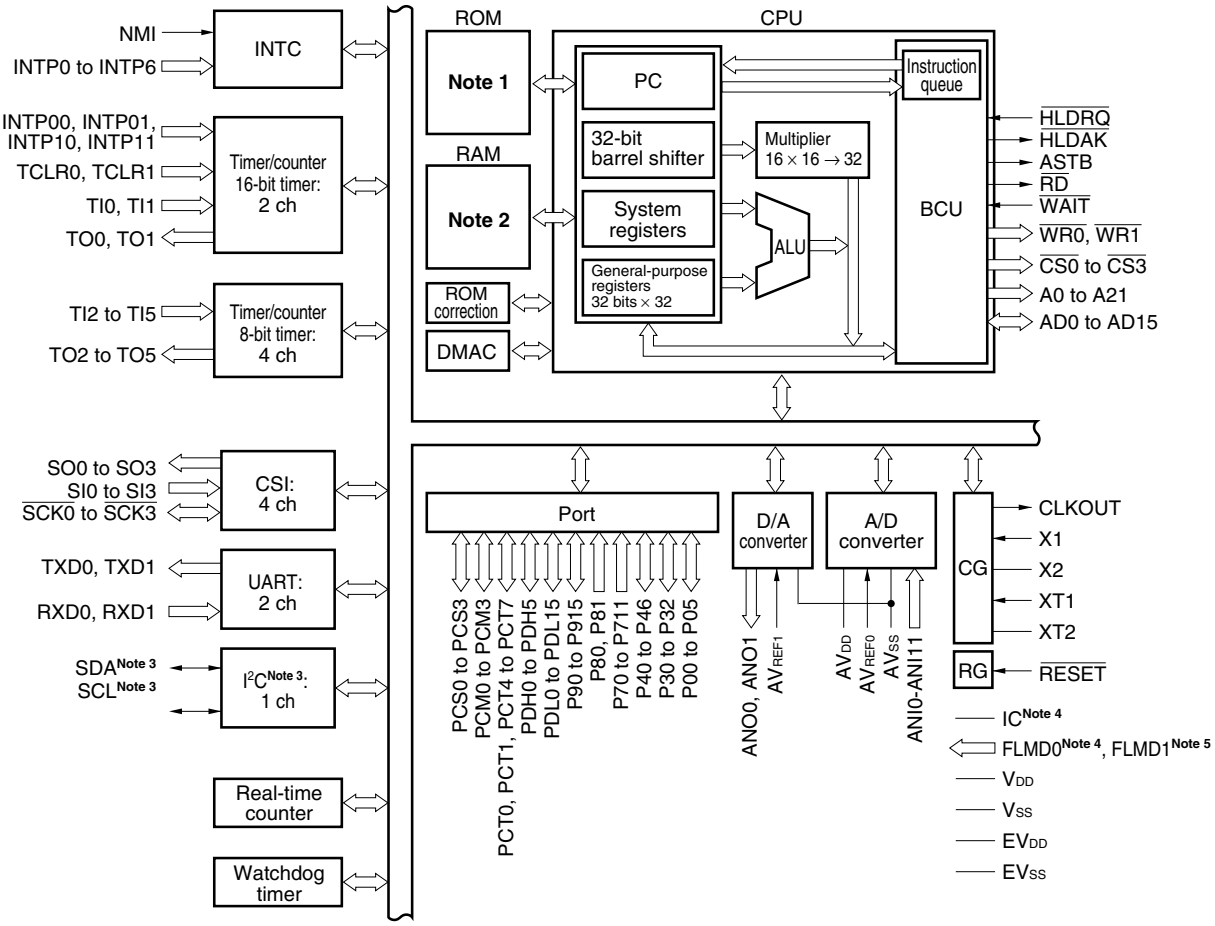
Notes 1. FLMD0 and FLMD1 are valid only in the μPD70F3204 and 70F3204Y.

2. IC: Directly connect this pin to V_{SS} (μPD703204 and 703204Y).
FLMD0: Connect this pin to V_{SS} in the normal operation mode (μPD70F3204 and 70F3204Y).

1.6 Function Block Configuration

1.6.1 Internal block diagram

- V850ES/SA2



Notes 1. μPD703200, 703200Y: 128 KB (mask ROM)
μPD703201, 703201Y: 256 KB (mask ROM)
μPD70F3201, 70F3201Y: 256 KB (flash memory)

2. μPD703200, 703200Y: 8 KB
μPD703201, 703201Y, 70F3201, 70F3201Y: 16 KB

3. μPD703200Y, 703201Y, and 70F3201Y only

4. μPD703200, 703200Y, 703201, and 703201Y only

5. μPD70F3201 and 70F3201Y only

3.2 CPU Register Set

The registers of the V850ES/SA2 and V850ES/SA3 can be classified into two types: general-purpose program registers and dedicated system registers. All the registers are 32 bits wide.

For details, refer to the **V850ES Architecture User's Manual**.

(1) Program register set

31	0
r0	(Zero register)
r1	(Assembler-reserved register)
r2	
r3	(Stack pointer (SP))
r4	(Global pointer (GP))
r5	(Text pointer (TP))
r6	
r7	
r8	
r9	
r10	
r11	
r12	
r13	
r14	
r15	
r16	
r17	
r18	
r19	
r20	
r21	
r22	
r23	
r24	
r25	
r26	
r27	
r28	
r29	
r30	(Element pointer (EP))
r31	(Link pointer (LP))

31	0
PC	(Program counter)

(2) System register set

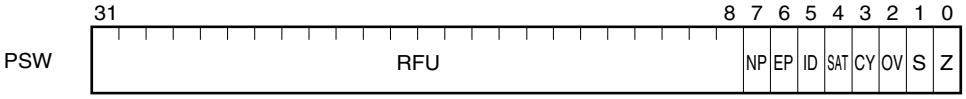
31	0
EIPC	(Interrupt status saving register)
EIPSW	(Interrupt status saving register)
FEPC	(NMI status saving register)
FEPSW	(NMI status saving register)
ECR	(Interrupt source register)
PSW	(Program status word)
CTPC	(CALLT execution status saving register)
CTPSW	(CALLT execution status saving register)
DBPC	(Exception/debug trap status saving register)
DBPSW	(Exception/debug trap status saving register)
CTBP	(CALLT base pointer)

(4) Program status word (PSW)

The program status word (PSW) is a collection of flags that indicate the status of the program (result of instruction execution) and the status of the CPU.

If the contents of a bit of this register are changed by using the LDSR instruction, the new contents are validated immediately after completion of LDSR instruction execution. If the ID flag is set to 1, however, interrupt request acknowledgment is disabled even while the LDSR instruction is being executed.

Bits 31 to 8 of this register are reserved for future function expansion (these bits are fixed to 0).



Bit position	Flag name	Meaning
31 to 8	RFU	Reserved field. Fixed to 0.
7	NP	Indicates that a non-maskable interrupt (NMI) is being serviced. This bit is set to 1 when an NMI request is acknowledged, disabling multiple interrupts. 0: NMI is not being serviced. 1: NMI is being serviced.
6	EP	Indicates that an exception is being processed. This bit is set to 1 when an exception occurs. Even if this bit is set, interrupt requests are acknowledged. 0: Exception is not being processed. 1: Exception is being processed.
5	ID	Indicates whether a maskable interrupt can be acknowledged. 0: Interrupt enabled (EI) 1: Interrupt disabled (DI)
4	SAT[Note]	Indicates that the result of a saturation operation has overflowed and is saturated. Because this is a cumulative flag, it is set to 1 when the result of a saturation operation instruction is saturated, and is not cleared to 0 even if the subsequent operation result is not saturated. Use the LDSR instruction to clear this bit. This flag is neither set to 1 nor cleared to 0 by execution of an arithmetic operation instruction. 0: Not saturated 1: Saturated
3	CY	Indicates whether a carry or a borrow occurs as a result of an operation. 0: Carry or borrow does not occur. 1: Carry or borrow occurs.
2	OV[Note]	Indicates whether an overflow occurs during operation. 0: Overflow does not occur. 1: Overflow occurs.
1	S[Note]	Indicates whether the result of an operation is negative. 0: The result is positive or 0. 1: The result is negative.
0	Z	Indicates whether the result of an operation is 0. 0: The result is not 0. 1: The result is 0.

Remark Also read **Note** on the next page.

(c) Port mode control register 0 (PMC0)

This is an 8-bit register that specifies the port mode or control mode.

This register can be read or written in 8-bit or 1-bit units.

After reset: 00H R/W Address: FFFFF440H

	7	6	5	4	3	2	1	0
PMC0	0	0	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00

PMC05	Specifies operation mode of P05 pin
0	I/O port
1	INTP4 input

PMC04	Specifies operation mode of P04 pin
0	I/O port
1	INTP3/TI5 input

PMC03	Specifies operation mode of P03 pin
0	I/O port
1	INTP2/TI4 input

PMC02	Specifies operation mode of P02 pin
0	I/O port
1	INTP1/TI3 input

PMC01	Specifies operation mode of P01 pin
0	I/O port
1	INTP0/TI2 input

PMC00	Specifies operation mode of P00 pin
0	I/O port
1	NMI input

Caution A register for selects external interrupts (INTP0 to INTP3) and timer inputs (TI2 to TI5) is not provided.

When using port 0 to input an external interrupt, specify the valid edge of the interrupt request by using the INTR0/INTF0 register. When using the port for timer input, specify the valid edge of TIn by using the TCLn register.

- **INTR0: External interrupt rising edge specification register 0 (Refer to 4.3.1 (2) (f).)**
- **INTF0: External interrupt falling edge specification register 0 (Refer to 4.3.1 (2) (e).)**
- **TCLn: Timer n clock select register (refer to CHAPTER 8 8-BIT TIEMR/EVENT COUNTERS 2 TO 5)**

(c) Port mode control register DH (PMCDH)

This is an 8-bit register that specifies the port mode or control mode.

It can be read or written in 8-bit or 1-bit units.

After reset: 00H R/W Address: FFFFF046H

	7	6	5	4	3	2	1	0
PMCDH	PMCDH7[Note]	PMCDH6[Note]	PMCDH5	PMCDH4	PMCDH3	PMCDH2	PMCDH1	PMCDH0

PMCDHn	Specifies operation mode of PDHn pin (V850ES/SA2: n = 0 to 5, V850ES/SA3: n = 0 to 7)
0	I/O port
1	Am output (address bus output) (V850ES/SA2: m = 16 to 21, V850ES/SA3: m = 16 to 23)

Note Bits 7 and 6 are provided in the V850ES/SA3 only. Be sure to clear these bits to 0 in the V850ES/SA2.

(a) Transfer rate selection example

CKSn2	CKSn1	CKSn0	Baud Rate (bps)					
			20 MHz Operation	17 MHz Operation	13.5 MHz Operation	10 MHz Operation	8 MHz Operation	4 MHz Operation
0	0	0	Setting prohibited	Setting prohibited	Setting prohibited	5,000,000	4,000,000	2,000,000
0	0	1	5,000,000	4,250,000	3,375,000	2,500,000	2,000,000	1,000,000
0	1	0	2,500,000	2,125,000	1,687,500	1,250,000	1,000,000	500,000
0	1	1	1,250,000	1,062,500	843,750	625,000	500,000	250,000
1	0	0	625,000	531,250	421,875	312,500	250,000	125,000
1	0	1	312,500	265,625	210,938	156,250	125,000	62,500

(6) Serial clock counter

This counter counts the serial clocks that are output and the serial clocks that are input during transmit/receive operations and is used to verify that 8-bit data was sent or received.

(7) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIIC).

An I^2C interrupt is generated following either of two triggers.

- Eighth or ninth clock of the serial clock (set by WTIM bit[Note])
- Interrupt request generated when a stop condition is detected (set by SPIE bit[Note])

Note WTIM bit: Bit 3 of IIC control register (IICC)
SPIE bit: Bit 4 of IIC control register (IICC)

(8) Serial clock controller

In master mode, this circuit generates the clock output via the SCL pin from a sampling clock.

(9) Serial clock wait controller

This circuit controls the wait timing.

(10) ACK output circuit, stop condition detector, start condition detector, and ACK detector

These circuits are used to output and detect various control signals.

(11) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(4) Acknowledge signal ($\overline{\text{ACK}}$)

The acknowledge signal ($\overline{\text{ACK}}$) is used by the transmitting and receiving devices to confirm serial data reception.

The receiving device returns one $\overline{\text{ACK}}$ signal for each 8 bits of data it receives. The transmitting device normally receives an $\overline{\text{ACK}}$ signal after transmitting 8 bits of data. However, when the master device is the receiving device, it does not output an $\overline{\text{ACK}}$ signal after receiving the final data to be transmitted. The transmitting device detects whether or not an $\overline{\text{ACK}}$ signal is returned after it transmits 8 bits of data. When an $\overline{\text{ACK}}$ signal is returned, the reception is judged as normal and processing continues. If the slave device does not return an $\overline{\text{ACK}}$ signal, the master device outputs either a stop condition or a restart condition and then stops the current transmission. Failure to return an $\overline{\text{ACK}}$ signal may be caused by the following two factors.

<1> Reception was not correctly performed.

<2> The final data was received.

When the receiving device sets the SDA line to low level during the ninth clock, the $\overline{\text{ACK}}$ signal becomes active (normal receive response).

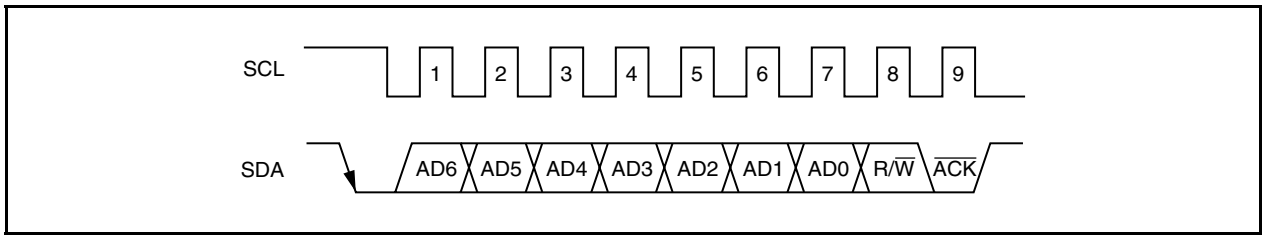
When bit 2 (ACKE) of the IIC control register (IICC) is set to 1, automatic $\overline{\text{ACK}}$ signal generation is enabled.

Transmission of the eighth bit following the 7 address data bits causes bit 3 (TRC) of the IIC status register (IICS) to be set. When the TRC bit's value is 0, it indicates receive mode. Therefore, ACKE should be set to 1.

When the slave device is receiving (when TRC = 0), if the slave device does not need to receive any more data after receiving several bytes, setting ACKE to 0 will prevent the master device from starting transmission of the subsequent data.

Similarly, when the master device is receiving (when TRC = 0) and the subsequent data is not needed and when either a restart condition or a stop condition should therefore be output, setting ACKE to 0 will prevent the $\overline{\text{ACK}}$ signal from being returned. This prevents the MSB data from being output via the SDA line (i.e., stops transmission) during transmission from the slave device.

Figure 15-10. $\overline{\text{ACK}}$ Signal



When the local address is received, an $\overline{\text{ACK}}$ signal is automatically output in synchronization with the falling edge of the eighth clock of SCL regardless of the ACKE bit value. No $\overline{\text{ACK}}$ signal is output if the received address is not a local address.

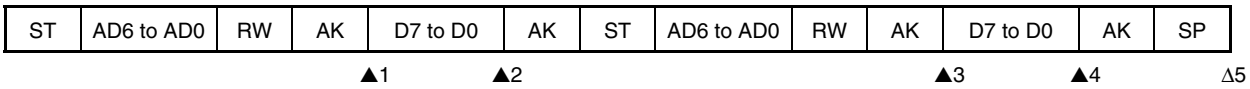
The $\overline{\text{ACK}}$ signal output method during data reception is based on the wait timing setting, as described below.

When 8-clock wait is selected: The $\overline{\text{ACK}}$ signal is output at the falling edge of the eighth clock of SCL if ACKE is set to 1 before wait cancellation.

When 9-clock wait is selected: The $\overline{\text{ACK}}$ signal is automatically output at the falling edge of the eighth clock of SCL if ACKE has already been set to 1.

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIM = 0 (after restart, matches with SVA)



▲1: IICS = 0001X110B

▲2: IICS = 0001X000B

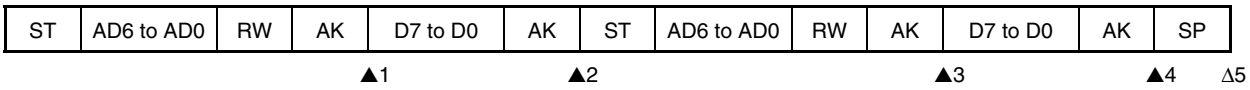
▲3: IICS = 0001X110B

▲4: IICS = 0001X000B

Δ 5: IICS = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE = 1
X: Don't care

<2> When WTIM = 1 (after restart, matches with SVA)



▲1: IICS = 0001X110B

▲2: IICS = 0001XX00B

▲3: IICS = 0001X110B

▲4: IICS = 0001XX00B

Δ 5: IICS = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE = 1
X: Don't care

15.12 Wakeup Function

The I²C bus slave function is a function that generates an interrupt request (INTIIC) when a local address and extension code have been received.

This function makes processing more efficient by preventing unnecessary interrupt requests from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has output a start condition) to a slave device.

However, when a stop condition is detected, bit 5 (SPIE) of the IIC control register (IICC) is set regardless of the wakeup function, and this determines whether interrupt requests are enabled or disabled.

CHAPTER 16 DMA FUNCTIONS (DMA CONTROLLER)

The V850ES/SA2 and V850ES/SA3 include a direct memory access (DMA) controller (DMAC) that executes and controls DMA transfer.

The DMAC controls data transfer between memory and I/O, between memories, or between I/Os based on DMA requests issued by the on-chip peripheral I/O (serial interface, real-time pulse unit, and A/D converter), interrupts from external input pins, or software triggers (memory refers to internal RAM or external memory).

16.1 Features

- 4 independent DMA channels
- Transfer unit: 8/16 bits
- Maximum transfer count: 65,536 (2^{16})
- Transfer type: Two-cycle transfer
- Transfer mode: Single transfer mode
- Transfer requests
  - Request by interrupts from on-chip peripheral I/O (serial interface, timer/counter, A/D converter) or interrupts from external input pin
  - Requests by software trigger
- Transfer objects
  - Internal RAM ↔ internal peripheral I/O
  - Peripheral I/O ↔ internal peripheral I/O
  - Internal RAM ↔ external memory
  - External memory ↔ internal peripheral I/O
  - External memory ↔ external memory

16.3.5 DMA channel control registers 0 to 3 (DCHC0 to DCHC3)

These 8-bit registers are used to control the DMA transfer operating mode for DMA channel n (n = 0 to 3).

These registers can be read or written in 8-bit or 1-bit units. (However, bit 7 is read-only and bits 1 and 2 are write-only. If bit 1 or 2 is read, the read value is always 0.)

After reset: 00H R/W Address: DCHC0 FFFFF0E0H, DCHC1 FFFFF0E2H, DCHC2 FFFFF0E4H, DCHC3 FFFFF0E6H

	<7>	6	5	4	3	<2>	<1>	<0>
DCHCn	TCn Note 1	0	0	0	0	INITn Note 2	STGn Note 2	Enn

(n = 0 to 3)

TCn	Status flag indicates whether DMA transfer through DMA channel n has ended or not
0	DMA transfer had not ended.
1	DMA transfer had ended.
It is set to 1 when DMA transfer ends and cleared (to 0) when it is read.	

INITn	When changing the DDAnH, DDAnL, DSAnL, DSAnH, or DBCn register before the number of transfers set by DBCn has finished, set this bit to 1 to initialize DMA.
Set the INIT bit to 1 when the Enn bit is 0.	

STGn	If this bit is set to 1 in the DMA transfer enable state (TCn bit = 0, Enn bit = 1), DMA transfer is started.

Enn	Setting of whether DMA transfer through DMA channel n is to be enabled or disabled
0	DMA transfer disabled
1	DMA transfer enabled
This bit is cleared to 0 when DMA transfer ends.	

Notes 1. The TCn bit is read-only.

2. The INITn and STGn bits are write-only.

Caution Before generating a DMA transfer request by software, make sure that the TCn bit is set to 1 and then clear the TCn bit to 0.

Remark If the completion of DMA transfer and the bit manipulation instruction for the DCHCn register conflict, the Enn bit may not be cleared.

CHAPTER 17 INTERRUPT/EXCEPTION PROCESSING FUNCTION

The V850ES/SA2 and V850ES/SA3 are provided with a dedicated interrupt controller (INTC) for interrupt servicing and can process a total of 38 to 40 interrupt requests.

An interrupt is an event that occurs independently of program execution, and an exception is an event whose occurrence is dependent on program execution.

The V850ES/SA2 and V850ES/SA3 can process interrupt requests from the on-chip peripheral hardware and external sources. Moreover, exception processing can be started by the TRAP instruction (software exception) or by generation of an exception event (i.e. fetching of an illegal opcode) (exception trap).

17.1 Features

○ Interrupts
- External interrupts: 8 sources (including NMI)
- Internal interrupts:
  μPD703200, 703201, 70F3201: 30 sources
  μPD703200Y, 703201Y, 70F3201Y: 31 sources
  μPD703204, 70F3204: 31 sources
  μPD703204Y, 70F3204Y: 32 sources
- 8 levels of programmable priorities (maskable interrupts)
- Multiple interrupt control according to priority
- Masks can be specified for each maskable interrupt request.
- Noise elimination, edge detection, and valid edge specification for external interrupt request signals.

○ Exceptions
- Software exceptions: 32 sources
- Exception trap: 2 sources (illegal opcode exception, debug trap)

Interrupt/exception sources are listed in Table 17-1.

17.3.4 Interrupt control register (xxICn)

An interrupt control register is assigned to each interrupt request (maskable interrupt) and sets the control conditions for each maskable interrupt request.

This register can be read or written in 8-bit or 1-bit units.

This register is set to 47H after reset.

★ **Caution Read the xxIFn bit of the xxICn register with interrupts disabled (DI). If the xxIFn bit is read with interrupts enabled (EI), a normal value may not be read when the timing of interrupt acknowledgment and reading of the bit conflict.**

After reset: 47H R/W Address: FFFFF110H to FFFFF15AH

	<7>	<6>	5	4	3	2	1	0
xxICn	xxIFn	xxMKn	0	0	0	xxPRn2	xxPRn1	xxPRn0

xxIFn	Interrupt request flag[Note]
0	Interrupt request not issued
1	Interrupt request issued

xxMKn	Interrupt mask flag
0	Interrupt servicing enabled
1	Interrupt servicing disabled (pending)

xxPRn2	xxPRn1	xxPRn0	Interrupt priority specification bit
0	0	0	Specifies level 0 (highest).
0	0	1	Specifies level 1.
0	1	0	Specifies level 2.
0	1	1	Specifies level 3.
1	0	0	Specifies level 4.
1	0	1	Specifies level 5.
1	1	0	Specifies level 6.
1	1	1	Specifies level 7 (lowest).

Note The flag xxIFn is reset automatically by the hardware if an interrupt request is acknowledged.

Remark xx: Identification name of each peripheral unit (OV, P00 to P03, P10 to P13, CM, DMA, CSI, SE, SR, ST, AD)

n: Peripheral unit number (None or 0 to 3).

The addresses and bits of the interrupt control registers are as follows.

CHAPTER 18 STANDBY FUNCTION

18.1 Overview

The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. The available standby modes are listed in Table 18-1.

Table 18-1. Standby Modes

Mode	Functional Outline
HALT mode	Mode to stop only the operating clock of the CPU
IDLE mode	Mode to stop all the internal operations of the chip except the oscillator
Software STOP mode	Mode to stop all the internal operations of the chip except the subclock oscillator
Subclock operation mode	Mode to use the subclock as the internal system clock
Sub-IDLE mode	Mode to stop all the internal operations of the chip, except the oscillator, in the subclock operation mode

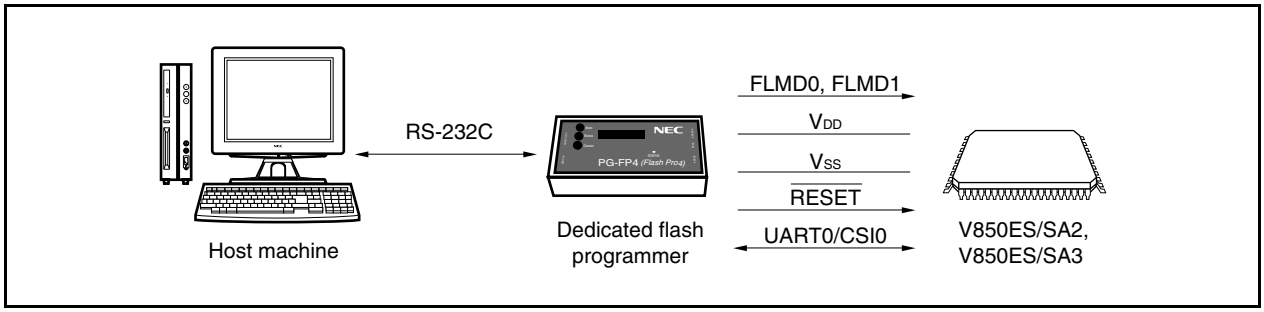
★ **Table 21-5. Wiring of V850ES/SA3 Flash Write Adapter (FA-121F1-EA6-A)**

Pin Configuration of Flash Programmer (PG-FP3/PG-FP4)			With CSI0 + HS		With CSI0		With UART0	
Signal Name	I/O	Pin Function	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD	Input	Receive signal	P41/SO0/SDA	A12	P41/SO0/SDA	A12	P31/SO1/TXD0	E2
SO/TxD	Output	Transmit signal	P40/SI0	B12	P40/SI0	B12	P30/SI1/RXD0	E1
SCK	Output	Transfer clock	P42/$\overline{SCK0}$/SCL	B11	P42/$\overline{SCK0}$/SCL	B11	Not needed	Not needed
CLK	Output	Clock to V850ES/SA3	X1	F2	X1	F2	X1	F2
/RESET	Output	Reset signal	$\overline{RESET}$	G1	$\overline{RESET}$	G1	$\overline{RESET}$	G1
FLMD0	Output	Write voltage	FLMD0	H12	FLMD0	H12	FLMD0	H12
FLMD1	Output	Write voltage	PDL5/AD5/FLMD1	J11	PDL5/AD5/FLMD1	J11	PDL5/AD5/FLMD1	J11
HS	Input	Handshake signal for CSI0 + HS	PDH0/A16	D11	Not needed	Not needed	Not needed	Not needed
VDD	–	VDD voltage generation/ voltage monitor	V_{DD}	F3, H2	V_{DD}	F3, H2	V_{DD}	F3, H2
			AV_{DD}	B1	AV_{DD}	B1	AV_{DD}	B1
			EV_{DD}	G13, L6	EV_{DD}	G13, L6	EV_{DD}	G13, L6
GND	–	Ground	V_{SS}	F1, H1	V_{SS}	F1, H1	V_{SS}	F1, H1
			AV_{SS}	C2	AV_{SS}	C2	AV_{SS}	C2
			AV_{REF0}	B2	AV_{REF0}	B2	AV_{REF0}	B2
			AV_{REF1}	D2	AV_{REF1}	D2	AV_{REF1}	D2
			EV_{SS}	G11, M5	EV_{SS}	G11, M5	EV_{SS}	G11, M5

21.3 Programming Environment

The following shows the environment required for writing programs to the flash memory of V850ES/SA2 and V850ES/SA3.

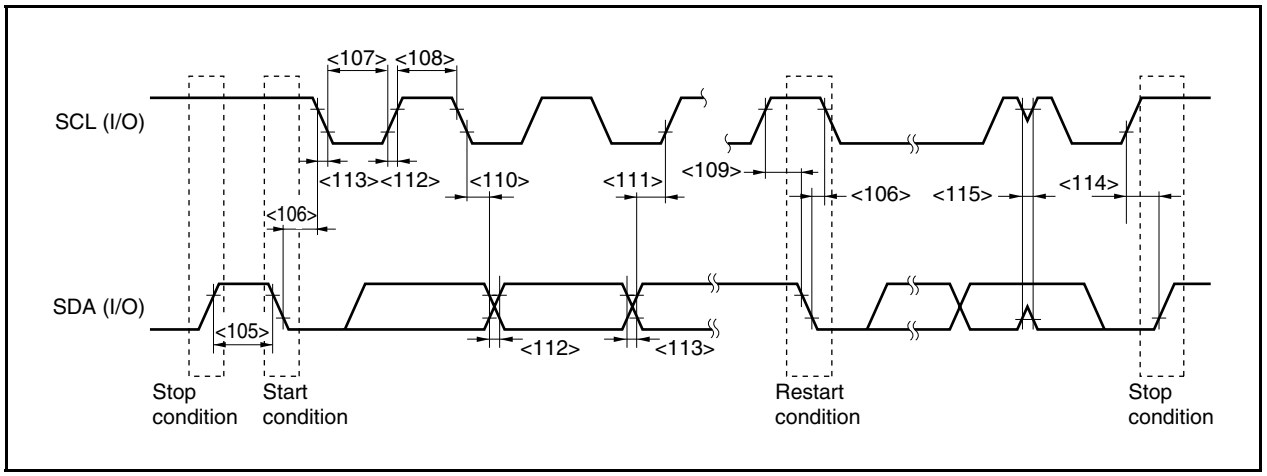
Figure 21-3. Environment Required for Writing Programs to Flash Memory



A host machine is required for controlling the dedicated flash programmer.

UART0 or CSI0 is used for the interface between the dedicated flash programmer and the V850ES/SA2 or V850ES/SA3 to perform writing, erasing, etc. A dedicated program adapter (FA Series) required for off-board writing.

I²C bus mode (μPD703200Y, 703201Y, 703204Y, 70F3201Y, 70F3204Y only)



A/D converter

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF0} = 2.2 to 2.7 V, AV_{SS} = V_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note 1]				±0.1	±0.3	%FSR
Conversion time	t_{CONV}		6.3		150	μs
Zero-scale error[Note 1]					±0.2	%FSR
Full-scale error[Note 1]					±0.2	%FSR
Integral linearity error[Note 2]					±2	LSB
Differential linearity error[Note 2]					±1	LSB
Analog reference voltage	AV_{REF}	$AV_{REF0} = AV_{DD}$	2.2		2.7	V
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF0} current	AI_{REF0}			10		μA
AV_{DD} power supply current	AI_{DD}			400	800	μA

Notes 1. Excluding quantization error (±0.05%FSR)

2. Excluding quantization error (±0.5 LSB)

Remark LSB: Least significant bit
FSR: Full-scale range