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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, PWM, WDT
Number of I/O	68
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 2.7V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3201ygc-yeu-a

(10) Serial interface (SIO)

The V850ES/SA2 and V850ES/SA3 have asynchronous serial interfaces (UART0 and UART1), clocked serial interfaces (V850ES/SA2: CSI0 to CSI3, V850ES/SA3: CSI0 to CSI4), and an I^2C bus interface (I^2C) as the serial interfaces. The V850ES/SA2 can use up to four channels, and the V850ES/SA3 can use up to five channels at the same time. Of these channels, one can be switched between UART and CSI, and another can be switched between CSI and I^2C.

UART0 and UART1 transfer data using the TXD0, TXD1, RXD0, and RXD1 pins.

CSI0 to CSI3 transfer data using the SO0 to SO3, SI0 to SI3, and $\overline{SCK0}$ to $\overline{SCK3}$ pins.

CSI4 transfers data using the SO4, SI4, and $\overline{SCK4}$ pins (V850ES/SA3 only).

I^2C transfers data using the SDA and SCL pins.

I^2C is provided only in the μPD703200Y, 703201Y, 703204Y, 70F3201Y, and 70F3204Y.

UART includes a dedicated baud rate generator.

(11) A/D converter

The V850ES/SA2 and V850ES/SA3 have a high-speed high-resolution, 10-bit A/D converter with 12 and 16 analog input pins, respectively. The A/D converter in both products is a successive approximation type.

(12) D/A converter

A two-channel 8-bit resolution R-string D/A converter is provided.

(13) DMA controller

A DMA controller with four channels is provided. This DMA controller transfers data between the internal RAM, on-chip peripheral I/O, and external memory, in response to interrupt requests from the on-chip peripheral I/O.

(14) ROM correction

This is a function to replace part of the program in the mask ROM with program in the internal RAM for execution. The program can be corrected at up to four places.

(3) P30 to P32 (Port 3) … 3-state I/O

Port 3 is a 3-bit I/O port that can be set to the input or output mode in 1-bit units.

Besides functioning as I/O port pins, P30 to P32 also operate as the I/O pins of the serial interface.

These pins can be set to the port or control mode in 1-bit units.

The output mode of P31 and P32 can also be set to normal output or N-ch open-drain output.

(a) Port mode

P30 to P32 can be set to the input or output mode in 1-bit units by using port mode register 3 (PM3).

(b) Control mode

(i) SI1 (serial input 1) … Input

This pin inputs the serial receive data of CSI1.

(ii) SO1 (serial output 1) … Output

This pin outputs the serial transmit data of CSI1.

(iii) $\overline{\text{SCK1}}$ (serial clock 1) … 3-state I/O

This is the serial clock I/O pin of CSI1.

(iv) RXD0 (receive data 0) … Input

This pin inputs the serial receive data of UART0.

(v) TXD0 (transmit data 0) … Output

This pin outputs the serial transmit data of UART0.

(4) P40 to P46 (Port 4) … 3-state I/O

Port 4 is a 7-bit I/O port that can be set to the input or output mode in 1-bit units.

Besides functioning as I/O port pins, P40 to P46 also operate as the I/O pins of the timer/counters and serial interface, and as the external interrupt request input pin. These pins can be set to the port or control mode in 1-bit units.

The output mode of P41 and P42 can also be set to normal output or N-ch open-drain output.

(a) Port mode

P40 to P46 can be set to the input or output mode in 1-bit units by using port mode register 4 (PM4).

(b) Control mode

(i) TI0, TI1 (timer input 0, 1) … Input

These pins input an external count clock to timers 0 and 1.

(ii) TO0, TO1 (timer output 0, 1) … Output

These pins output a pulse signal from timers 0 and 1.

(iii) TCLR0, TCLR1 (timer clear input 0, 1) … Input

These pins input an external clear signal to timers 0 and 1.

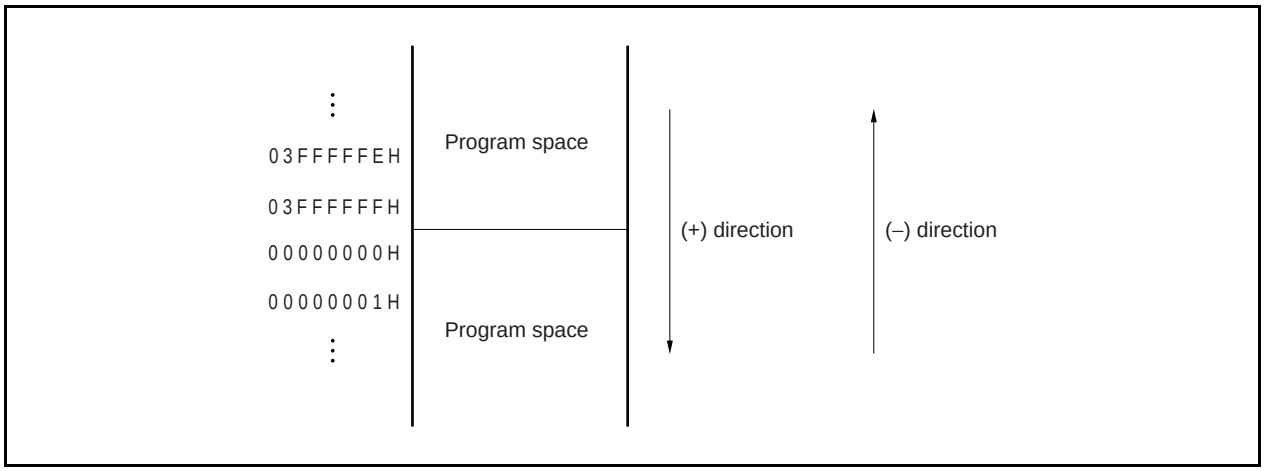
3.4.3 Wrap-around of CPU address space

(1) Program space

Of the 32 bits of the PC (program counter), the higher 6 bits are fixed to 0 and only the lower 26 bits are valid. The higher 6 bits ignore a carry or borrow from bit 25 to 26 during branch address calculation.

Therefore, the lowest address of the program space, 00000000H, and the highest address, 03FFFFFFH, are contiguous addresses. That the lowest address and the highest address of the program space are contiguous in this way is called wrap-around.

Caution Because the 4 KB area of addresses 03FFF000H to 03FFFFFFH is an internal peripheral I/O area, instructions cannot be fetched from this area. Therefore, do not execute an operation in which the result of a branch address calculation affects this area.



(2) Data space

The result of an operand address calculation operation that exceeds 32 bits is ignored.

Therefore, the lowest address of the data space, 00000000H, and the highest address, FFFFFFFFH, are contiguous, and wrap-around occurs at the boundary of these addresses.

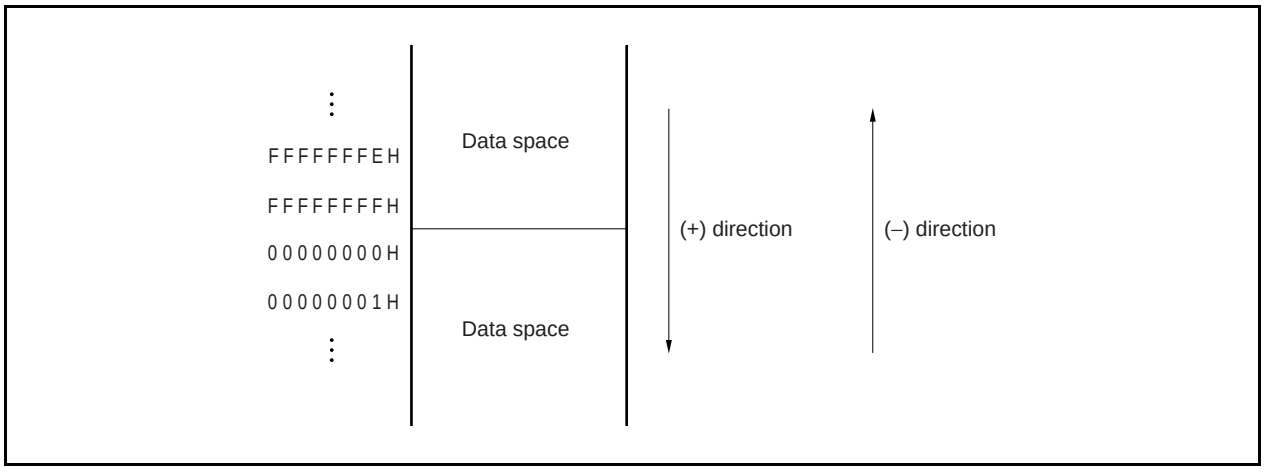
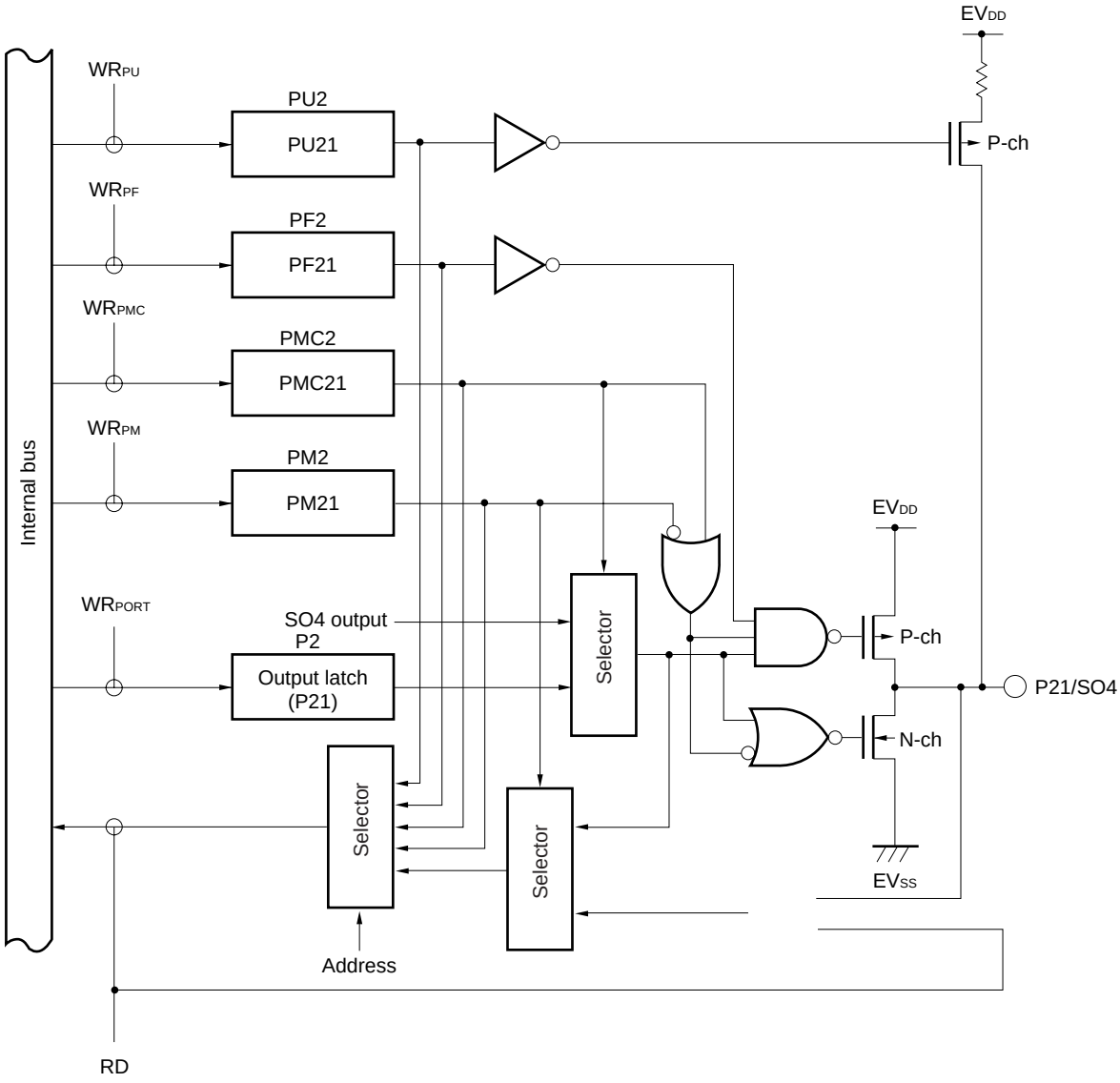


Figure 4-6. Block Diagram of P21



4.3.3 Port 3

Port 3 can be set to the input or output mode in 1-bit units.

The number of I/O port bits of each product is the same.

Commercial Name	Number of I/O Port Bits
V850ES/SA2	3-bit I/O port
V850ES/SA3	3-bit I/O port

(1) Functions of port 3

- ○ Input/output data can be specified in 1-bit units by using port register 3 (P3).
- ○ Can be set to the input or output mode in 1-bit units by using port mode register 3 (PM3).
- ○ Can be set to the port mode or control mode (alternate function) in 1-bit units by using port mode control register 3 (PMC3).
- ○ Control mode 1 or control mode 2 can be specified in 1-bit units by using port function control register 3 (PFC3).
- ○ N-ch open-drain output can be set in 1-bit units by using port function register 3 (PF3).
- ○ An internal pull-up resistor can be connected in 1-bit units by using pull-up resistor option register 3 (PU3).

Port 3 has an alternate function as the following pins.

Table 4-6. Alternate-Function Pins of Port 3

Pin Name		Alternate-Function Pin	I/O	PULL[Note]	Remark
Port 3	P30	SI1/RXD0	I/O	Provided	–
	P31	SO1/TXD0			N-ch open-drain output selectable
	P32	$\overline{\text{SCK0}}$			

Note Software pull-up function

(2) Registers

(a) Port register CD (PCD)

Port register CD (PCD) is an 8-bit register that controls reading the pin level and writing the output level. This register can be read or written in 8-bit or 1-bit units.

After reset: Undefined R/W Address: FFFFF00EH

	7	6	5	4	3	2	1	0
PCD	0	0	0	0	PCD3	PCD2	PCD1	0

PCDn	Controls output data (in output mode) (n = 1 to 3)
0	Outputs 0.
1	Outputs 1.

Remarks 1. In input mode: When port CD (PCD) is read, the pin level at that time is read. When written, the data written to PCD is written. The input pin is not affected.

In output mode: When port CD (PCD) is read, the value of PCD is read. When a value is written to PCD, it is immediately output.

2. After reset, an undefined value (pin input level) is read from PCD in the input mode. When PCD is

4.3.13 Port DL

Port DL can be set to the input or output mode in 1-bit units.

The number of I/O port bits of each product is the same.

Commercial Name	Number of I/O Port Bits
V850ES/SA2	16-bit I/O port
V850ES/SA3	16-bit I/O port

(1) Functions of port DL

- ○ Input/output data can be specified in 1-bit units by using port register DL (PDL).
- ○ Can be set to the input or output mode in 1-bit units by using port mode register DL (PMDL).
- ○ Can be set to the port mode or control mode (alternate function) in 1-bit units by using port mode control register DL (PMCDL).

Port DL has an alternate function as the following pins.

Table 4-17. Alternate-Function Pins of Port DL

Pin Name		Alternate-Function Pin	I/O	PULL[Note 1]	Remark
	PDL0	AD0			
	PDL1	AD1			
	PDL2	AD2			
	PDL3	AD3			
	PDL4	AD4			
	PDL5	AD5/FLMD1[Note 2]			
	PDL6	AD6			
	PDL7	AD7			
	PDL8	AD8			
	PDLDL	AD9			
	PDL10	AD10			

13.1 Features

- Transfer rate: 300 bps to 312.5 kbps (using a dedicated baud rate generator and an internal system clock of 20 MHz)
- Full-duplex communications
  - On-chip receive buffer register n (RXBn)
  - On-chip transmit buffer register n (TXBn)
- Two-pin configuration
  - TXDn: Transmit data output pin
  - RXDn: Receive data input pin
- Reception error detection functions
  - Parity error
  - Framing error
  - Overrun error
- Interrupt sources: 3 types
  - Reception error interrupt (INTSREn): Interrupt is generated according to the logical OR of the three types of reception errors
  - Reception completion interrupt (INTSRn): Interrupt is generated when receive data is transferred from the shift register to receive buffer register n after serial transfer is completed during a reception enabled state
  - Transmission completion interrupt (INTSTn): Interrupt is generated when the serial transmission of transmit data (8 or 7 bits) from the shift register is completed
- The character length of transmit/receive data is specified by the ASIMn register
- Character length: 7 or 8 bits
- Parity functions: Odd, even, 0, or none
- Transmission stop bits: 1 or 2 bits
- On-chip dedicated baud rate generator

Remark n = 0, 1

(3) Slave device operation (when receiving extension code)

(a) Start ~ Code ~ Data ~ Data ~ Stop

<1> When WTIM = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP
			▲1		▲2		▲3	Δ4

▲1: IICS = 0010X010B

▲2: IICS = 0010X000B

▲3: IICS = 0010X000B

Δ 4: IICS = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE = 1
X: Don't care

<2> When WTIM = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP
			▲1	▲2		▲3	▲4	Δ5

▲1: IICS = 0010X010B

▲2: IICS = 0010X110B

▲3: IICS = 0010X100B

▲4: IICS = 0010XX00B

Δ 5: IICS = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIE = 1
X: Don't care

16.3.2 DMA destination address registers 0 to 3 (DDA0 to DDA3)

These registers are used to set the DMA destination address (28 bits each) for DMA channel n (n = 0 to 3). They are divided into two 16-bit registers, DDAnH and DDAnL.

(1) DMA destination address registers 0H to 3H (DDA0H to DDA3H)

These registers can be read or written in 16-bit units.

After reset: Undefined R/W Address: DDA0H FFFFF086H, DDA1H FFFFF08EH, DDA2H FFFFF096H, DDA3H FFFFF09EH

	15	14	13	12	11	10	9	8
DDAnH	IR	0	0	0	0	0	DA25	DA24

7	6	5	4	3	2	1	0
DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16

(n = 0 to 3)

IR	DMA destination address specification
0	External memory, on-chip peripheral I/O
1	Internal RAM

DA25 to DA16	Sets the DMA destination addresses (A25 to A16). During DMA transfer, it stores the next DMA transfer destination address.

(2) DMA destination address registers 0L to 3L (DDA0L to DDA3L)

These registers can be read or written in 16-bit units.

After reset: Undefined R/W Address: DDA0L FFFFF084H, DDA1L FFFFF08CH, DDA2L FFFFF094H, DDA3L FFFFF09CH

	15	14	13	12	11	10	9	8
DDAnL	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

(n = 0 to 3)

DA15 to DA0	Sets the DMA destination addresses (A15 to A0). During DMA transfer, it stores the next DMA transfer destination address.

16.7 Transfer Object

16.7.1 Transfer type and transfer object

Table 13-2 shows the relationship between transfer type and transfer object (√: Transfer enabled, ×: Transfer disabled).

Table 16-2. Relationship Between Transfer Type and Transfer Object

		Destination				
		Internal ROM	On-Chip Peripheral I/O	External I/O	Internal RAM	External Memory
Source	On-chip peripheral I/O	×	√	√	√	√
	External I/O	×	√	√	√	√
	Internal RAM	×	√	√	×	√
	External memory	×	√	√	√	√
	Internal ROM	×	×	×	×	×

Caution The operation is not guaranteed for combinations of transfer destination and source marked with "×" in Table 16-2.

Remark During two-cycle 16-bit transfer, if the data bus width of the transfer source and that of the transfer destination are different, the operation becomes as follows.

In the case of transfer from a 16-bit bus to an 8-bit bus
A 16-bit read cycle is generated and then an 8-bit write cycle is generated twice.

In the case of transfer from an 8-bit bus to a 16-bit bus
An 8-bit read cycle is generated twice and then a 16-bit write cycle is generated.

16.7.2 External bus cycles during DMA transfer (two-cycle transfer)

The external bus cycles during DMA transfer (two-cycle transfer) are shown below.

Table 16-3. External Bus Cycles During DMA Transfer (Two-Cycle Transfer)

Transfer Object	External Bus Cycle	
On-chip peripheral I/O, internal RAM	None[Note]	–
External I/O	Yes	SRAM cycle
External memory	Yes	Memory access cycle set by the BCT register

Note Other external cycles such as a CPU-based bus cycle can be started.

17.3.3 Priorities of maskable interrupts

The V850ES/SA2 and V850ES/SA3 provide multiple interrupt servicing in which an interrupt is acknowledged while another interrupt is being serviced. Multiple interrupts can be controlled by priority levels.

There are two types of priority level control: control based on the default priority levels, and control based on the programmable priority levels that are specified by the interrupt priority level specification bit (xxPRn) of the interrupt control register (xxICn). When two or more interrupts having the same priority level specified by the xxPRn bit are generated at the same time, interrupts are serviced in order depending on the priority level allocated to each interrupt request type (default priority level) beforehand. For more information, refer to **Table 17-1 Interrupt Source List**. The programmable priority control customizes interrupt requests into eight levels by setting the priority level specification flag.

Note that when an interrupt request is acknowledged, the ID flag of PSW is automatically set to 1. Therefore, when multiple interrupts are to be used, clear the ID flag to 0 beforehand (for example, by placing the EI instruction in the interrupt service program) to set the interrupt enable mode.

Remark xx: Identification name of each peripheral unit (AD, BRG, CC, CSI, DMA, IIC, OVF, P, ROV, RTC, SRE, ST, TM, WDT)
n: Peripheral unit number (None or 0 to 3).

18.2 HALT Mode

18.2.1 Setting and operation status

The HALT mode is set when a dedicated instruction (HALT) is executed in the normal operation mode.

In the HALT mode, the clock oscillator continues operating. Only clock supply to the CPU is stopped; clock supply to the other on-chip peripheral functions continues.

As a result, program execution is stopped, and the internal RAM retains the contents before the HALT mode was set. The on-chip peripheral functions that are independent of instruction processing by the CPU continue operating.

Table 18-3 shows the operation status in the HALT mode.

The average power consumption of the system can be reduced by using the HALT mode in combination with the normal operation mode for intermittent operation.

Caution Insert five or more NOP instructions after the HALT instruction.

18.2.2 Releasing HALT mode

The HALT mode is released by a non-maskable interrupt request, an unmasked maskable interrupt request, $\overline{\text{RESET}}$ pin input, and reset by the watchdog timer.

After the HALT mode has been released, the normal operation mode is restored.

(1) Releasing HALT mode by non-maskable interrupt request or unmasked maskable interrupt request

The HALT mode is released by a non-maskable interrupt request or an unmasked maskable interrupt request, regardless of the priority of the interrupt request. If the HALT mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is serviced as follows.

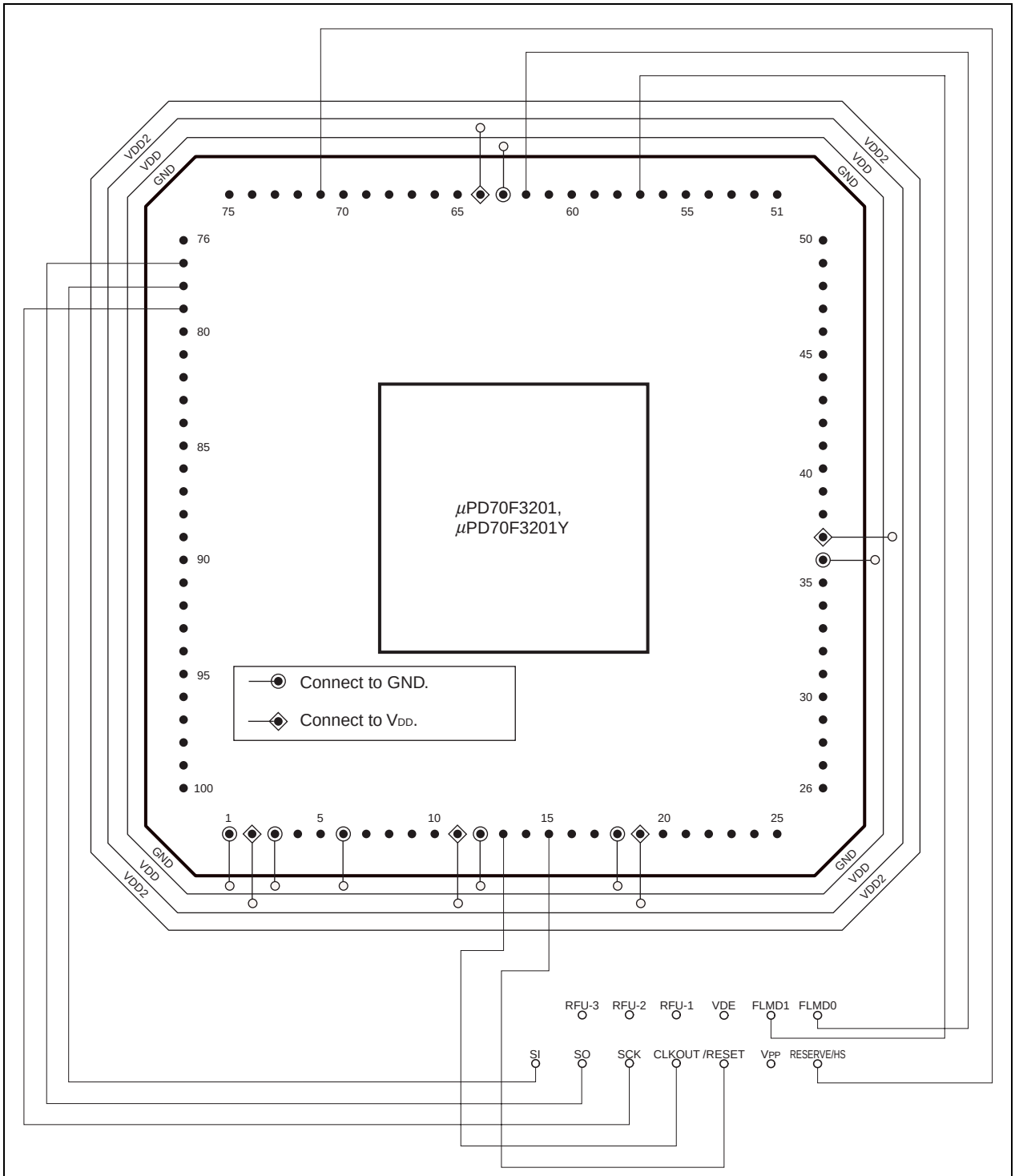
(a) If an interrupt request with a priority lower than that of the interrupt request currently being serviced is issued, only the HALT mode is released, and that interrupt request is not acknowledged. The interrupt request itself is retained.

(b) If an interrupt request with a priority higher than that of the interrupt request currently being serviced is issued (including a non-maskable interrupt request), the HALT mode is released and that interrupt request is acknowledged.

Table 18-2. Operation After Releasing HALT Mode by Interrupt Request

Release Source	Interrupt Enabled (EI) Status	Interrupt Disabled (DI) Status
Non-maskable interrupt request	Execution branches to the handler address	
Maskable interrupt request	Execution branches to the handler address or the next instruction is executed	The next instruction is executed

★ **Figure 21-1. Wiring Example of V850ES/SA2 Flash Write Adapter (FA-100GC-8EU-A)**



Remarks 1. Handle the pins not described above in accordance with the specified handling of unused pins (refer to **2.4 Types of Pin I/O Circuits, I/O Buffer Power Supplies, and Connection of Unused Pins**).

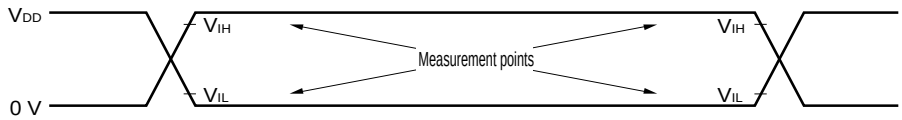
When connecting to V_{DD} via a resistor, use of a resistor of 1 kΩ to 10 kΩ is recommended.

2. This adapter is for a 100-pin plastic LQFP package.

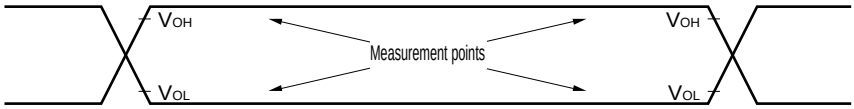
3. This diagram shows the wiring when using a handshake-supporting CSI.

AC characteristics

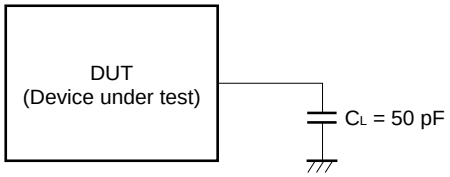
AC test input measurement points (V_{DD}, AV_{DD}, EV_{DD})



AC test output measurement points



Load conditions



Caution If the load capacitance exceeds 50 pF due to the circuit configuration, reduce the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

(5/7)

Symbol	Name	Unit	Page
PFM	Power fail comparison mode register	ADC	285
PFT	Power fail comparison threshold value register	ADC	285
PIC0	Interrupt control register	INTC	441
PIC1	Interrupt control register	INTC	441
PIC2	Interrupt control register	INTC	441
PIC3	Interrupt control register	INTC	441
PIC4	Interrupt control register	INTC	441
PIC5	Interrupt control register	INTC	441
PIC6	Interrupt control register	INTC	441
PM0	Port mode register 0	Port	93
PM2	Port mode register 2	Port	100
PM3	Port mode register 3	Port	107
PM4	Port mode register 4	Port	114
PM9	Port mode register 9	Port	129
PM9H	Port mode register 9H	Port	129
PM9L	Port mode register 9L	Port	129
PMC0	Port mode control register 0	Port	94
PMC2	Port mode control register 2	Port	101
PMC3	Port mode control register 3	Port	108
PMC4	Port mode control register 4	Port	115
PMC9	Port mode control register 9	Port	130
PMC9H	Port mode control register 9H	Port	130
PMC9L	Port mode control register 9L	Port	130
PMCCM	Port mode control register CM	Port	148
PMCCS	Port mode control register CS	Port	154
PMCCT	Port mode control register CT	Port	159
PMCD	Port mode register CD	Port	144
PMCDH	Port mode control register DH	Port	164
PMCDL	Port mode control register DL	Port	168
PMCDLH	Port mode control register DLH	Port	168
PMCDLL	Port mode control register DLL	Port	168
PMCM	Port mode register CM	Port	147
PMCS	Port mode register CS	Port	153
PMCT	Port mode register CT	Port	158
PMDH	Port mode register DH	Port	163
PMDL	Port mode register DL	Port	168
PMDLH	Port mode register DLH	Port	168
PMDLL	Port mode register DLL	Port	168
PRCMD	Command register	CPU	85
PRSCM	Prescaler compare register	CG	211
PRSM	Prescaler mode register	CG	210
PSC	Power save control register	CG	207, 471
PSMR	Power save mode register	CG	207, 471
PSW	Program status word	CPU	59