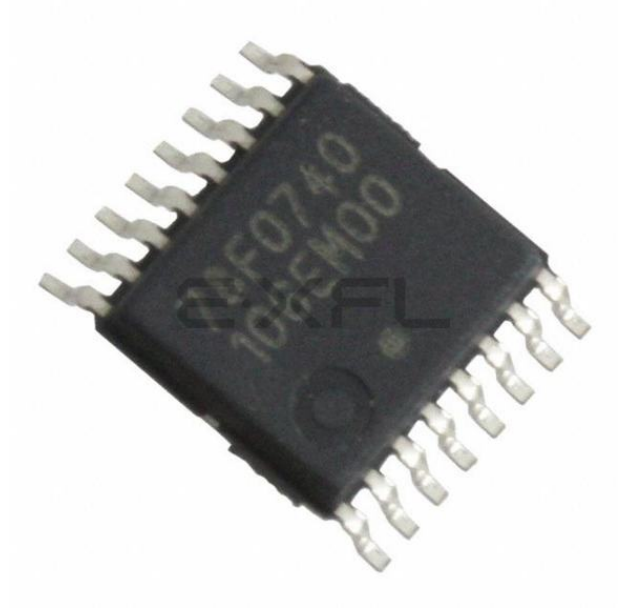
Renesas Electronics America Inc - UPD78F0740MA-FAA-AX Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	9
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0740ma-faa-ax

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

CHAPTER 1 OUTLINE

1.1 Features

○ 78K0 CPU core

○ I/O ports, ROM and RAM capacities

Item / Products	I/O ports	Program Memory (Flash Memory)	Data Memory (Internal High-Speed RAM)
78K0/IY2 (16 pins)	12 (CMOS I/O: 9, CMOS input: 3)	4 KB to 16 KB	384 bytes to 768 bytes
78K0/IA2 (20 pins)	16 (CMOS I/O: 13, CMOS input: 3)	8 KB and 16 KB	512 bytes and 768 bytes
78K0/IB2 (30 pins)	25 (CMOS I/O: 22, CMOS input: 3)		
78K0/IB2 (32 pins)	23 (CMOS I/O: 20, CMOS input: 3)		

○ Low power consumption (V_{DD} = 5.0 V)
- Internal high-speed oscillator operation mode: 350 μA (TYP.) (f_{CPU} = 1 MHz operation)
- STOP mode: 0.58 μA (TYP.) (f_{IL} = 30 kHz operation)

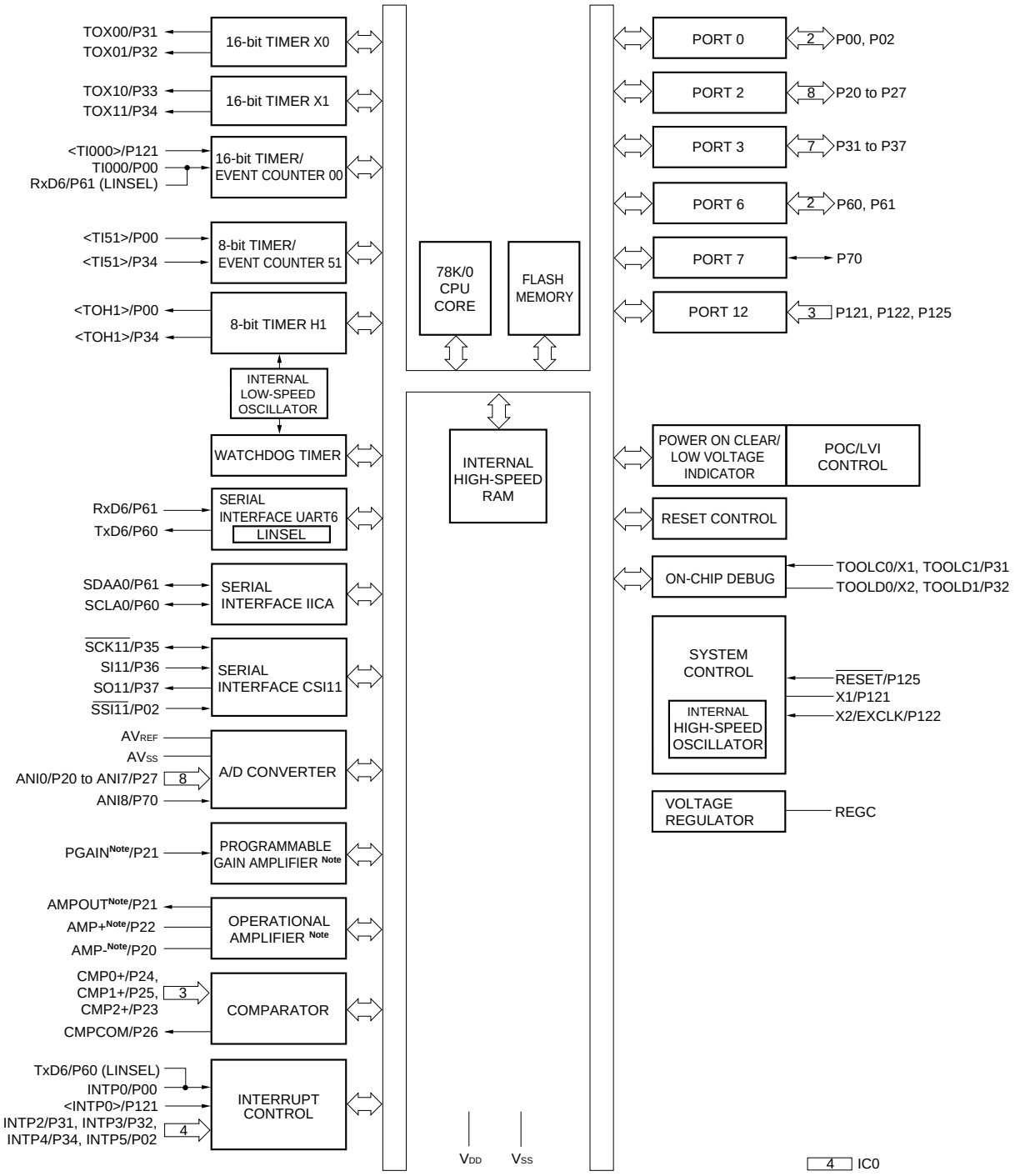
○ Clock
- High-speed system clock … Selected from the following four sources
  - Ceramic/crystal oscillator: 1 to 10 MHz[Note]
  - External clock: 1 to 10 MHz[Note]
  - Internal high-speed oscillator: 4 MHz ± 2 % (–20 to +70°C)[Note], or 8 MHz ± 3 %(–40 to +85°C)
  - Clock for 16-bit timers X0 and X1: 40 MHz (TYP.) (when using PLL)
- Internal low-speed oscillator 30 kHz ± 10 % … Watchdog timer, timer clock in intermittent operation

Note When using a 4 MHz clock, operation at 20 MHz is possible by using PLL.

○ Timer
- 16-bit timer X … PWM output (40 MHz (MAX.) clock operation), operation in conjunction with an external signal, synchronous output of up to four channels, A/D conversion trigger generation
- 16-bit timer/event counter … PPG output, capture input, external event counter input
- 8-bit timer H1 … PWM output, operable with low-speed internal oscillation clock
- 8-bit timer/event counter 51 … External event counter input
- Watchdog timer … Operable with low-speed internal oscillation clock

Item / Products	16-bit timer	16-bit timer/ event counter	8-bit timer	Watchdog timer
78K0/IY2 (16 pins)	2 ch	1 ch	Timer H1: 1 ch Timer 51: 1 ch	1 ch
78K0/IA2 (20 pins)				
78K0/IB2 (30 pins)				
78K0/IB2 (32 pins)				

- 32-pin



Note μPD78F0755, 78F0756 (products with operational amplifier) only

Cautions 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

2. ANI0/P20/AMP-, ANI1/P21/AMPOUT/PGAIN, ANI2/P22/AMP+, ANI3/P23/CMP2+, ANI4/P24/CMP0+, ANI5/P25/CMP1+, ANI6/P26/CMPCOM, ANI7/P27, and ANI8/P70 are set in the analog input mode after release of reset.

3. $\overline{\text{RESET}}$/P125 immediately after release of reset is set in the external reset input.

Remark Functions in angle brackets < > can be assigned by setting the input switch control register (MUXSEL).

(8) PWM output operation (PWM output from TOX00, TOX01, TOX10, and TOX11 when TOH1 output is at high level)

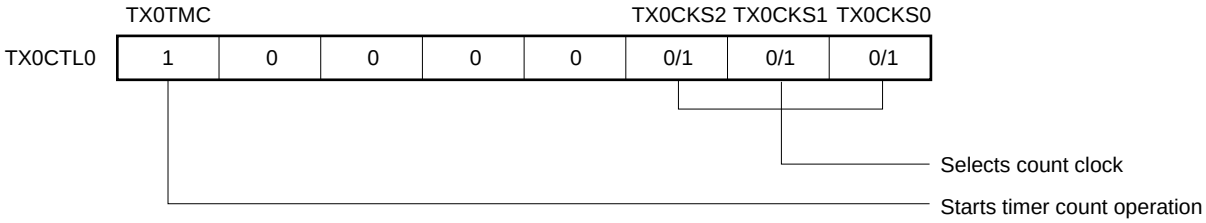
A square wave is output from the TOX00, TOX01, TOX10, and TOX11 pins by combining 8-bit timer H1 and 16-bit timers X0 and X1, only when the TOH1 output is at high level.

See **(1) PWM output operation (single output)** through **(4) PWM output operation (TMX0 and TMX1 synchronous start mode)** for the setting of outputting a square wave.

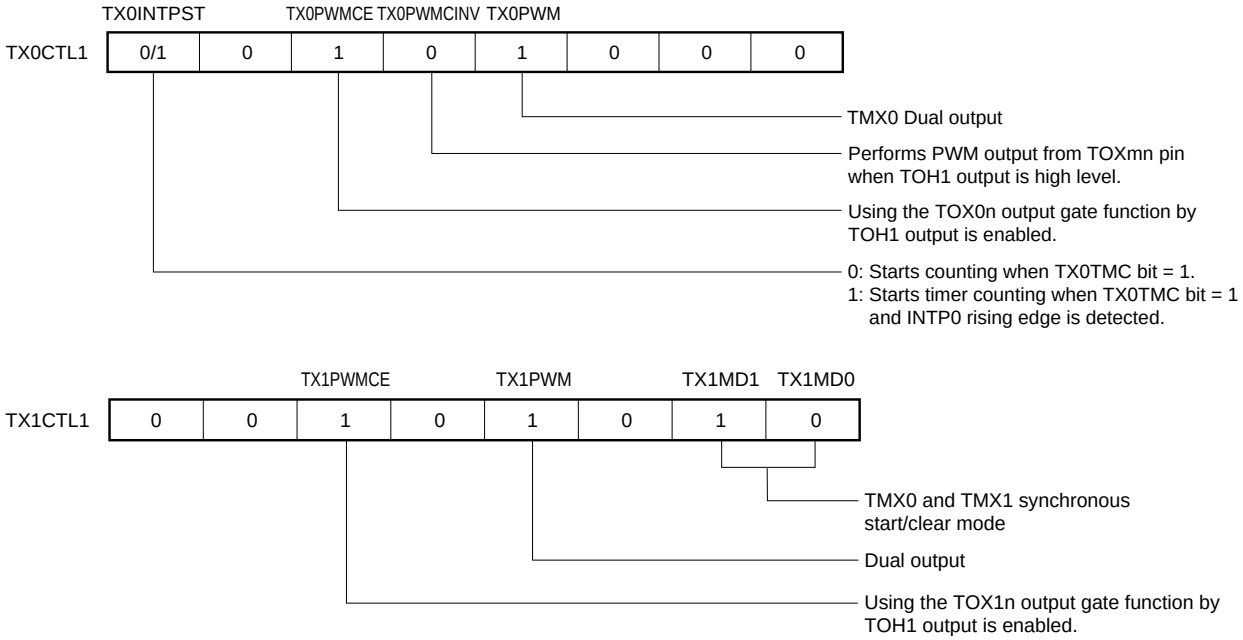
Remark For the setting of TOH1 output, see **CHAPTER 9 8-BIT TIMER H1.**

Figure 6-41. Example of Register Settings for PWM Output Operation (TMX0 and TMX1 synchronous start/clear mode, PWM Output from TOX00, TOX01, TOX10, and TOX11 When TOH1 Output Is at High Level) (1/2)

(a) 16-bit timer X0 operation control register 0



(b) 16-bit timer Xn operation control register 1



Remark n = 0, 1, mn = 00, 01, 10, 11

6.7.2 Registers Controlling High-Impedance Output Controller

Registers used to control the High-Impedance Output Controller are shown below.

- High-impedance output function enable register (HIZTREN)
- High-impedance output mode select register (HIZTRS)
- High-impedance output function control register 0 (HZA0CTL0)

(1) High-impedance output function enable register (HIZTREN)

HIZTREN is a register that enables/disables the input of the trigger signal used for controlling high-impedance output.

HIZTREN can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears HIZTREN to 00H.

Figure 6-56. Format of High-impedance Output Function Enable Register (HIZTREN)

Address: FF6EH After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
HIZTREN	HIZTREN0	0	0	0	0	0	0	0

HIZTREN0	Input control of trigger signal used for high-impedance output control
0	Disables input
1	Enables input

7.3 Registers Controlling 16-Bit Timer/Event Counter 00

Registers used to control 16-bit timer/event counter 00 are shown below.

- 16-bit timer mode control register 00 (TMC00)
- Capture/compare control register 00 (CRC00)
- 16-bit timer output control register 00 (TOC00)
- Prescaler mode register 00 (PRM00)
- Port alternate switch control register (MUXSEL)
- Port mode register 0 (PM0)
- Port register 0 (P0)

Note 78K0/IB2 (30 pins) only

(1) 16-bit timer mode control register 00 (TMC00)

TMC00 is an 8-bit register that sets the 16-bit timer/event counter 00 operation mode, TM00 clear mode, and output timing, and detects an overflow.

Rewriting TMC00 is prohibited during operation (when TMC003 and TMC002 = other than 00). However, it can be changed when TMC003 and TMC002 are cleared to 00 (stopping operation) and when OVF00 is cleared to 0.

TMC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TMC00 to 00H.

Caution 16-bit timer/event counter 00 starts operation at the moment TMC003 and TMC002 are set to values other than 00 (operation stop mode), respectively. Set TMC003 and TMC002 to 00 to stop the operation.

(8) 8-bit A/D conversion result register L (ADCRL)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the lower 8 bits of the A/D conversion result.

(9) 8-bit A/D conversion result register H (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

(10) 10-bit A/D conversion result register for TMXn synchronization (ADCRXn = 0, 1)

If A/D conversion is started with the output of 16-bit timer Xn as the trigger, the conversion result is loaded from the successive approximation register and the A/D conversion result is held in the lower 10 bits (the higher 6 bits are fixed to 0) every time an A/D conversion ends.

(11) 8-bit A/D conversion result register L for TMXn synchronization (ADCRXnL = 0, 1)

If A/D conversion is started with the output of 16-bit timer Xn as the trigger, the conversion result is loaded from the successive approximation register and the lower 8 bits of the A/D conversion result are held in ADCRXnL register, every time an A/D conversion ends.

Caution When data is read from ADCR, ADCRL, ADCRH, ADCRX0, ADCRX1, ADCRX0L, and ADCRX1L, a wait cycle is generated. Do not read data from ADCR, ADCRL, ADCRH, ADCRX0, ADCRX1, ADCRX0L, and ADCRX1L when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.

(12) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When all the specified A/D conversion has been completed, this controller generates an A/D conversion end interrupt request signal (INTAD).

(13) AV_{REF} pin

This pin inputs an analog power/reference voltage to the A/D converter. Make this pin the same potential as the V_{DD} pin when ports 2 and 7 are used as a digital port.

The signal input to ANI0 to ANI8 is converted into a digital signal, based on the voltage applied across AV_{REF} and AV_{SS}.

(14) AV_{SS} pin (78K0/IB2 only)

This is the ground potential pin of the A/D converter. Always use this pin at the same potential as that of the V_{SS} pin even when the A/D converter is not used.

(15) V_{SS} pin

This is the ground potential pin. In the 78K0/IY2 and 78K0/IA, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

11.4.2 Basic operation of A/D converter (timer trigger mode)

<1> Set the A/D conversion time and the operation mode by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of the A/D converter mode register 0 (ADM0).

<2> Set bit 0 (ADCE) of ADM0 to 1 to start the operation of the A/D voltage comparator.

<3> Set channels for A/D conversion to analog input by using the A/D port configuration registers 0 and 1 (ADPC0, ADPC1) and set to input mode by using port mode registers 2 and 7 (PM2, PM7).

<4> Set the PGA operation to set the PGA output and the single Amp operation to set the operational amplifier output for analog input. (refer to **CHAPTER 12 OPERATIONAL AMPLIFIER**).

<5> Select TMX0 or TMX1 synchronization by using bits 4 and 5 (ADTRG0, ADTRG1) of the analog input channel specification register (ADS).

<6> Select one channel for A/D conversion by using the analog input channel specification register (ADS).

<7> Set the timer trigger wait state by setting (1) bit 7 (ADCS) of ADM0.
(<8> to <16> are operations performed by hardware.)

<8> A conversion operation is started when a trigger signal (TMX0 or TMX1 output) is detected.

<9> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<10> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<11> Bit 9 of the successive approximation register (SAR) is set. The comparison voltage generator outputs (1/2) AV_{REF} voltage.

<12> The voltage difference between the output voltage of the comparison voltage generator and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB of SAR remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB is reset to 0.

<13> Next, bit 8 of SAR is automatically set to 1, and the operation proceeds to the next comparison. The output voltage of the comparison voltage generator is selected according to the preset value of bit 9, as described below.

- Bit 9 = 1: (3/4) AV_{REF}
- Bit 9 = 0: (1/4) AV_{REF}

The output voltage of the comparison voltage generator and sampled voltage are compared and bit 8 of SAR is manipulated as follows.

- Analog input voltage ≥ Output voltage of comparison voltage generator: Bit 8 = 1
- Analog input voltage < Output voltage of comparison voltage generator: Bit 8 = 0

<14> Comparison is continued in this way up to bit 0 of SAR.

<15> Upon completion of the comparison of 10 bits, an effective digital result value remains in SAR, and the result value is transferred to the A/D conversion result register (TMX0 synchronization: ADCRX0, ADCRX0L, TMX1 synchronization: ADCRX1, ADCRX1L) and then latched.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.

<16> Repeat steps <9> to <15>, until ADCS is cleared to 0.
To stop the A/D converter, clear ADCS to 0.
To restart A/D conversion from the status of ADCE = 1, start from <7>. To start A/D conversion again when ADCE = 0, set ADCE to 1, wait for 1 μs or longer, and start <7>. To change a channel of A/D conversion, start from <6>.

(11) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 11-27. Internal Equivalent Circuit of ANIn Pin

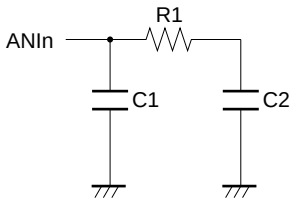


Table 11-9. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{REF}	Mode	R1	C1	C2
4.0 V ≤ AV_{REF} ≤ 5.5 V	Normal	5.2 kΩ	8 pF	6.3 pF
	High-speed 1	5.2 kΩ		
	High-speed 2	7.8 kΩ		
2.7 V ≤ AV_{REF} < 4.0 V	Normal	18.6 kΩ		
	High-speed 2	7.8 kΩ		

Remarks 1. The resistance and capacitance values shown in Table 11-9 are not guaranteed values.

2. n = 0 to 8 (it depends on products)

3. A/D conversion result registers differ depending on trigger mode.

- Software trigger mode: ADCR, ADCRH, ADCRL registers
- Timer trigger mode: ADCRX0, ADCRX0L registers (TMX0 synchronization)
  ADCRX1, ADCRX1L registers (TMX1 synchronization)

(6) Baud rate generator control register 6 (BRGC6)

This register sets the division value of the 8-bit counter of serial interface UART6/DALI.

BRGC6 can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Remark BRGC6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1).

Figure 14-10. Format of Baud Rate Generator Control Register 6 (BRGC6)

Address: FF57H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
BRGC6	MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60

MDL67	MDL66	MDL65	MDL64	MDL63	MDL62	MDL61	MDL60	k	Output clock selection of 8-bit counter	
									UART mode	DALI mode
0	0	0	0	0	0	×	×	×	Setting prohibited	Setting prohibited
0	0	0	0	0	1	0	0	4	$f_{XCLK6}/4$	
0	0	0	0	0	1	0	1	5	$f_{XCLK6}/5$	
0	0	0	0	0	1	1	0	6	$f_{XCLK6}/6$	
0	0	0	0	0	1	1	1	7	$f_{XCLK6}/7$	
0	0	0	0	1	0	0	0	8	$f_{XCLK6}/8$	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	1	1	1	1	1	0	0	252	$f_{XCLK6}/252$	
1	1	1	1	1	1	0	1	253	$f_{XCLK6}/253$	
1	1	1	1	1	1	1	0	254	$f_{XCLK6}/254$	
1	1	1	1	1	1	1	1	255	$f_{XCLK6}/255$	

Cautions 1. Make sure that bit 6 (TXE6) and bit 5 (RXE6) of the ASIM6 register = 0 when rewriting the MDL67 to MDL60 bits.

2. In UART mode the baud rate is the output clock of the 8-bit counter divided by 2.

3. In DALI mode the baud rate is the output clock of the 8-bit counter divided by 4.

Remarks 1. f_{XCLK6}: Frequency of base clock selected by the TPS63 to TPS60 bits of CKSR6 register

2. k: Value set by MDL67 to MDL60 bits (k = 4, 5, 6, ..., 255)

3. ×: Don't care

(10) Port output mode register 6 (POM6)

This register sets the output mode of P60 and P61 in 1-bit units.

When using the P60/TxD6/SCLA0 pin as the data output of serial interface UART6/DALI, clear POM60 to 0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 14-14. Format of Port Output Mode Register 6 (POM6)

Address: FF2AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
POM6	0	0	0	0	0	0	POM61	POM60

POM6n	P6n pin output mode selection (n = 0, 1)
0	Normal output (CMOS output) mode
1	N-ch open drain output (V_{DD} tolerance) mode

15.4.2 Setting transfer clock by using IICWL and IICWH registers

(1) Setting transfer clock on master side

$$\text{Transfer clock} = \frac{f_{PRS}}{IICWL + IICWH + f_{PRS}(t_R + t_F)}$$

At this time, the optimal setting values of the IICWL and IICWH registers are as follows.
(The fractional parts of all setting values are rounded up.)

- When the fast mode

$$IICWL = \frac{0.52}{\text{Transfer clock}} \times f_{PRS}$$
$$IICWH = \left(\frac{0.48}{\text{Transfer clock}} - t_R - t_F\right) \times f_{PRS}$$

- When the normal mode

$$IICWL = \frac{0.47}{\text{Transfer clock}} \times f_{PRS}$$
$$IICWH = \left(\frac{0.53}{\text{Transfer clock}} - t_R - t_F\right) \times f_{PRS}$$

(2) Setting IICWL and IICWH on slave side

(The fractional parts of all setting values are truncated.)

- When the fast mode

$$IICWL = 1.3\ \mu s \times f_{PRS}$$
$$IICWH = (1.2\ \mu s - t_R - t_F) \times f_{PRS}$$

- When the normal mode

$$IICWL = 4.7\ \mu s \times f_{PRS}$$
$$IICWH = (5.3\ \mu s - t_R - t_F) \times f_{PRS}$$

Caution Note the minimum f_{PRS} operation frequency when setting the transfer clock. The minimum f_{PRS} operation frequency for serial interface IICA is determined according to the mode.

Fast mode: f_{PRS} = 3.5 MHz (min.)

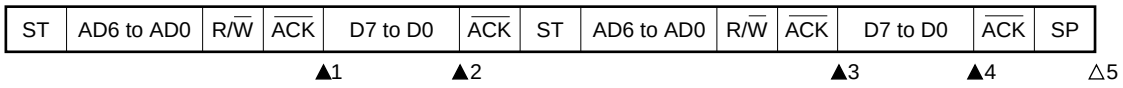
Normal mode: f_{PRS} = 1 MHz (min.)

Remarks 1. Calculate the rise time (t_R) and fall time (t_F) of the SDA0 and SCLA0 signals separately, because they differ depending on the pull-up resistance and wire load.

2. IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDAA0 and SCLA0 signal falling times (refer to **CHAPTER 28 ELECTRICAL SPECIFICATIONS**)
t_R: SDAA0 and SCLA0 signal rising times (refer to **CHAPTER 28 ELECTRICAL SPECIFICATIONS**)
f_{PRS}: Peripheral hardware clock frequency

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

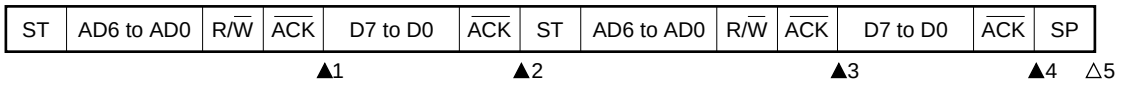
(i) When WTIM0 = 0 (after restart, matches with SVA0)



▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001×000B
▲3: IICAS0 = 0001×110B
▲4: IICAS0 = 0001×000B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, matches with SVA0)



▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001××00B
▲3: IICAS0 = 0001×110B
▲4: IICAS0 = 0001××00B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 16-2. Format of Serial Operation Mode Register 11 (CSIM11)

Address: FF88H After reset: 00H R/W[Note 1]

Symbol	<7>	6	5	4	3	2	1	0
CSIM11	CSIE11	TRMD11	SSE11	DIR11	0	0	0	CSOT11

CSIE11	Operation control in 3-wire serial I/O mode
0	Disables operation[Note 2] and asynchronously resets the internal circuit[Note 3].
1	Enables operation

TRMD11[Note 4]	Transmit/receive mode control
0[Note 5]	Receive mode (transmission disabled).
1	Transmit/receive mode

SSE11[Notes 6, 7]	$\overline{\text{SSI11}}$ pin use selection
0	$\overline{\text{SSI11}}$ pin is not used
1	$\overline{\text{SSI11}}$ pin is used

DIR11[Note 8]	First bit specification
0	MSB
1	LSB

CSOT11	Communication status flag
0	Communication is stopped.
1	Communication is in progress.

Notes 1. Bit 0 is a read-only bit.

2. To use P37/SO11, P35/$\overline{\text{SCK11}}$, and P20/$\overline{\text{SSI11}}$/INTP5 as general-purpose ports, set CSIM11 in the default status (00H).

3. Bit 0 (CSOT11) of CSIM11 and serial I/O shift register 11 (SIO11) are reset.

4. Do not rewrite TRMD11 when CSOT11 = 1 (during serial communication).

5. The SO11 output (refer to **Figure 16-1**) is fixed to the low level when TRMD11 is 0. Reception is started when data is read from SIO11.

6. Do not rewrite SSE11 when CSOT11 = 1 (during serial communication).

7. Before setting this bit to 1, fix the $\overline{\text{SSI11}}$ pin input level to 0 or 1.

8. Do not rewrite DIR11 when CSOT11 = 1 (during serial communication).

(2) Serial clock selection register 11 (CSIC11)

This register specifies the timing of the data transmission/reception and sets the serial clock.

CSIC11 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

(2) Multiplication input data registers A, B (MULA, MULB)

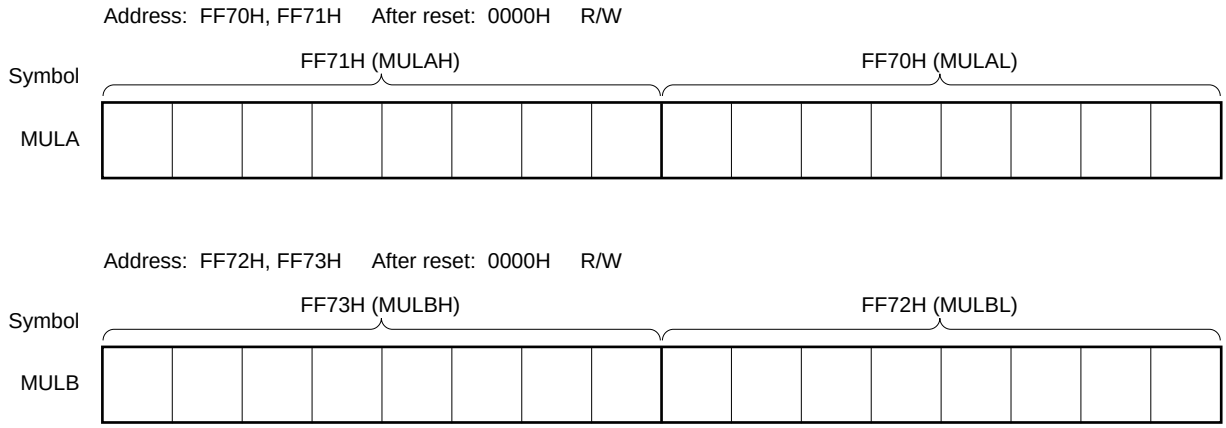
These are 16-bit registers that store data for multiplication. The multiplier multiplies the values of MULA and MULB.

MULA and MULB can be set by an 8-bit or 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 0000H.

Caution In the case of multiplication of 8 bits by 8 bits, set the multiplied data to MULAL and MULBL.

Figure 17-3. Format of Multiplication input data registers A, B (MULA, MULB)



(1) Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

IF0L, IF0H, IF1L, and IF1H are set by a 1-bit or 8-bit memory manipulation instruction. When IF0L and IF0H, and IF1L and IF1H are combined to form 16-bit registers IF0 and IF1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Cautions 1. When operating a timer, serial interface, or A/D converter after standby release, operate it once after clearing the interrupt request flag. An interrupt request flag may be set by noise.

2. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as "IF0L.0 = 0;" or "_asm("clr1 IF0L, 0");" because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).

If a program is described in C language using an 8-bit memory manipulation instruction such as "IF0L &= 0xfe;" and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between "mov a, IF0L" and "mov IF0L, a", the flag is cleared to 0 at "mov IF0L, a". Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

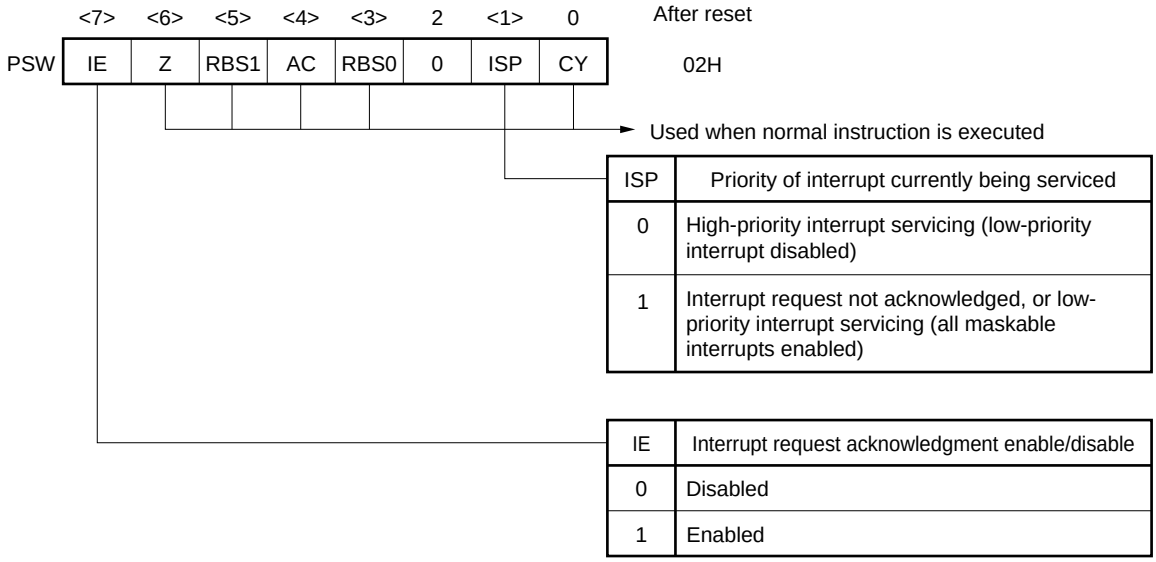
(6) Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP flag that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. If a maskable interrupt request is acknowledged, the contents of the priority specification flag of the acknowledged interrupt are transferred to the ISP flag. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets PSW to 02H.

Figure 18-13. Format of Program Status Word



ISP	Priority of interrupt currently being serviced
0	High-priority interrupt servicing (low-priority interrupt disabled)
1	Interrupt request not acknowledged, or low-priority interrupt servicing (all maskable interrupts enabled)

IE	Interrupt request acknowledgment enable/disable
0	Disabled
1	Enabled

Figure 22-2. Format of Low-Voltage Detection Register (LVIM)

Address: FFBEH After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	2	<1>	<0>
LVIM	LVION	0	0	0	0	0	LVIMD	LVIF

LVION[Notes 3, 4]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

LVIMD[Note 3]	Low-voltage detection operation mode (interrupt/reset) selection
0	Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the LVI detection voltage (V_{LVI}) ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$).
1	Generates an internal reset signal when the supply voltage (V_{DD}) < the LVI detection voltage (V_{LVI}) and releases the reset signal when $V_{DD} \geq V_{LVI}$.

LVIF	Low-voltage detection flag
0	Supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI}), or when LVI operation is disabled
1	Supply voltage (V_{DD}) < LVI detection voltage (V_{LVI})

Notes 1. The reset value changes depending on the reset source and the setting of the option byte. This register is not cleared (00H) by LVI reset (except reset by LVI default start function). The value of this register is reset to “00H” by other resets.

2. Bit 0 is read-only.

3. LVION and LVIMD are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

4. When LVION is set to 1, operation of the comparator in the LVI circuit is started. Use software to wait for an operation stabilization time (10 μs (MAX.)) from when LVION is set to 1 until operation is stabilized. After the operation stabilizes, an external input (minimum pulse width: 200 μs) of 200 μs or more is required until LVIF is set (1) after the voltage drops to the LVI detection voltage or less.

Cautions 1. To stop LVI, follow either of the procedures below.

- **When using 8-bit memory manipulation instruction: Write 00H to LVIM.**
- **When using 1-bit memory manipulation instruction: Clear LVION to 0.**

2. If LVI operation is disabled (clears LVION) when LVI is used in interrupt mode (LVIMD = 0) and the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

22.4.1 When used as reset

(1) When LVI default start function stopped is set (LVISTART = 0)

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Set the LVI detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).
  - <3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <4> Use software to wait for an operation stabilization time (10 μs (MAX.)).
  - <5> Wait until it is checked that (supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI})) by bit 0 (LVIF) of LVIM.
  - <6> Set bit 1 (LVIMD) of LVIM to 1 (generates reset when the level is detected).

  Figure 22-4 shows the timing of the internal reset signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <6> above.

  Cautions 1. Be sure to execute <1>. When LVIMK = 0, an interrupt may occur immediately after the processing in <3>.
  2. If supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI}) when LVIMD is set to 1, an internal reset signal is not generated.

- When stopping operation
  Either of the following procedures must be executed.

  - When using 8-bit memory manipulation instruction:
    Write 00H to LVIM.

  - When using 1-bit memory manipulation instruction:
    Clear LVIMD to 0 and then LVION to 0.