Renesas Electronics America Inc - UPD78F0743MC-CAA-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	DALI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0743mc-caa-ax

○ Serial interface
- UART6 … Asynchronous 2-wire serial interface
- DALI … 2-wire serial interface for lighting control (slave)
- IICA … Clock synchronous 2-wire serial interface, multimaster supported
  standby can be released upon address match in slave mode
- CSI11 … Clock synchronous 3-wire serial interface, operable as SPI in slave mode

Item / Products	UART6/DALI	IICA	CSI11
78K0/IY2 (16 pins)	–	–	–
78K0/IA2 (20 pins)	1 ch	1 ch	
78K0/IB2 (30 pins)			1 ch
78K0/IB2 (32 pins)			

○ Multiplier (8 bits × 8 bits = 16 bits, 16 bits × 16 bits = 32 bits, 1-clock operation)
○ 10-bit resolution A/D conversion
- 78K0/IY2: 5 ch
- 78K0/IA2: 6 ch
- 78K0/IB2: 9 ch

○ Operational amplifier (Products with operational amplifier only): 1 ch
○ Comparator: 3 ch
○ Power-on-clear (POC) circuit
○ Low-voltage detector (LVI) circuit (An interrupt/reset (selectable) is generated when the detection voltage is reached))
- Detection voltage: Selectable from ten levels between 2.84 and 4.22 V
  *1.91 V is used only when the power is turned on when the LVI default start is set.

○ Single-power-supply flash memory
- Flash self programming enabled
- Software protection function: Protected from outside party copying (no flash reading command)

○ Safety function
- Watchdog timer operated by clock independent from CPU
  … A hang-up can be detected even if the system clock stops
- Supply voltage drop detectable by LVI
  … Appropriate processing can be executed before the supply voltage drops below the operation voltage
- Equipped with option byte function
  … Important system operation settings set in hardware

○ On-chip debug function …Available to control for the target device, and to reference memory
○ Assembler and C language supported
○ Enhanced development environment
- Support for full-function emulator (IECUBE), and simplified emulator (QB-MINI2)

○ Power supply voltage: V_{DD} = 2.7 to 5.5 V
○ Operating ambient temperature: T_A = –40 to +105°C

Table 4-9. Setting Functions of P23/ANI3/CMP2+, P24/ANI4/CMP0+, P25/ANI5/CMP1+ Pins

ADPC0 Register	PM2 Register	CMPmEN bit (m = 0 to 2)	ADS Register (n = 3 to 5)	P23/ANI3/CMP2+, P24/ANI4/CMP0+, P25/ANI5/CMP1+ Pins
Digital I/O selection	Input mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital input
	Output mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital output
Analog input selection	Input mode	0	Selects ANIn.	Analog input (to be converted into digital signal)
			Does not select ANIn.	Analog input (not to be converted into digital signal)
		1	Selects ANIn.	Analog input (to be converted into digital signal), and comparator input
			Does not select ANIn.	Comparator input
	Output mode	–	–	Setting prohibited

Remark ADPC0: A/D port configuration register 0
PM2: Port mode register 2
CMPmEN: Bit 7 of comparator m control register (CmCTL)
ADS: Analog input channel specification register

Table 4-10. Setting Functions of P26/ANI6/CMPCOM Pin

ADPC0 Register	PM2 Register	CmMODSEL1 bit (m = 0 to 2)	CmMODSEL0 bit (m = 0 to 2)	ADS Register	P26/ANI6/CMPCOM Pin
Digital I/O selection	Input mode	–		Selects ANI6.	Setting prohibited
				Does not select ANI6.	Digital input
	Output mode	–		Selects ANI6.	Setting prohibited
				Does not select ANI6.	Digital output
Analog input selection	Input mode	CmMODSEL1 = 0, or CmMODSEL0 = 0		Selects ANI6.	Analog input (to be converted into digital signal)
				Does not select ANI6.	Analog input (not to be converted into digital signal)
		CmMODSEL1 = 1, and CmMODSEL0 = 1		Selects ANI6.	Analog input (to be converted into digital signal), and comparator common input
				Does not select ANI6.	Comparator common input
	Output mode	–		–	Setting prohibited

Remark ADPC0: A/D port configuration register 0
PM2: Port mode register 2
CmMODSEL1, CmMODSEL0: Bits 4, 3 of comparator m control register (CmCTL)
ADS: Analog input channel specification register

5.4 System Clock Oscillator

5.4.1 X1 oscillator

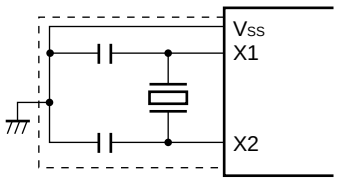
The X1 oscillator oscillates with a crystal resonator or ceramic resonator (clock-through mode: 1 to 10 MHz, PLL mode: 4 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal (clock-through mode: 1 to 10 MHz, PLL mode: 4 MHz) to the EXCLK pin.

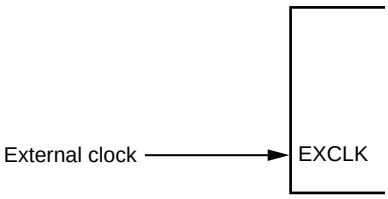
Figure 5-9 shows an example of the external circuit of the X1 oscillator.

Figure 5-9. Example of External Circuit of X1 Oscillator

(a) Crystal or ceramic oscillation



(b) External clock



Cautions are listed on the next page.

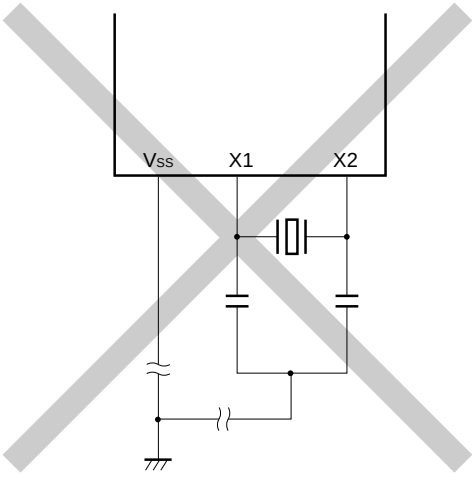
Caution. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the Figure 5-9 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

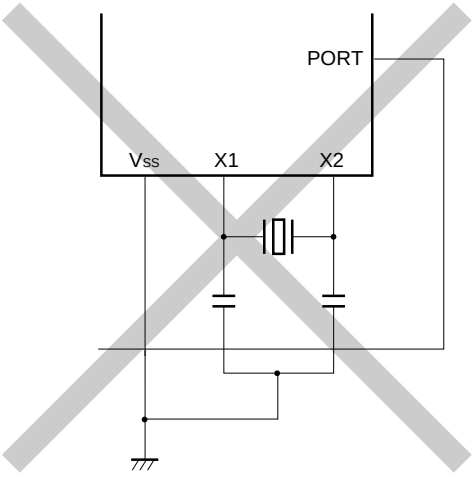
Figure 5-10 shows examples of incorrect resonator connection.

Figure 5-10. Examples of Incorrect Resonator Connection (1/2)

(a) Too long wiring



(b) Crossed signal line



CHAPTER 6 16-BIT TIMERS X0 AND X1

6.1 Functions of 16-Bit Timers X0 and X1

16-bit timers X0 and X1 are mounted onto all 78K0/Ix2 microcontroller products.

16-bit timers X0 and X1 are dedicated PWM output timers and have two outputs each, enabling the generation of up to four PWM outputs. Complementary PWM output can also be generated to control a half-bridge circuit (2 outputs) or full-bridge circuit (4 outputs). Also, by linking with a comparator or INTP0, PFC control and PWM output can be stopped urgently.

16-bit timers X0 and X1 are provided with the following functions.

(1) PWM output

- A variable pulse with any duty or cycle can be output while the timer is operating.
- The default timer output level (high or low level) can be set.

(2) A/D conversion start timing signal output

The A/D conversion start timing signal can be output by using a compare register (TXnCCR0 register: n = 0, 1).

(3) Capture function

This function captures the count value to the capture register by detecting a comparator output or an external interrupt input (INTP0).

(4) Timer start synchronization function

Up to 4 PWM outputs can be simultaneously started by combining two timer units (16-bit timers X0 and X1).

(5) Timer start/clear synchronization function

Up to 4 PWM output cycles can be synchronized by combining two timer units (16-bit timers X0 and X1).

(6) Timer output gating function (by interlocking with 8-bit timer H1)

Timer output can be gate-controlled by using the output of 8-bit timer H1 (the TOH1 output).

(7) Timer reset mode (comparator, INTP0 interlocking mode 1)

Timer output can be reset and the timer counter cleared while the comparator 0 to 2 outputs or the INTP0 input is high level. When the comparator 0 to 2 outputs or the INTP0 input go to low level, timer output restarts.

(8) Timer restart mode (comparator, INTP0 interlocking mode 2)

Timer can be restarted upon detection of the rising edge of the comparator 0 to 2 outputs or the INTP0 input.

(9) Timer output reset mode (comparator, INTP0 interlocking mode 3)

Timer output can be reset upon detection of the rising edge of the comparator 0 to 2 outputs or the INTP0 input. The reset status is cleared when the next timer interrupt occurs and timer output restarts.

(10) High-impedance output control function (by interlocking with comparator and INTP0)

Timer output can be made high impedance upon detection of the valid edge of the comparator 0 to 2 outputs or the INTP0 input.

Figure 6-11. Format of 16-Bit Timer X1 Operation Control Register 2 (TX1CTL2)

Address: FF96H After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	<0>
TX1CTL2	0	0	0	0	0	0	TX1ADEN	TX1CCS

TX1ADEN	Control of generating A/D conversion synchronization trigger from TMX1
0	Disables generating A/D conversion synchronization trigger
1	Enables generating A/D conversion synchronization trigger[Note]

TX1CCS	TX1CCR0 register operation
0	Operates as compare register[Note]
1	Operates as capture register

Note When enabling generation of the A/D conversion synchronization trigger (TX1ADEN = 1), set the TX1CCR0 register to operate as a compare register (TX1CCS = 0), because the A/D conversion synchronization trigger is generated upon a match between the counter and the TX1CCR0 register.

Cautions 1. During the 16-bit timer operation, setting the other bits of TX1CTL2 is prohibited. However, TX1CTL2 can be refreshed (the same value is written).

2. The registers used by the A/D converter (ADM0, ADPC0, ADPC1, ADS) can be rewritten while the 16-bit timer X1 is operating.

3. A/D conversion synchronization triggers that occur while A/D conversion is stopped (ADCS = 0) are invalid. A/D conversion synchronization triggers that occur after A/D conversion has been enabled (ADCS = 1) are valid.

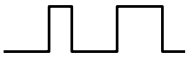
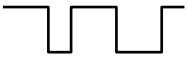
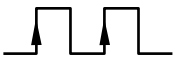
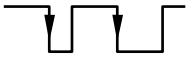
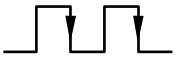
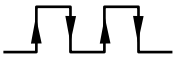
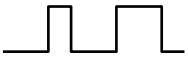
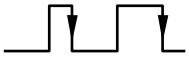
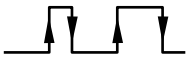
(4) 16-bit timer X0 operation control register 3 (TX0CTL3)

TX0CTL3 is a register that sets the mode of the interlocking function with comparator 2 and INTP0, and sets the operation when restarting upon comparator output.

TX0CTL3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TX0CTL3 to 00H.

Table 7-2. Capture Operation of CR000 and CR010

External Input Signal / Capture Operation	TI000 Pin Input 		TI010 Pin Input[Note 1] 	
Capture operation of CR000	CRC001 = 1 TI000 pin input (reverse phase) 	Set values of ES001 and ES000 Position of edge to be captured	CRC001 bit = 0 TI010 pin input 	Set values of ES101 and ES100 Position of edge to be captured
		01: Rising 		01: Rising 
		00: Falling 		00: Falling 
		11: Both edges (cannot be captured)		11: Both edges 
	Interrupt signal	INTTM000 signal is not generated even if value is captured.	Interrupt signal	INTTM000 signal is generated each time value is captured.
Capture operation of CR010	TI000 pin input[Note 2] 	Set values of ES001 and ES000 Position of edge to be captured		
		01: Rising 		
		00: Falling 		
		11: Both edges 		
	Interrupt signal	INTTM010 signal is generated each time value is captured.		

Notes 1. 78K0/IB2 (30 pins) only

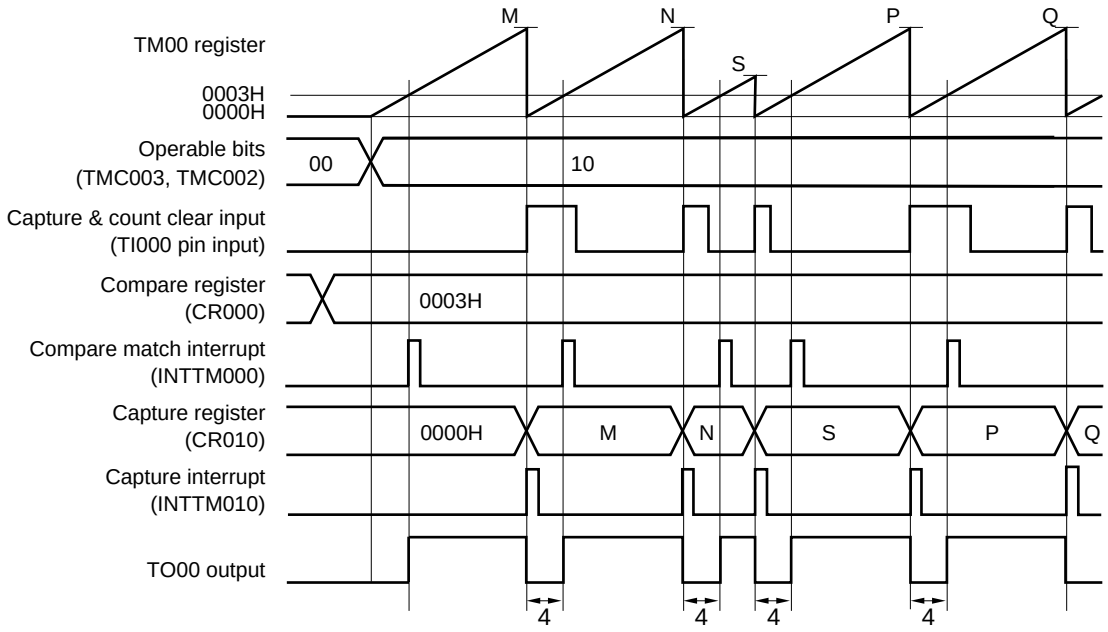
2. The capture operation of CR010 is not affected by the setting of the CRC001 bit.

Caution To capture the count value of the TM00 register to the CR000 register by using the phase reverse to that input to the TI000 pin, the interrupt request signal (INTTM000) is not generated after the value has been captured. If the valid edge is detected on the TI010 pin during this operation, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal. To not use the external interrupt, mask the INTTM000 signal.

Remark CRC001: Refer to **7.3 (2) Capture/compare control register 00 (CRC00)**.
ES101, ES100, ES001, ES000: Refer to **7.3 (4) Prescaler mode register 00 (PRM00)**.

Figure 7-26. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (2/2)

(b) TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 0AH, CR000 = 0003H



This is an application example where the width set to CR000 (4 clocks in this example) is to be output from the TO00 pin when the count value has been captured & cleared.

The count value is captured to CR010, a capture interrupt signal (INTTM010) is generated, TM00 is cleared (to 0000H), and the TO00 output level is inverted when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0003H (four clocks have been counted), a compare match interrupt signal (INTTM000) is generated and the TO00 output level is inverted.

7.6 Cautions for 16-Bit Timer/Event Counter 00

(1) Restrictions for each channel of 16-bit timer/event counter 00

Table 7-3 shows the restrictions for each channel.

Table 7-3. Restrictions for Each Channel of 16-Bit Timer/Event Counter 00

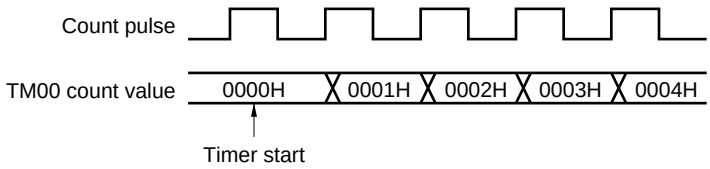
Operation	Restriction
As interval timer	–
As square-wave output[Note]	
As external event counter	
As clear & start mode entered by TI000 pin valid edge input	Using timer output (TO00) is prohibited when detection of the valid edge of the TI010 pin is used. (TOC00 = 00H)
As free-running timer	–
As PPG output[Note]	0000H ≤ CP010 < CR000 ≤ FFFFH
As one-shot pulse outputa[Note]	Setting the same value to CR000 and CP010 is prohibited.
As pulse width measurement	Using timer output (TO00) is prohibited (TOC00 = 00H)

Note 78K0/IB2 (30 pins) only

(2) Timer start errors

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because counting TM00 is started asynchronously to the count pulse.

Figure 7-56. Start Timing of TM00 Count



(3) Setting of CR000 and CR010 (clear & start mode entered upon a match between TM00 and CR000)

Set a value other than 0000H to CR000 and CR010 (TM00 cannot count one pulse when it is used as an external event counter).

(9) Capture operation

(a) When valid edge of TI000 is specified as count clock

When the valid edge of TI000 is specified as the count clock, the capture register for which TI000 is specified as a trigger does not operate correctly.

(b) Pulse width to accurately capture value by signals input to TI010 and TI000 pins

To accurately capture the count value, the pulse input to the TI000 and TI010 pins as a capture trigger must be wider than two count clocks selected by PRM00 (refer to **Figure 7-7**).

(c) Generation of interrupt signal

The capture operation is performed at the falling edge of the count clock but the interrupt signals (INTTM000 and INTTM010) are generated at the rising edge of the next count clock (refer to **Figure 7-7**).

(d) Note when CRC001 (bit 1 of capture/compare control register 00 (CRC00)) is set to 1

When the count value of the TM00 register is captured to the CR000 register in the phase reverse to the signal input to the TI000 pin, the interrupt signal (INTTM000) is not generated after the count value is captured. If the valid edge is detected on the TI010 pin during this operation, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal. Mask the INTTM000 signal when the external interrupt is not used.

(10) Edge detection

(a) Specifying valid edge after reset

If the operation of the 16-bit timer/event counter 00 is enabled after reset and while the TI000 or TI010 pin is at high level and when the rising edge or both the edges are specified as the valid edge of the TI000 or TI010 pin, then the high level of the TI000 or TI010 pin is detected as the rising edge. Note this when the TI000 or TI010 pin is pulled up. However, the rising edge is not detected when the operation is once stopped and then enabled again.

(b) Sampling clock for eliminating noise

The sampling clock for eliminating noise differs depending on whether the valid edge of TI000 is used as the count clock or capture trigger. In the former case, the sampling clock is fixed to f_{PRS}. In the latter, the count clock selected by PRM00 is used for sampling.

When the signal input to the TI000 pin is sampled and the valid level is detected two times in a row, the valid edge is detected. Therefore, noise having a short pulse width can be eliminated (refer to **Figure 7-7**).

(11) Timer operation

The signal input to the TI000/TI010 pin is not acknowledged while the timer is stopped, regardless of the operation mode of the CPU.

Remark f_{PRS}: Peripheral hardware clock frequency

CHAPTER 8 8-BIT TIMER/EVENT COUNTER 51

8.1 Functions of 8-Bit Timer/Event Counter 51

8-bit timer/event counter 51 is mounted onto all 78K0/Ix2 microcontroller products.
8-bit timer/event counter 51 has the following functions.

- Interval timer
- External event counter

8.2 Configuration of 8-Bit Timer/Event Counter 51

8-bit timer/event counter 51 includes the following hardware.

Table 8-1. Configuration of 8-Bit Timer/Event Counter 51

Item	Configuration
Timer register	8-bit timer counter 51 (TM51)
Timer input	TI51
Register	8-bit timer compare register 51 (CR51)
Control registers	Timer clock selection register 51 (TCL51) 8-bit timer mode control register 51 (TMC51) Port alternate switch control register (MUXSEL) Port mode register 0 (PM0) or port mode register 3 (PM3)Note Port register 0 (P0) or port register 3 (P3)Note

Note 78K0/IY2, 78K0/IB2 (30 pins): PM3
78K0/IA2, 78K0/IB2 (32 pins): PM0 or PM3

Figure 8-1 shows the block diagram of 8-bit timer/event counter 51.

(1) 8-bit timer H compare register 01 (CMP01)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in all of the timer operation modes.

This register constantly compares the value set to CMP01 with the count value of the 8-bit timer counter H1 and, when the two values match, generates an interrupt request signal (INTTMH1) and inverts the output level of TOH1.

Rewrite the value of CMP01 while the timer is stopped (TMHE1 = 0).

A reset signal generation clears this register to 00H.

Figure 9-2. Format of 8-Bit Timer H Compare Register 01 (CMP01)

Address: FF1AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP01								

Caution CMP01 cannot be rewritten during timer count operation. CMP01 can be refreshed (the same value is written) during timer count operation.

(2) 8-bit timer H compare register 11 (CMP11)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in the PWM output mode and carrier generator mode.

In the PWM output mode, this register constantly compares the value set to CMP11 with the count value of the 8-bit timer counter H1 and, when the two values match, inverts the output level of TOH1. No interrupt request signal is generated.

In the carrier generator mode, the CMP11 register always compares the value set to CMP11 with the count value of the 8-bit timer counter H1 and, when the two values match, generates an interrupt request signal (INTTMH1). At the same time, the count value is cleared.

CMP11 can be refreshed (the same value is written) and rewritten during timer count operation.

If the value of CMP11 is rewritten while the timer is operating, the new value is latched and transferred to CMP11 when the count value of the timer matches the old value of CMP11, and then the value of CMP11 is changed to the new value. If matching of the count value and the CMP11 value and writing a value to CMP11 conflict, the value of CMP11 is not changed.

A reset signal generation clears this register to 00H.

Figure 9-3. Format of 8-Bit Timer H Compare Register 11 (CMP11)

Address: FF1BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP11								

Caution In the PWM output mode and carrier generator mode, be sure to set CMP11 when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

<5> By performing procedures <3> and <4> repeatedly, a pulse with an arbitrary duty can be obtained.

<6> To stop the count operation, set TMHE1 = 0.

If the setting value of the CMP01 register is N, the setting value of the CMP11 register is M, and the count clock frequency is f_{CNT}, the PWM pulse output cycle and duty are as follows.

- PWM pulse output cycle = (N + 1)/f_{CNT}
- Duty = (M + 1)/(N + 1)

Cautions 1. The set value of the CMP11 register can be changed while the timer counter is operating. However, this takes a duration of three operating clocks (signal selected by the CKS12 to CKS10 bits of the TMHMD1 register) from when the value of the CMP11 register is changed until the value is transferred to the register.

2. Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

3. Make sure that the CMP11 register setting value (M) and CMP01 register setting value (N) are within the following range.
00H ≤ CMP11 (M) < CMP01 (N) ≤ FFH

Remarks 1. For the setting of the output pin, refer to **9.3 (4) Port mode registers 0 and 3 (PM0, PM3)**.

2. For details on how to enable the INTTMH1 signal interrupt, refer to **CHAPTER 18 INTERRUPT FUNCTIONS**.

Table 12-3. Setting Functions of P21/ANI1/AMPOUT/PGAIN Pin

ADPC0 Register	PM2 Register	OPAMP0E bit Note	PGAEN bit	ADS Register	P21/ANI1/AMPOUT/PGAIN Pin
Digital I/O selection	Input mode	0	–	Selects ANI1.	Setting prohibited
				Does not select ANI1.	Digital input
		1	–	–	Setting prohibited
	Output mode	0	–	Selects ANI1.	Setting prohibited
				Does not select ANI1.	Digital output
		1	–	–	Setting prohibited
Analog selection	Input mode	0	0	Selects ANI1.	Analog input (to be converted into digital signal)
				Does not select ANI1.	Analog input (not to be converted into digital signal)
		0	1	Selects PGA output.	PGA input (to be converted into digital signal)
				Does not select PGA output.	PGA input (not to be converted into digital signal)
		1	0	Selects ANI1.	Operational amplifier output (to be converted into digital signal)
				Does not select ANI1.	Operational amplifier output (not to be converted into digital signal)
		1	1	Selects PGA output.	Operational amplifier output, and PGA input (to be converted into digital signal)
				Selects ANI1.	Operational amplifier output (to be converted into digital signal)
				Does not select PGA output and ANI1.	Operational amplifier output (not to be converted into digital signal)
	Output mode	–		–	Setting prohibited

Note 78K0/IA2, 78K0/IB2 only

Remark ADPC0: A/D port configuration register 0
PM2: Port mode register 2
OPAMP0E: Bit 7 of operational amplifier 0 control register (AMP0M)
PGAEN: Bit 6 of AMP0M
ADS: Analog input channel specification register

Figure 13-7. Format of DA2 Internal Reference Voltage Selection Register (C2RVM)

Address: FF67H After reset: 00H R/W

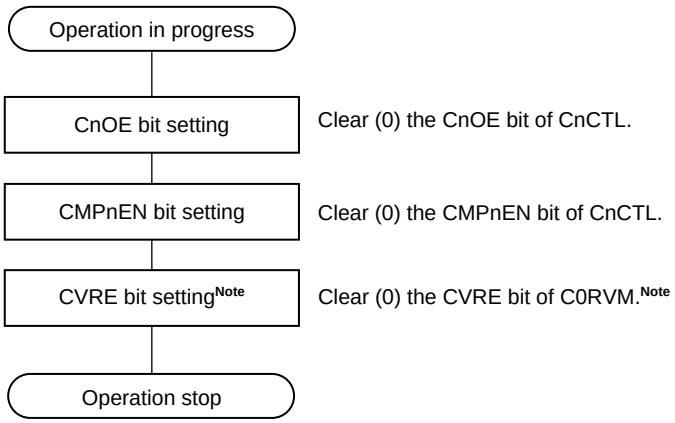
Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
C2RVM	0	0	0	C2VRS4	C2VRS3	C2VRS2	C2VRS1	C2VRS0

C2VRS4	C2VRS3	C2VRS2	C2VRS1	C2VRS0	Reference voltage level (DA2) setting
0	0	0	0	0	0.05 V (TYP.)
0	0	0	0	1	0.1 V (TYP.)
0	0	0	1	0	0.15 V (TYP.)
0	0	0	1	1	0.2 V (TYP.)
0	0	1	0	0	0.25 V (TYP.)
0	0	1	0	1	0.3 V (TYP.)
0	0	1	1	0	0.35 V (TYP.)
0	0	1	1	1	0.4 V (TYP.)
0	1	0	0	0	0.44 V (TYP.)
0	1	0	0	1	0.49 V (TYP.)
0	1	0	1	0	0.54 V (TYP.)
0	1	0	1	1	0.59 V (TYP.)
0	1	1	0	0	0.64 V (TYP.)
0	1	1	0	1	0.69 V (TYP.)
0	1	1	1	0	0.74 V (TYP.)
0	1	1	1	1	0.79 V (TYP.)
1	0	0	0	0	0.84 V (TYP.)
1	0	0	0	1	0.89 V (TYP.)
1	0	0	1	0	0.94 V (TYP.)
1	0	0	1	1	0.99 V (TYP.)
1	0	1	0	0	1.04 V (TYP.)
1	0	1	0	1	1.09 V (TYP.)
1	0	1	1	0	1.14 V (TYP.)
1	0	1	1	1	1.19 V (TYP.)
1	1	0	0	0	1.23 V (TYP.)
1	1	0	0	1	1.28 V (TYP.)
1	1	0	1	0	1.33 V (TYP.)
1	1	0	1	1	1.38 V (TYP.)
1	1	1	0	0	1.43 V (TYP.)
1	1	1	0	1	1.48 V (TYP.)
1	1	1	1	0	1.53 V (TYP.)
1	1	1	1	1	1.58 V (TYP.)

Caution To change the reference voltage level when the internal reference voltage generation operation is enabled (CVRE = 1), a voltage stabilization wait time is required. See Figure 13-12 Example of Procedure for Changing Internal Reference Voltage for the setting method.

13.4.3 Stopping comparator operation

Figure 13-14. Example of Setting Procedure when Stopping Comparator Operation



Note Only when using the internal reference voltage.

(4) DALI communication (slave transmission/reception) operation procedure

An example of DALI slave processing is shown below.

<1> Perform initial settings such as of the port I/Os and baud rate (1,200 bps).

<2> Wait for a command to be transmitted from the master.

<3> After receiving the command from the master, acquire and analyze the command data stored in the DALI receive buffer register (RXBDL).

<4> After analyzing the command, perform the following processing.

- **Successive receive commands**
  - **→ After receiving a command again, perform command processing and return to step <2>.**
- **Command without a response in a single reception**
  - **→ Perform command processing and return to step <2>.**
- **Command requiring a response in a single reception**
  - **→ Perform command processing, and if a response is required, return to step <2> after transmitting data.**
- **Command other than the above**
  - **→ Perform processing as an undefined command and return to step <2>.**

The flow of the above operation procedure and the transmission/reception timing chart are shown below.

15.5.12 Arbitration

When several master devices simultaneously generate a start condition (when the STT0 bit is set to 1 before the STD0 bit is set to 1), communication among the master devices is performed as the number of clocks are adjusted until the data differs. This kind of operation is called arbitration.

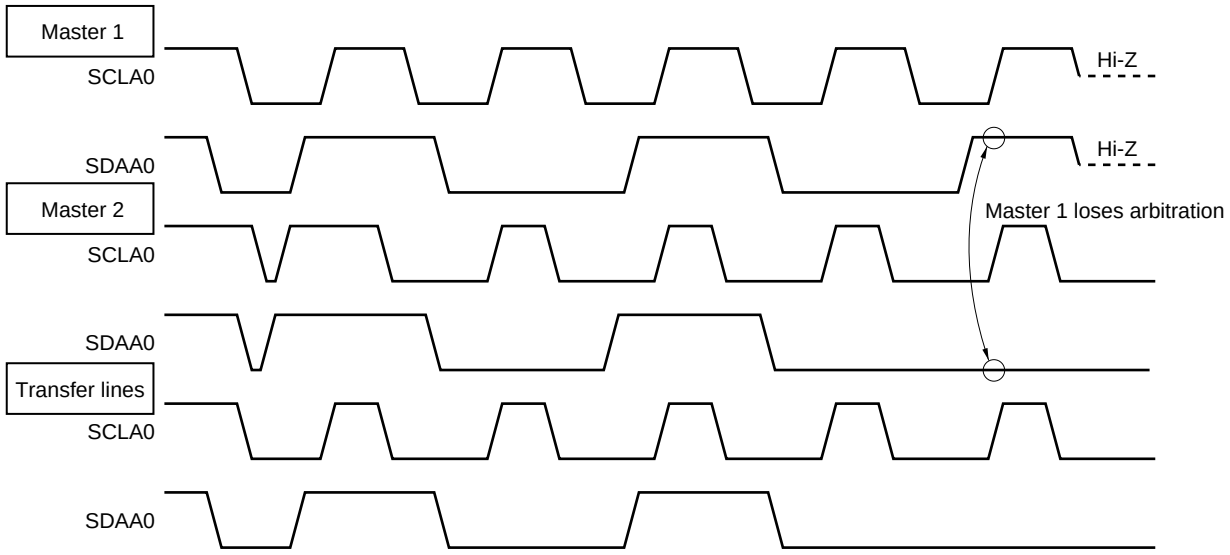
When one of the master devices loses in arbitration, an arbitration loss flag (ALD0) in the IICA status register 0 (IICAS0) is set (1) via the timing by which the arbitration loss occurred, and the SCLA0 and SDAA0 lines are both set to high impedance, which releases the bus.

The arbitration loss is detected based on the timing of the next interrupt request (the eighth or ninth clock, when a stop condition is detected, etc.) and the ALD0 = 1 setting that has been made by software.

For details of interrupt request timing, refer to **15.5.8 Interrupt request (INTIICA0) generation timing and wait control**.

Remark STD0: Bit 1 of IICA status register 0 (IICAS0)
STT0: Bit 1 of IICA control register 0 (IICACTL0)

Figure 15-22. Arbitration Timing Example



15.5.17 Timing of I^2C interrupt request (INTIICA0) occurrence

The timing of transmitting or receiving data and generation of interrupt request signal INTIICA0, and the value of the IICAS0 register when the INTIICA0 signal is generated are shown below.

Remark ST: Start condition
AD6 to AD0: Address
R/$\overline{W}$: Transfer direction specification
$\overline{ACK}$: Acknowledge
D7 to D0: Data
SP: Stop condition

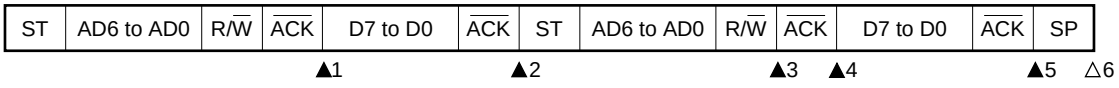
(c) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, does not match address (= extension code))

▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001×000B
▲3: IICAS0 = 0010×010B
▲4: IICAS0 = 0010×000B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, does not match address (= extension code))



▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001××00B
▲3: IICAS0 = 0010×010B
▲4: IICAS0 = 0010×110B
▲5: IICAS0 = 0010××00B
△6: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 19-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection	
				f_X = 10 MHz
0	0	1	$2^{11}/f_X$	204.8 μs
0	1	0	$2^{13}/f_X$	819.2 μs
0	1	1	$2^{14}/f_X$	1.64 ms
1	0	0	$2^{15}/f_X$	3.27 ms
1	0	1	$2^{16}/f_X$	6.55 ms
Other than above			Setting prohibited	

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

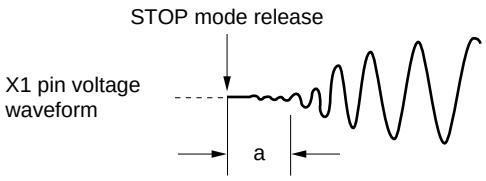
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark f_X: X1 clock oscillation frequency

19.2 Standby Function Operation

19.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock or internal high-speed oscillation clock.

The operating statuses in the HALT mode are shown below.