Renesas Electronics America Inc - UPD78F0744MC-CAA-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	DALI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0744mc-caa-ax

○ Serial interface
- UART6 … Asynchronous 2-wire serial interface
- DALI … 2-wire serial interface for lighting control (slave)
- IICA … Clock synchronous 2-wire serial interface, multimaster supported
  standby can be released upon address match in slave mode
- CSI11 … Clock synchronous 3-wire serial interface, operable as SPI in slave mode

Item / Products	UART6/DALI	IICA	CSI11
78K0/IY2 (16 pins)	–	–	–
78K0/IA2 (20 pins)	1 ch	1 ch	
78K0/IB2 (30 pins)			1 ch
78K0/IB2 (32 pins)			

○ Multiplier (8 bits × 8 bits = 16 bits, 16 bits × 16 bits = 32 bits, 1-clock operation)
○ 10-bit resolution A/D conversion
- 78K0/IY2: 5 ch
- 78K0/IA2: 6 ch
- 78K0/IB2: 9 ch

○ Operational amplifier (Products with operational amplifier only): 1 ch
○ Comparator: 3 ch
○ Power-on-clear (POC) circuit
○ Low-voltage detector (LVI) circuit (An interrupt/reset (selectable) is generated when the detection voltage is reached))
- Detection voltage: Selectable from ten levels between 2.84 and 4.22 V
  *1.91 V is used only when the power is turned on when the LVI default start is set.

○ Single-power-supply flash memory
- Flash self programming enabled
- Software protection function: Protected from outside party copying (no flash reading command)

○ Safety function
- Watchdog timer operated by clock independent from CPU
  … A hang-up can be detected even if the system clock stops
- Supply voltage drop detectable by LVI
  … Appropriate processing can be executed before the supply voltage drops below the operation voltage
- Equipped with option byte function
  … Important system operation settings set in hardware

○ On-chip debug function …Available to control for the target device, and to reference memory
○ Assembler and C language supported
○ Enhanced development environment
- Support for full-function emulator (IECUBE), and simplified emulator (QB-MINI2)

○ Power supply voltage: V_{DD} = 2.7 to 5.5 V
○ Operating ambient temperature: T_A = –40 to +105°C

Table 4-9. Setting Functions of P23/ANI3/CMP2+, P24/ANI4/CMP0+, P25/ANI5/CMP1+ Pins

ADPC0 Register	PM2 Register	CMPmEN bit (m = 0 to 2)	ADS Register (n = 3 to 5)	P23/ANI3/CMP2+, P24/ANI4/CMP0+, P25/ANI5/CMP1+ Pins
Digital I/O selection	Input mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital input
	Output mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital output
Analog input selection	Input mode	0	Selects ANIn.	Analog input (to be converted into digital signal)
			Does not select ANIn.	Analog input (not to be converted into digital signal)
		1	Selects ANIn.	Analog input (to be converted into digital signal), and comparator input
			Does not select ANIn.	Comparator input
	Output mode	–	–	Setting prohibited

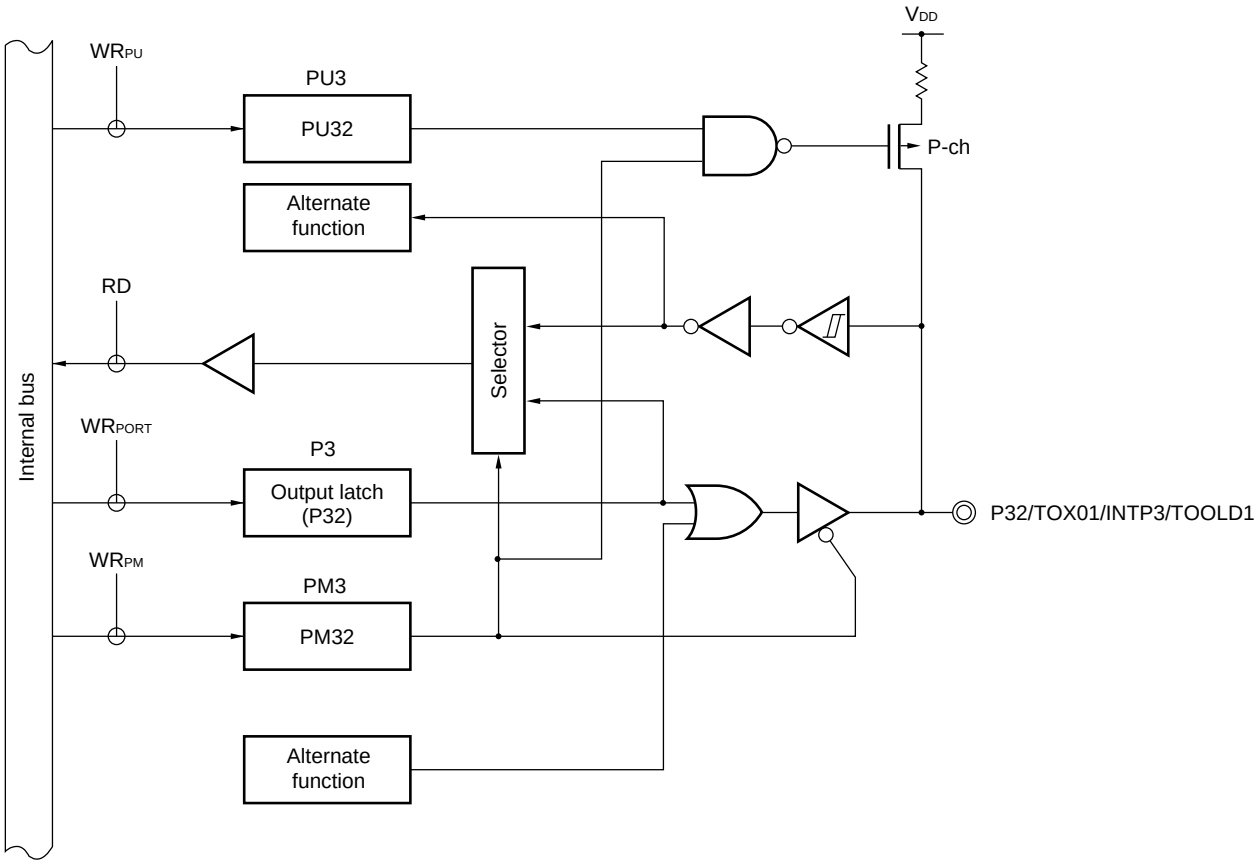
Remark ADPC0: A/D port configuration register 0
PM2: Port mode register 2
CMPmEN: Bit 7 of comparator m control register (CmCTL)
ADS: Analog input channel specification register

Table 4-10. Setting Functions of P26/ANI6/CMPCOM Pin

ADPC0 Register	PM2 Register	CmMODSEL1 bit (m = 0 to 2)	CmMODSEL0 bit (m = 0 to 2)	ADS Register	P26/ANI6/CMPCOM Pin
Digital I/O selection	Input mode	–		Selects ANI6.	Setting prohibited
				Does not select ANI6.	Digital input
	Output mode	–		Selects ANI6.	Setting prohibited
				Does not select ANI6.	Digital output
Analog input selection	Input mode	CmMODSEL1 = 0, or CmMODSEL0 = 0		Selects ANI6.	Analog input (to be converted into digital signal)
				Does not select ANI6.	Analog input (not to be converted into digital signal)
		CmMODSEL1 = 1, and CmMODSEL0 = 1		Selects ANI6.	Analog input (to be converted into digital signal), and comparator common input
				Does not select ANI6.	Comparator common input
	Output mode	–		–	Setting prohibited

Remark ADPC0: A/D port configuration register 0
PM2: Port mode register 2
CmMODSEL1, CmMODSEL0: Bits 4, 3 of comparator m control register (CmCTL)
ADS: Analog input channel specification register

Figure 4-14. Block Diagram of P32



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

5.6.7 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 5-8. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 (The CPU is operating on the high-speed system clock)	RSTOP = 1
X1 clock	MCS = 0 (The CPU is operating on the internal high-speed oscillation clock)	MSTOP = 1
External main system clock		

5.6.8 Peripheral hardware and source clocks

The following lists peripheral hardware and source clocks incorporated in the 78K0/Ix2 microcontrollers.

Remark The peripheral hardware depends on the product. Refer to **1.4 Block Diagram** and **1.5 Outline of Functions**.

Table 5-9. Peripheral Hardware and Source Clocks

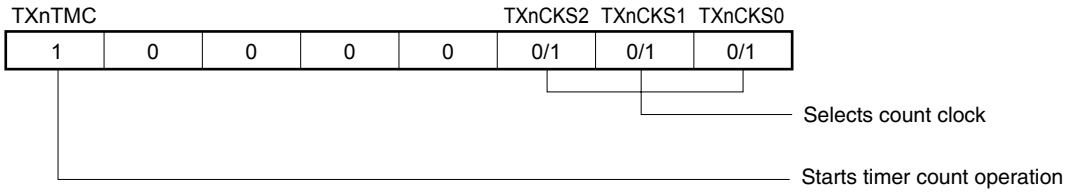
Peripheral Hardware \ Source Clock		Peripheral Hardware Clock (f_{PRS})	Internal Low-Speed Oscillation Clock (f_{IL})	TMX control clock (f_{TMX})	External Clock from Peripheral Hardware Pins
16-bit timers X0 and X1		Y	N	Y	N
16-bit timer/event counter 00		Y	N	N	Y (TI000 pin)[Note]
8-bit timer/event counter 51		Y	N	N	Y (TI51 pin)[Note]
8-bit timer H1		Y	Y	N	N
Watchdog timer		N	Y	N	N
A/D converter		Y	N	N	N
Serial interface	UART6/ DALI	Y	N	N	N
	CSI11	Y	N	N	Y ($\overline{\text{SCK11}}$ pin)[Note]
	IICA	Y	N	N	Y (SCLA0 pin)[Note]

Note Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when in the STOP mode.

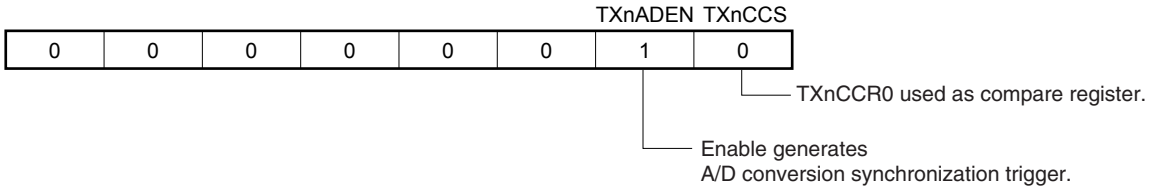
Remark Y: Can be selected, N: Cannot be selected

Figure 6-22. Example of Register Settings for A/D Conversion Start Timing Signal Output

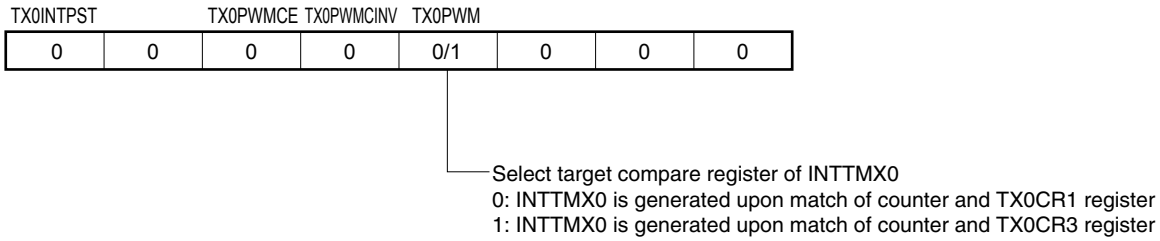
(a) 16-bit timer Xn operation control register 0 (TXnCTL0)



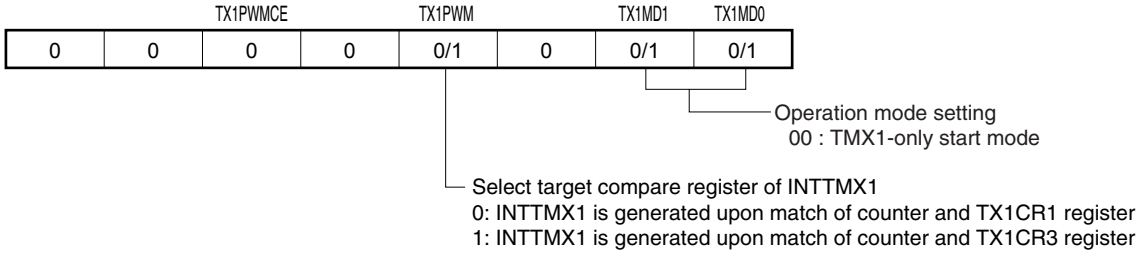
(b) 16-bit timer Xn operation control register 2 (TXnCTL2)



(c) 16-bit timer X0 operation control register 1 (TX0CTL1)



(d) 16-bit timer X1 operation control register 1 (TX1CTL1)



(e) 16-bit timer Xn compare register m (TXnCRm)

If N is set to TXnCRm, the A/D conversion synchronization trigger generation period is as follows.

- The A/D conversion synchronization trigger generation period = (N + 1) × Count clock cycle

Setting TXnCRm to 0000H is prohibited.

(f) 16-bit timer Xn capture/compare register 0 (TXnCCR0)

If M is set to TXnCCR0, the A/D conversion synchronization trigger is generated at a time later than counting 0000H only for M.

Remarks 1. m = 1, 3
n = 0, 1

2. For details of A/D conversion in combination with 16 bit timer X0 or X1, refer to **11.4.2 Basic operation of A/D converter (timer trigger mode)**.

7.2 Configuration of 16-Bit Timer/Event Counter 00

16-bit timer/event counter 00 includes the following hardware.

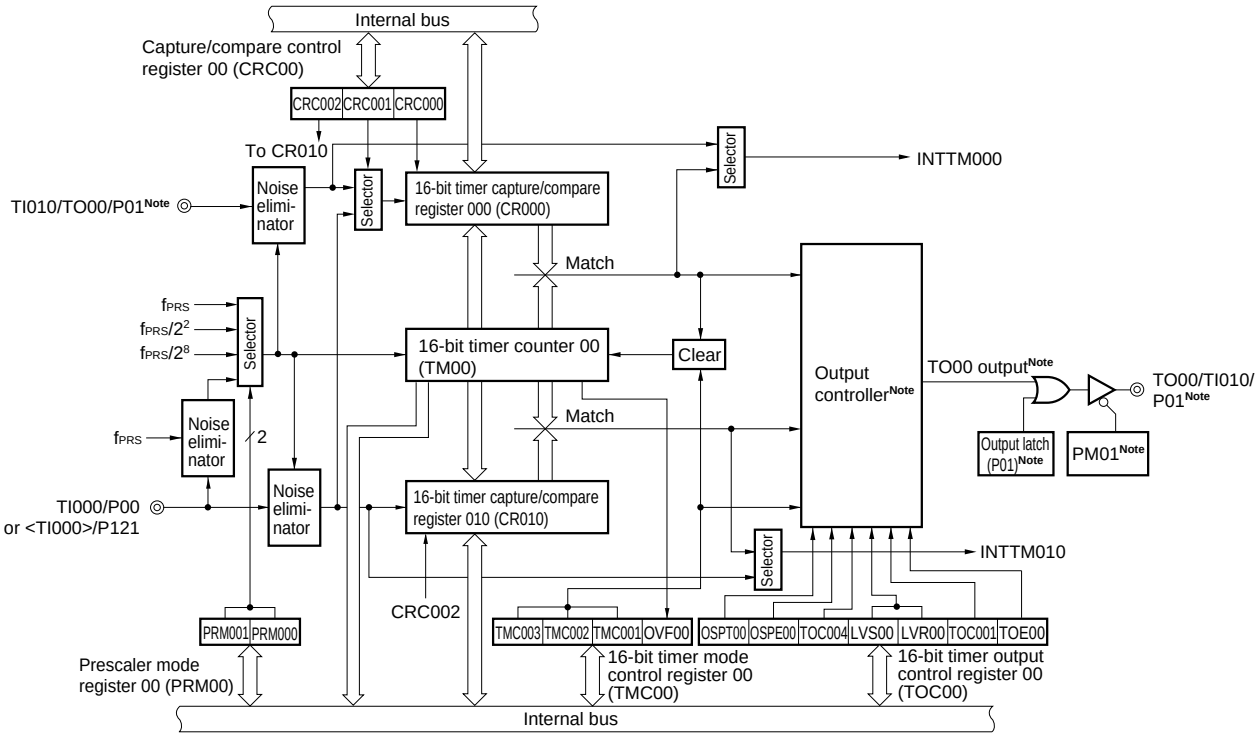
Table 7-1. Configuration of 16-Bit Timer/Event Counter 00

Item	Configuration
Time/counter	16-bit timer counter 00 (TM00)
Register	16-bit timer capture/compare registers 000, 010 (CR000, CR010)
Timer input	TI000, TI010Note
Timer output	TO00Note, output controllerNote
Control registers	16-bit timer mode control register 00 (TMC00) 16-bit timer capture/compare control register 00 (CRC00) 16-bit timer output control register 00 (TOC00)Note Prescaler mode register 00 (PRM00) Port alternate switch control register (MUXSEL) Port mode register 0 (PM0) Port register 0 (P0)

Note 78K0/IB2 (30 pins) only

Figure 7-1 shows the block diagram.

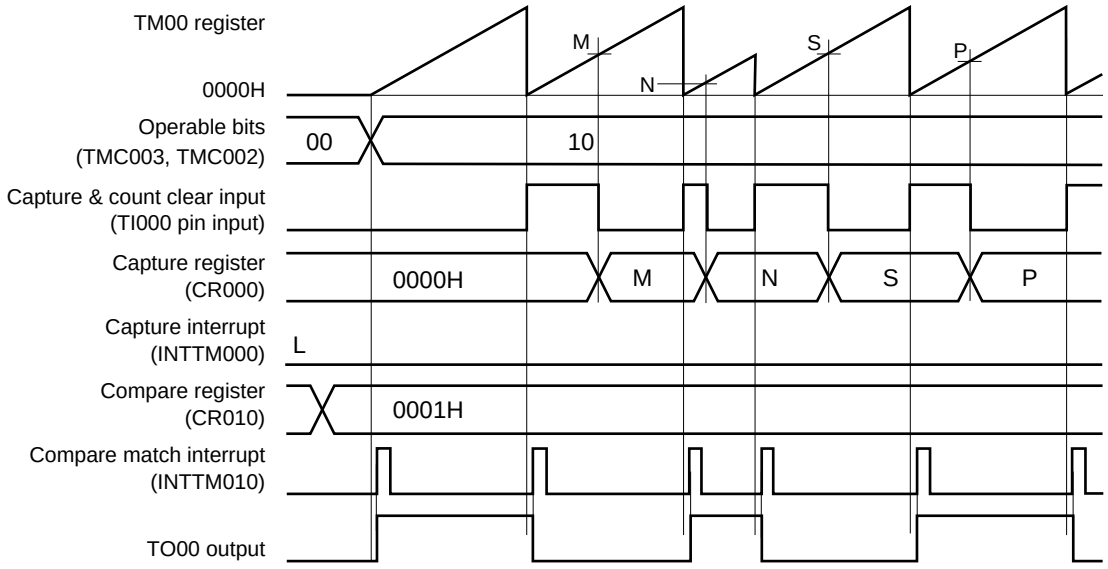
Figure 7-1. Block Diagram of 16-Bit Timer/Event Counter 00



Note 78K0/IB2 (30 pins) only

Figure 7-28. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00 = 03H, TMC00 = 08H, CR010 = 0001H



This is an application example where the TO00 output level is to be inverted when the count value has been captured & cleared.

TM00 is cleared at the rising edge detection of the TI000 pin and it is captured to CR000 at the falling edge detection of the TI000 pin.

When bit 1 (CRC001) of capture/compare control register 00 (CRC00) is set to 1, the count value of TM00 is captured to CR000 in the phase reverse to that of the signal input to the TI000 pin, but the capture interrupt signal (INTTM000) is not generated. However, the INTTM000 signal is generated when the valid edge of the TI010 pin is detected. Mask the INTTM000 signal when it is not used.

Figure 9-4. Format of 8-Bit Timer H Mode Register 1 (TMHMD1)

Address: FF6CH After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD1	TMHE1	CKS12	CKS11	CKS10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS12	CKS11	CKS10	Count clock selection				
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz	f_{PRS} = 20 MHz (when using PLL)
0	0	0	f_{PRS}	2 MHz	5 MHz	10 MHz	20 MHz
0	0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz
0	1	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz	312.5 kHz
1	0	0	$f_{PRS}/2^{12}$	0.49 kHz	1.22 kHz	2.44 kHz	4.88 kHz
1	0	1	$f_{IL}/2^6$	0.47 kHz (TYP.)			
1	1	0	$f_{IL}/2^{15}$	0.92 Hz (TYP.)			
1	1	1	f_{IL}	30 kHz (TYP.)			

TMMD11	TMMD10	Timer operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode
1	1	Setting prohibited

TOLEV1	Timer output level control (in default mode)
0	Low level
1	High level

TOEN1	Timer output control
0	Disables output
1	Enables output

Cautions 1. When TMHE1 = 1, setting the other bits of TMHMD1 is prohibited. However, TMHMD1 can be refreshed (the same value is written).

2. In the PWM output mode and carrier generator mode, be sure to set the 8-bit timer H compare register 11 (CMP11) when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

3. When the carrier generator mode is used, set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

14.3 Registers Controlling Serial Interface UART6/DALI

Serial interface UART6/DALI is controlled by the following nine registers.

○ In UART mode

- UART/DALI mode control register (UADLCTL)
- UART/DALI operation mode register 6 (ASIM6)
- UART/DALI reception error status register 6 (ASIS6)
- UART transmission status register 6 (ASIF6)
- Clock selection register 6 (CKSR6)
- Baud rate generator control register 6 (BRGC6)
- LIN operation control register 6 (ASICL6)
- Input switch control register (ISC)
- Port mode register 6 (PM6)
- Port register 6 (P6)
- Port output mode register 6 (POM6)

○ In DALI mode

- UART/DALI mode control register (UADLCTL)
- UART/DALI operation mode register 6 (ASIM6)
- UART/DALI reception error status register 6 (ASIS6)
- Clock selection register 6 (CKSR6)
- Baud rate generator control register 6 (BRGC6)
- Port mode register 6 (PM6)
- Port output mode register 6 (POM6)

(1) UART/DALI mode control register (UADLCTL)

This is an 8-bit register that controls whether to operate serial interface UART6/DALI in UART mode or DALI mode.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 00H.

Figure 14-5. Format of UART/DALI mode control register (UADLCTL)

Address: FF5BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
UADLCTL	0	0	0	0	0	0	0	UADLSEL

UADLSEL	Operation mode
0	UART mode
1	DALI mode

Note Make sure that POWER6, TXE6 and RXE6 = 0 when rewriting the UADLSEL bit.

(10) Port output mode register 6 (POM6)

This register sets the output mode of P60 and P61 in 1-bit units.

When using the P60/TxD6/SCLA0 pin as the data output of serial interface UART6/DALI, clear POM60 to 0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

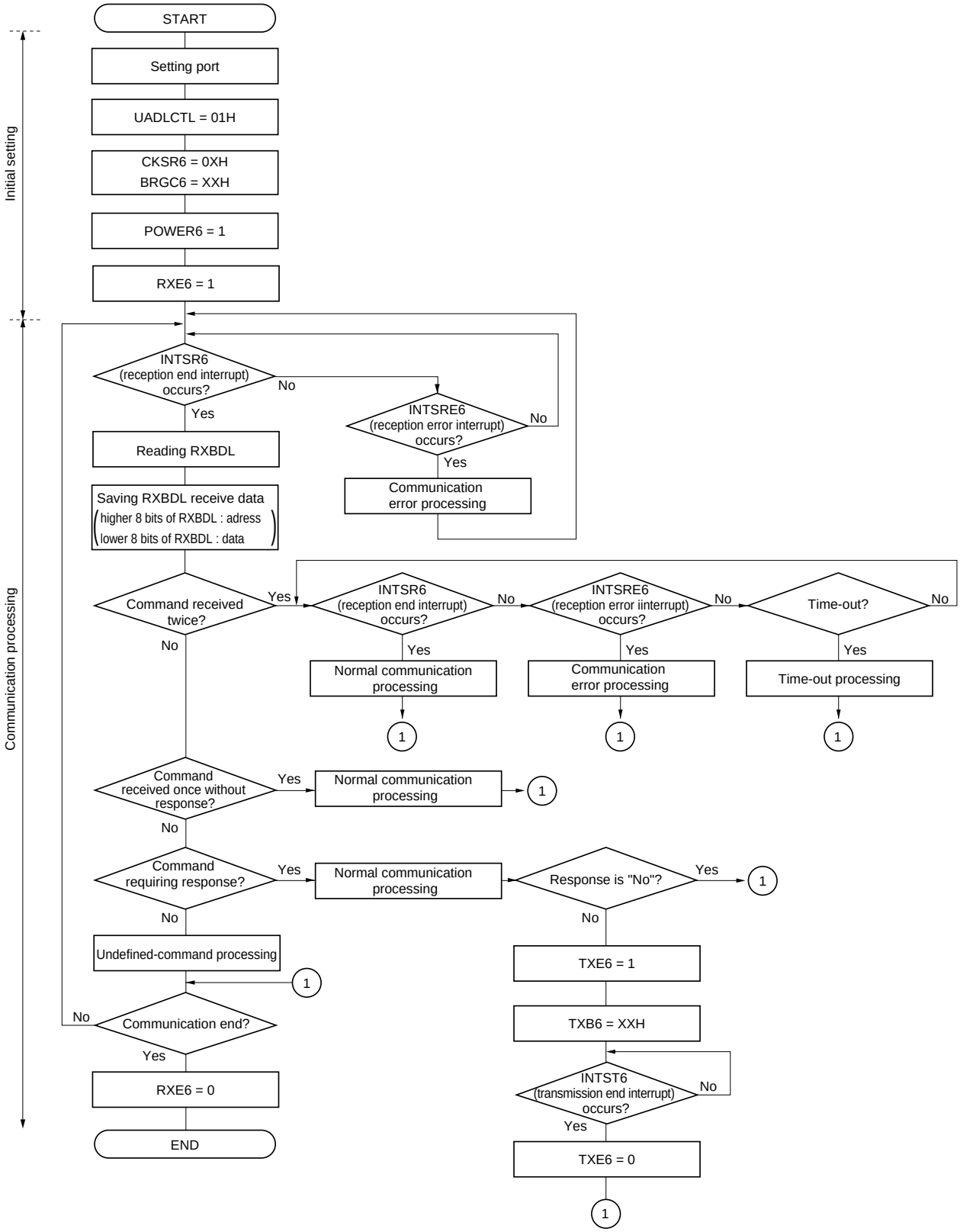
Figure 14-14. Format of Port Output Mode Register 6 (POM6)

Address: FF2AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
POM6	0	0	0	0	0	0	POM61	POM60

POM6n	P6n pin output mode selection (n = 0, 1)
0	Normal output (CMOS output) mode
1	N-ch open drain output (V_{DD} tolerance) mode

Figure 14-31. Example of DALI Communication (Slave Transmission/Reception) Flow Chart



15.5.16 Communication operations

The following shows three operation procedures with the flowchart.

(1) Master operation in single master system

The flowchart when using the 78K0/Kx2-L microcontrollers as the master in a single master system is shown below. This flowchart is broadly divided into the initial settings and communication processing. Execute the initial settings at startup. If communication with the slave is required, prepare the communication and then execute communication processing.

(2) Master operation in multimaster system

In the I^2C bus multimaster system, whether the bus is released or used cannot be judged by the I^2C bus specifications when the bus takes part in a communication. Here, when data and clock are at a high level for a certain period (1 frame), the 78K0/Kx2-L microcontrollers take part in a communication with bus released state.

This flowchart is broadly divided into the initial settings, communication waiting, and communication processing. The processing when the 78K0/Kx2-L microcontrollers lose in arbitration and is specified as the slave is omitted here, and only the processing as the master is shown. Execute the initial settings at startup to take part in a communication. Then, wait for the communication request as the master or wait for the specification as the slave. The actual communication is performed in the communication processing, and it supports the transmission/reception with the slave and the arbitration with other masters.

(3) Slave operation

An example of when the 78K0/Kx2-L microcontrollers are used as the I^2C bus slave is shown below.

When used as the slave, operation is started by an interrupt. Execute the initial settings at startup, then wait for the INTIICA0 interrupt occurrence (communication waiting). When an INTIICA0 interrupt occurs, the communication status is judged and its result is passed as a flag over to the main processing.

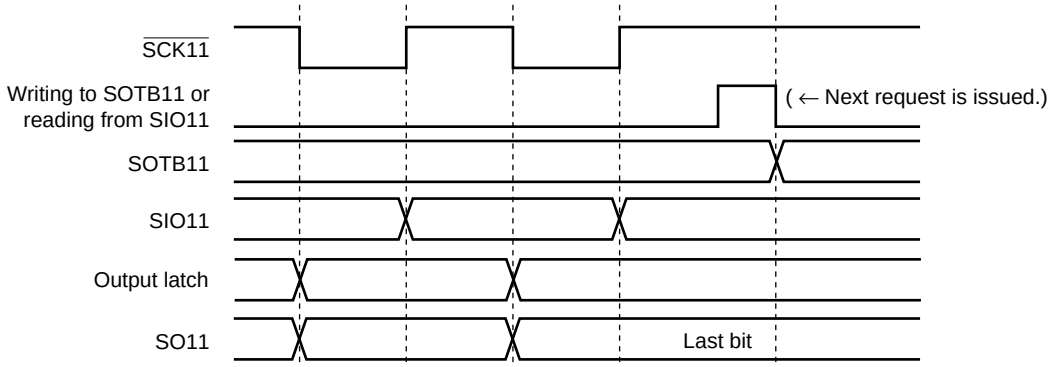
By checking the flags, necessary communication processing is performed.

(4) Output value of SO11 pin (last bit)

After communication has been completed, the SO11 pin holds the output value of the last bit.

Figure 16-9. Output Value of SO11 Pin (Last Bit) (1/2)

(a) Type 1: CKP11 = 0, DAP11 = 0



(b) Type 3: CKP11 = 1, DAP11 = 0

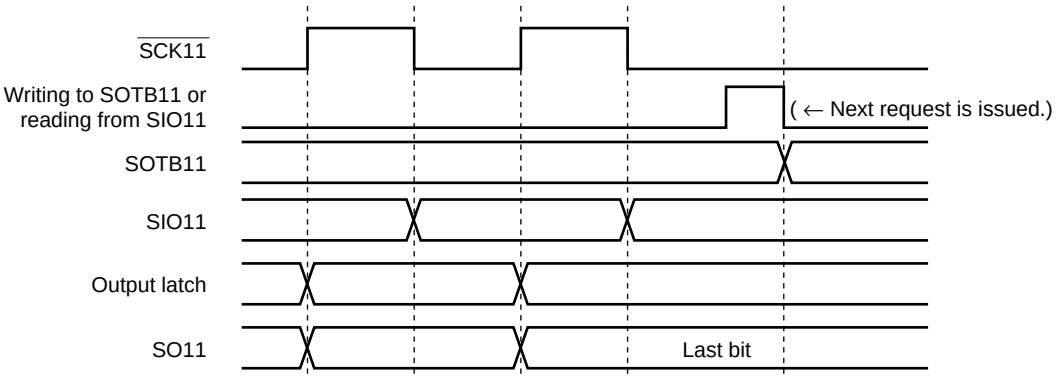


Table 18-3 shows the ports corresponding to EGPn and EGNn.

Table 18-3. Ports Corresponding to EGPn and EGNn (1/2)

(1) 78K0/IY2

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P121 or P125[Note]	INTP0
EGP2	EGN2	P31	INTP2
EGP3	EGN3	P32	INTP3
EGP4	EGN4	P34	INTP4
EGP6	EGN6	–	INTCMP0
EGP7	EGN7	–	INTCMP1
EGP8	EGN8	–	INTCMP2

(2) 78K0/IA2

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P00 or P121[Note]	INTP0
EGP2	EGN2	P31	INTP2
EGP3	EGN3	P32	INTP3
EGP4	EGN4	P34	INTP4
EGP6	EGN6	–	INTCMP0
EGP7	EGN7	–	INTCMP1
EGP8	EGN8	–	INTCMP2

Note The pin functions can be assigned by setting the port alternate switch control register (MUXSEL).

Caution Select the port mode by clearing EGPn and EGNn to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0, 2 to 4, 6 to 8

Table 25-1. Set Values of Internal Memory Size Switching Register

Products			IMS Setting
78K0/IY2	78K0/IA2	78K0/IB2	
μPD78F0740, 78F0750	–	–	61H
μPD78F0741, 78F0751	μPD78F0743, 78F0753	μPD78F0745, 78F0755	42H
μPD78F0742, 78F0752	μPD78F0744, 78F0754	μPD78F0746, 78F0756	04H

25.2 Writing with Flash Memory Programmer

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the 78K0/Ix2 microcontrollers have been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the 78K0/Ix2 microcontrollers are mounted on the target system.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

25.6 Security Settings

The 78K0/Ix2 microcontrollers support a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed using the Security Set command. The security setting is valid when the programming mode is set next.

- Disabling batch erase (chip erase)
  Execution of the block erase and batch erase (chip erase) commands for entire blocks in the flash memory is prohibited by this setting during on-board/off-board programming. Once execution of the batch erase (chip erase) command is prohibited, all of the prohibition settings (including prohibition of batch erase (chip erase)) can no longer be cancelled.

  Caution After the security setting for the batch erase is set, erasure cannot be performed for the device. In addition, even if a write command is executed, data different from that which has already been written to the flash memory cannot be written, because the erase command is disabled.

- Disabling block erase
  Execution of the block erase command for a specific block in the flash memory is prohibited during on-board/off-board programming. However, blocks can be erased by means of self programming.

- Disabling write
  Execution of the write and block erase commands for entire blocks in the flash memory is prohibited during on-board/off-board programming. However, blocks can be written by means of self programming.

- Disabling rewriting boot cluster 0
  Execution of the block erase command and write command on boot cluster 0 (0000H to 0FFFH) in the flash memory is prohibited by this setting. Execution of the batch erase (chip erase) command is also prohibited by this setting.

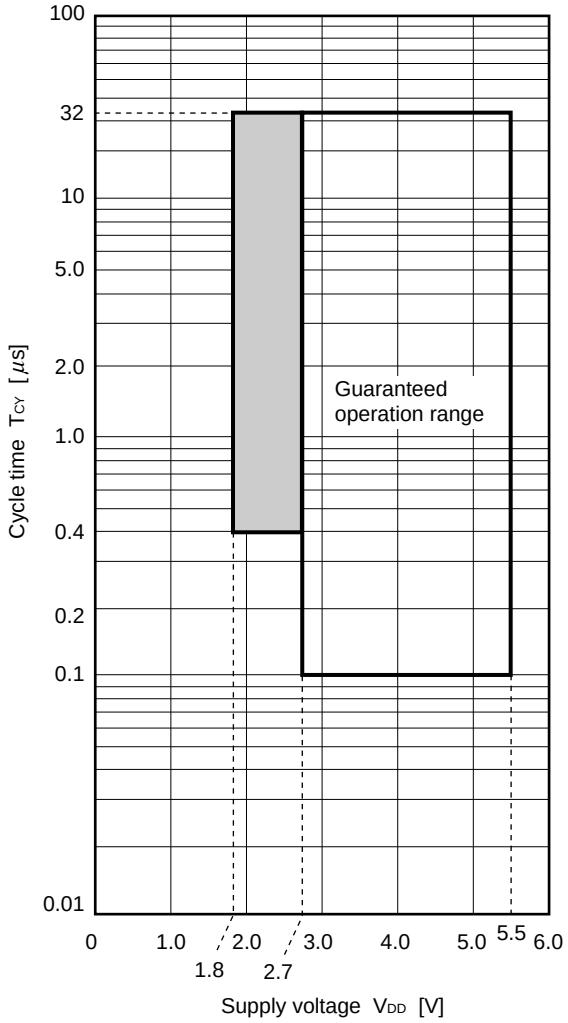
The batch erase (chip erase), block erase, write commands, and rewriting boot cluster 0 are enabled by the default setting when the flash memory is shipped. Security can be set by on-board/off-board programming and self programming. Each security setting can be used in combination.

All the security settings are cleared by executing the batch erase (chip erase) command.

Table 25-7 shows the relationship between the erase and write commands when the 78K0/Ix2 microcontroller security function is enabled.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

T_{CY} vs. V_{DD} (Main System Clock Operation, RMC = 00H (Normal Power Mode))



Caution The following operations and register settings can be performed in the shaded area in the figure (1.8 V ≤ V_{DD} < 2.7 V), as long as T_A = –40 to +85ºC:

- **CPU operations (instruction execution)**
  CPU clock: 62.5 kHz to 5 MHz
- **Reading and writing the internal RAM**
- **Low-voltage detector (LVI) operations**
- **Interval timer operations using 8-bit timer 51**
- **Interval timer operations using 8-bit timer H1**
- **Standby settings (STOP and HALT modes)**
- **Clock generator control register settings (except in PLL clock mode)**
  However, the clock can only be switched if the cycle time following the switch is at 0.4 μs or longer.
- **Watchdog timer (WDT) operations (including operations related to the internal low-speed oscillator)**
- **Port settings**
  Registers: PMxx, Pxx, PUxx, PIM6[Note 1], POM6[Note 1], RSTMASK, ADPC0, ADPC1[Note 2], MUXSEL

Notes 1. 78K0/IA2, 78K0/IB2 only

2. 78K0/IB2 only

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

28.5.7 Supply Voltage Rise Time

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 2.7 V (V_{DD} (MIN.)) Note (V_{DD}: 0 V → 2.7 V)	t_{PUP1}	LVI default start function stopped is set (LVISTART (Option Byte) = 0), when $\overline{\text{RESET}}$ input is not used			5.4	ms
Maximum time to rise to 2.7 V (V_{DD} (MIN.)) Note (releasing $\overline{\text{RESET}}$ input → V_{DD}: 2.7 V)	t_{PUP2}	LVI default start function stopped is set (LVISTART (Option Byte) = 0), when $\overline{\text{RESET}}$ input is used			1.9	ms

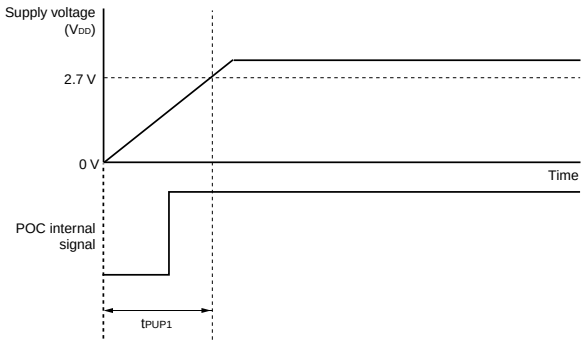
Note Make sure to raise the power supply in a shorter time than this.

Caution The operation guaranteed range is 2.7 V ≤ V_{DD} ≤ 5.5 V. If the rise of the voltage to reach 2.7 V after turning on the power is more gradual than 0.5 V/ms (MIN.), perform one of the following operations.

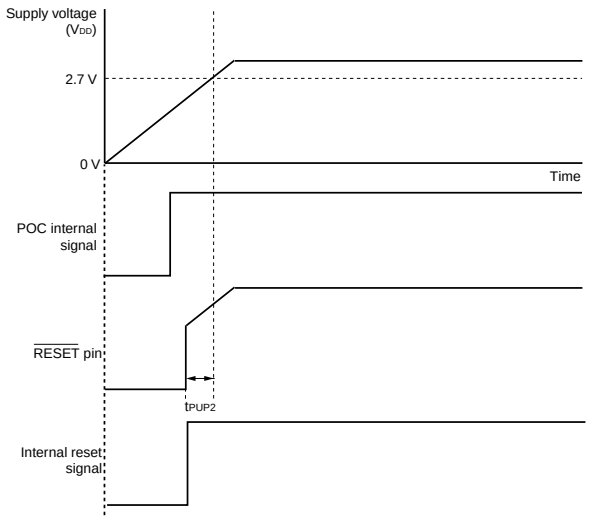
- **Input a low level to the $\overline{\text{RESET}}$ pin until 2.7 V is reached after turning on the power.**
- **Set the LVI default start function to operate (LVISTART = 1) using the option byte and perform a wait processing until the supply voltage rises from 1.91 V (TYP.) to 2.7 V.**

Supply Voltage Rise Time Timing

- When $\overline{\text{RESET}}$ pin input is not used



- When $\overline{\text{RESET}}$ pin input is used (when external reset is released by the $\overline{\text{RESET}}$ pin, after POC has been released)



APPENDIX B REGISTER INDEX

[A]

ADCR: 10-bit A/D conversion result register 372
ADCRH: 8-bit A/D conversion result register H 373
ADCRL: 8-bit A/D conversion result register L 373
ADCRX0: 10-bit A/D conversion result register for TMX0 synchronization 374
ADCRX0L: 8-bit A/D conversion result register L for TMX0 synchronization 374
ADCRX1 : 10-bit A/D conversion result register for TMX1 synchronization 374
ADCRX1L : 8-bit A/D conversion result register L for TMX1 synchronization 374
ADM0: A/D converter mode register 0 368
ADPC0: A/D port configuration register 0 ..... 141, 377, 403, 420
ADPC1: A/D port configuration register 1 ..... 141, 377
ADS: Analog input channel specification register 375, 404
AMP0M : Operational amplifier control register 402
ASICL6: LIN operation control register 6 440
ASIF6: UART transmission status register 6 438
ASIM6: UART/DALI operation mode register 6 435
ASIS6: UART/DALI reception error status register 6 437

[B]

BRGC6: Baud rate generator control register 6 440

[C]

C0CTL : Comparator 0 control register 411
C0RVM : DA0 internal reference voltage selection register 415
C1CTL : Comparator 1 control register 411
C1RVM : DA1 internal reference voltage selection register 425
C2CTL : Comparator 2 control register 411
C2RVM : DA2 internal reference voltage selection register 415
CKSR6: Clock selection register 6 438
CMP01: 8-bit timer H compare register 01 335
CMP11: 8-bit timer H compare register 11 335
CMPFLG : Comparator output flag register 419
CR000: 16-bit timer capture/compare register 000 254
CR010: 16-bit timer capture/compare register 010 254
CR51: 8-bit timer compare register 51 325
CRC00: Capture/compare control register 00 259
CSIC11: Serial clock selection register 11 552
CSIM11: Serial operation mode register 11 551

[E]

EGNCTL0: External interrupt falling edge enable register 0 588
EGNCTL1: External interrupt falling edge enable register 1 588
EGPCTL0: External interrupt rising edge enable register 0 588
EGPCTL1: External interrupt rising edge enable register 1 588

P7: Port register 7 136
P12: Port register 12 136
PCC: Processor clock control register 159
PIM6: Port input mode register 6 ..... 140, 490
PM0: Port mode register 0 ..... 134, 266, 328, 340, 554
PM2: Port mode register 2 ..... 134, 378, 405, 421
PM3: Port mode register 3 ..... 134, 203, 328, 340, 554
PM6: Port mode register 6 ..... 134, 443, 491
PM7: Port mode register 7 ..... 134, 378
POM6: Port output mode register 6 ..... 141, 444, 491
PR0H: Priority specification flag register 0H 584
PR0L: Priority specification flag register 0L 584
PR1H: Priority specification flag register 1H 584
PR1L: Priority specification flag register 1L 584
PRM00: Prescaler mode register 00 263
PU0: Pull-up resistor option register 0 138
PU3: Pull-up resistor option register 3 138
PU6: Pull-up resistor option register 6 138
PU12: Pull-up resistor option register 12 138

[R]

RCM: Internal oscillation mode register 160
RESF: Reset control flag register 623
RMC: Regulator mode control register 644
RSTMASK: Reset pin mode register 141
RXB6: UART receive buffer register 6 433
RXBDL: DALI receive buffer register 433
RXS6: UART/DALI receive shift register 6 433

[S]

SIO11: Serial I/O shift register 11 551
SOTB11: Transmit buffer register 11 550
SVA0: Slave address register 0 477

[T]

TCL51: Timer clock selection register 51 326
TM00: 16-bit timer counter 00 253
TM51: 8-bit timer counter 51 324
TMC00: 16-bit timer mode control register 00 258
TMC51: 8-bit timer mode control register 51 327
TMCYC1: 8-bit timer H carrier control register 1 338
TMHMD1: 8-bit timer H mode register 1 336
TOC00: 16-bit timer output control register 00 261
TX0CCR0: 16-bit timer X0 capture/compare register 0 190
TX0CR0: 16-bit timer X0 compare register 0 190
TX0CR1: 16-bit timer X0 compare register 1 190
TX0CR2: 16-bit timer X0 compare register 2 190
TX0CR3: 16-bit timer X0 compare register 3 190