Renesas Electronics America Inc - UPD78F0745MC-CAB-AX Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, DALI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0745mc-cab-ax

○ Serial interface
- UART6 … Asynchronous 2-wire serial interface
- DALI … 2-wire serial interface for lighting control (slave)
- IICA … Clock synchronous 2-wire serial interface, multimaster supported
  standby can be released upon address match in slave mode
- CSI11 … Clock synchronous 3-wire serial interface, operable as SPI in slave mode

Item / Products	UART6/DALI	IICA	CSI11
78K0/IY2 (16 pins)	–	–	–
78K0/IA2 (20 pins)	1 ch	1 ch	
78K0/IB2 (30 pins)			1 ch
78K0/IB2 (32 pins)			

○ Multiplier (8 bits × 8 bits = 16 bits, 16 bits × 16 bits = 32 bits, 1-clock operation)
○ 10-bit resolution A/D conversion
- 78K0/IY2: 5 ch
- 78K0/IA2: 6 ch
- 78K0/IB2: 9 ch

○ Operational amplifier (Products with operational amplifier only): 1 ch
○ Comparator: 3 ch
○ Power-on-clear (POC) circuit
○ Low-voltage detector (LVI) circuit (An interrupt/reset (selectable) is generated when the detection voltage is reached))
- Detection voltage: Selectable from ten levels between 2.84 and 4.22 V
  *1.91 V is used only when the power is turned on when the LVI default start is set.

○ Single-power-supply flash memory
- Flash self programming enabled
- Software protection function: Protected from outside party copying (no flash reading command)

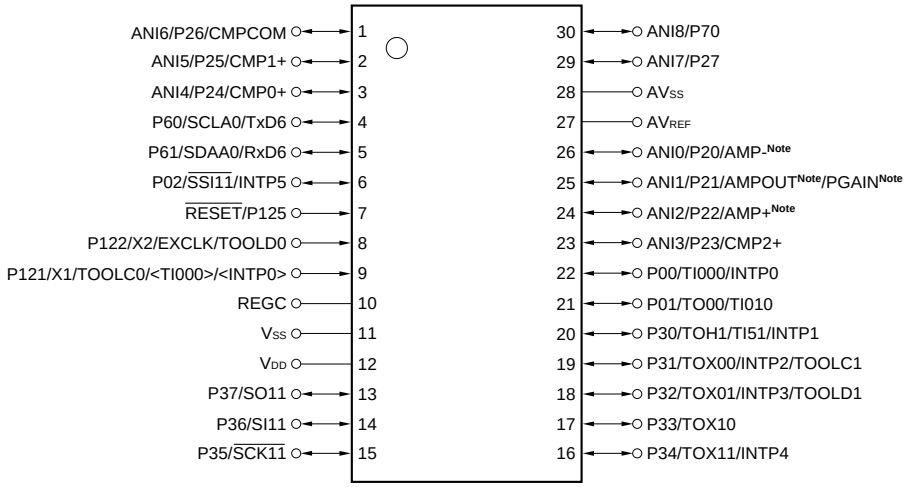
○ Safety function
- Watchdog timer operated by clock independent from CPU
  … A hang-up can be detected even if the system clock stops
- Supply voltage drop detectable by LVI
  … Appropriate processing can be executed before the supply voltage drops below the operation voltage
- Equipped with option byte function
  … Important system operation settings set in hardware

○ On-chip debug function …Available to control for the target device, and to reference memory
○ Assembler and C language supported
○ Enhanced development environment
- Support for full-function emulator (IECUBE), and simplified emulator (QB-MINI2)

○ Power supply voltage: V_{DD} = 2.7 to 5.5 V
○ Operating ambient temperature: T_A = –40 to +105°C

1.3.3 78K0/IB2

- 30-pin plastic SSOP (7.62 mm (300))



AMP-Note, AMP+Note:	Amplifier Input	REGC :	Regulator Capacitance
AMPOUTNote :	Amplifier Output	RESET :	Reset
PGAINNote :	Programmable Gain	RxD6 :	Receive Data
	Amplifier Input	SCLA0, SCK11 :	Serial Clock Input/Output
ANI0 to ANI8 :	Analog Input	SDAA0 :	Serial Data Input/Output
AVREF :	Analog Reference	SI11 :	Serial Data Input
	Voltage	SO11 :	Serial Data Output
AVSS :	Analog Ground	SSI11 :	Serial Interface Chip
EXCLK :	External Clock Input	TI000, TI010, TI51 :	Timer Input
	(Main System Clock)	TO00, TOH1 :	Timer Output
CMP0+ to CMP2+ :	Comparator Input	TOOLC0, TOOLC1 :	Clock Input for Tool
CMPCOM :	Comparator Common Input	TOOLD0, TOOLD1 :	Data Input/Output for Tool
INTP0 to INTP5 :	External Interrupt Input	TOX00, TOX01, TOX10,	
P00 to P02 :	Port 0	TOX11 :	Timer Output
P20 to P27 :	Port 2	TxD6 :	Transmit Data
P30 to P37 :	Port 3	VDD :	Power Supply
P60, P61 :	Port 6	VSS :	Ground
P70 :	Port 7	X1, X2 :	Crystal Oscillator
P121, P122, P125 :	Port 12		(Main System Clock)

Note μPD78F0755, 78F0756 (products with operational amplifier) only

Cautions 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

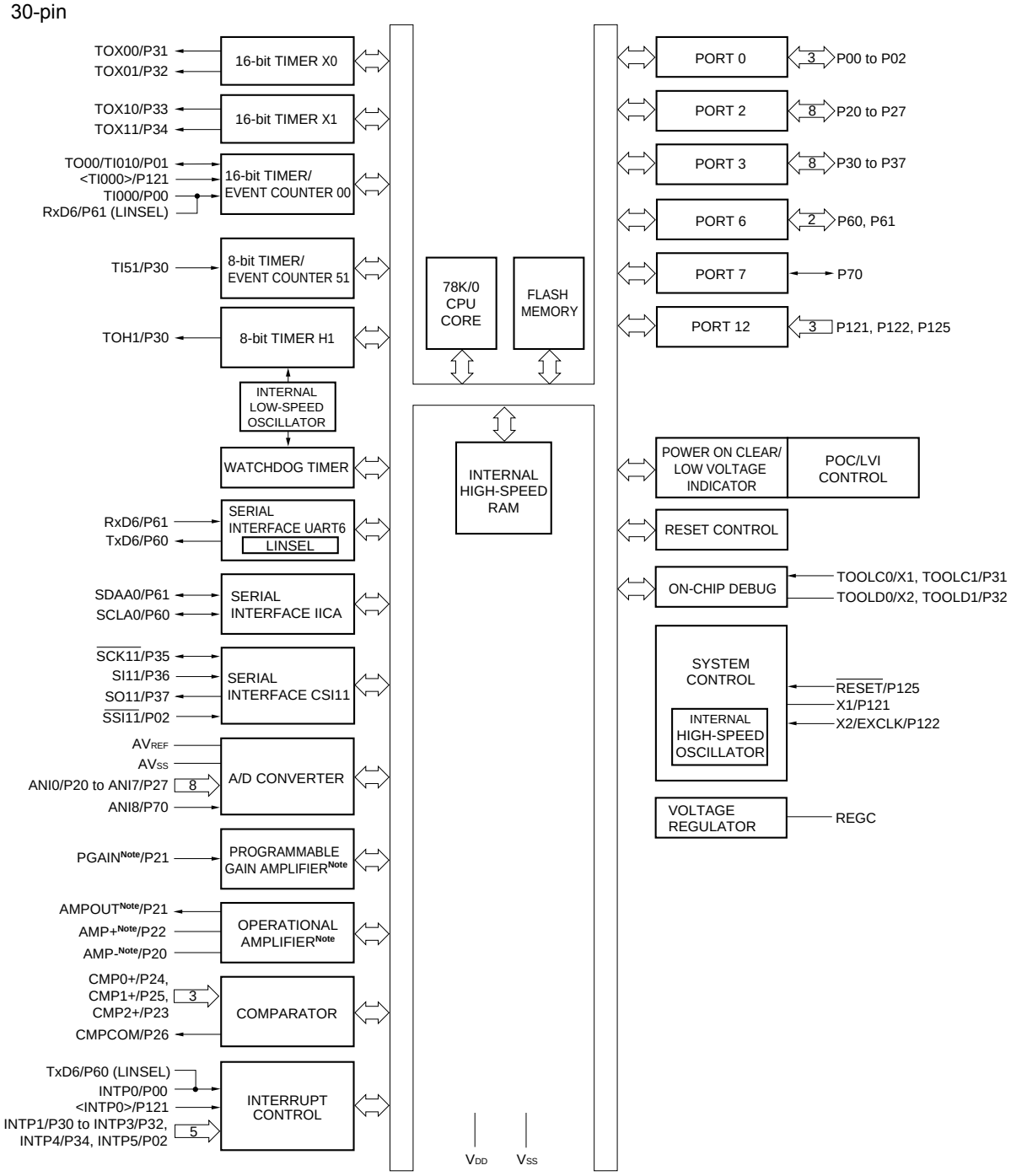
2. ANI0/P20/AMP-, ANI1/P21/AMPOUT/PGAIN, ANI2/P22/AMP+, ANI3/P23/CMP2+, ANI4/P24/CMP0+, ANI5/P25/CMP1+, ANI6/P26/CMPCOM, ANI7/P27, and ANI8/P70 are set in the analog input mode after release of reset.

3. RESET/P125 immediately after release of reset is set in the external reset input.

Remark Functions in angle brackets < > can be assigned by setting the input switch control register (MUXSEL).

1.4.3 78K0/IB2

- 30-pin



Note μPD78F0755, 78F0756 (products with operational amplifier) only

Cautions 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

2. ANI0/P20/AMP-, ANI1/P21/AMPOUT/PGAIN, ANI2/P22/AMP+, ANI3/P23/CMP2+, ANI4/P24/CMP0+, ANI5/P25/CMP1+, ANI6/P26/CMPCOM, ANI7/P27, and ANI8/P70 are set in the analog input mode after release of reset.

3. $\overline{\text{RESET}}$/P125 immediately after release of reset is set in the external reset input.

Remark Functions in angle brackets < > can be assigned by setting the input switch control register (MUXSEL).

(2) Non-port functions : 78K0/IA2 (2/2)

Function Name	I/O	Function	After Reset	Alternate Function
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input port	P00/INTP0/<TOH1>/<TI51>
				P121/X1/TOOLC0/<INTP0>
TI51	Input	External count clock input to 8-bit timer/event counter 51	Input port	P00/TI000/INTP0/<TOH1>
				P34/TOX11/INTP4/<TOH1>
TOH1	Output	8-bit timer H1 output	Input port	P00/TI000/INTP0/<TI51>
				P34/TOX11/INTP4/<TI51>
TOX00	Output	16-bit timer X0 output	Input port	P31/INTP2/TOOLC1
TOX01				P32/INTP3/TOOLD1
TOX10		16-bit timer X1 output		P33
TOX11				P34/INTP4/<TOH1>/<TI51>
X1	–	Connecting resonator for main system clock	Input port	P121/TOOLC0/<TI000>/<INTP0>
X2				P122/EXCLK/TOOLD0
EXCLK	Input	External clock input for main system clock	Input port	P122/X2/TOOLD0
V_{DD}	–	Positive power supply for pins other than port 2	–	–
AV_{REF}		A/D converter reference voltage input and positive power supply for port 2 and A/D converter		
V_{SS}	–	Ground potential for pins other than port 2	–	–
TOOLC0	Input	Clock input for flash memory programmer/on-chip debugger	Input port	P121/X1/<TI000>/<INTP0>
TOOLC1				P31/TOX00/INTP2
TOOLD0	I/O	Data I/O for flash memory programmer/on-chip debugger		P122/X2/EXCLK
TOOLD1				P32/TOX01/INTP3

Remark Functions in angle brackets < > can be assigned by setting the input switch control register (MUXSEL).

(g) $\overline{\text{SSI11}}$

This is a chip select input pin of serial interface CSI11.

2.2.2 P20 to P27 (port 2)

P20 to P27 function as an I/O port. These pins also function as pins for A/D converter analog input, operational amplifier I/O, and PGA input.

78K0/IY2	78K0/IA2	78K0/IB2
16 Pins	20 Pins	30 Pins/32 Pins
P20/ANI0	P20/ANI0/AMP-Note	P20/ANI0/AMP-Note
P21/ANI1/PGAINNote	P21/ANI1/AMPOUTNote/PGAINNote	P21/ANI1/AMPOUTNote/PGAINNote
–	P22/ANI2/AMP+Note	P22/ANI2/AMP+Note
P23/ANI3/CMP2+	P23/ANI3/CMP2+	P23/ANI3/CMP2+
P24/ANI4/CMP0+	P24/ANI4/CMP0+	P24/ANI4/CMP0+
P25/ANI5/CMP1+	P25/ANI5/CMP1+	P25/ANI5/CMP1+
–	–	P26/ANI6/CMPCOM
–	–	P27/ANI7

Note Products with operational amplifier only

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P27 function as an I/O port. P20 to P27 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P27 function as A/D converter analog input, operational amplifier I/O, and PGA input.

(a) ANI0 to ANI7

These are A/D converter analog input pins. When using these pins as analog input pins, refer to **(5) ANI0/P20 to ANI7/P27 and ANI8/P70** in **11.6 Cautions for A/D Converter**.

(b) AMP+, AMP-

These are operational amplifier input pins.

(c) AMPOUT

This is an operational amplifier output pin.

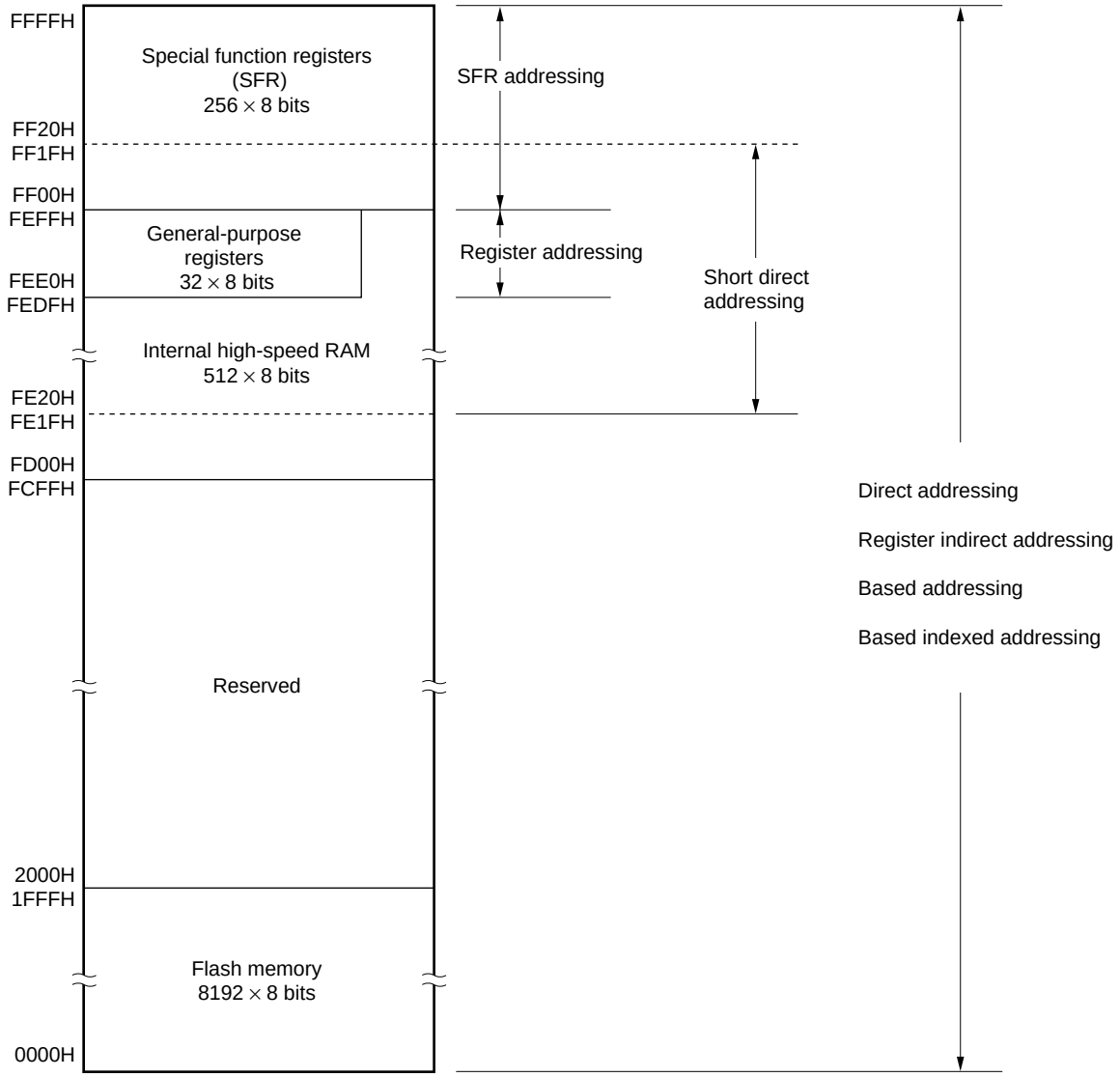
(d) PGAIN

This is a PGA (Programmable gain amplifier) input pin.

(e) CMP0+ to CMP2+

These are comparator input pins.

Figure 3-5. Correspondence Between Data Memory and Addressing
(μPD78F0741, 78F0743, 78F0745, 78F0751, 78F0753, 78F0755)



3.3 Instruction Address Addressing

An instruction address is determined by contents of the program counter (PC) and is normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to PC and branched by the following addressing (for details of instructions, refer to the **78K/0 Series Instructions User's Manual (U12326E)**).

3.3.1 Relative addressing

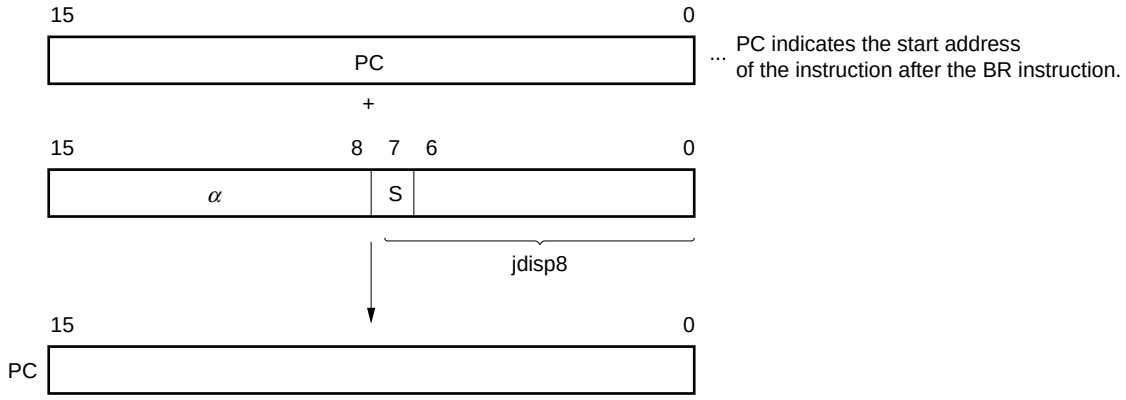
[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (−128 to +127) and bit 7 becomes a sign bit.

In other words, relative addressing consists of relative branching from the start address of the following instruction to the −128 to +127 range.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, all bits of α are 0.
When S = 1, all bits of α are 1.

Table 4-4. Port Functions (78K0/IB2 (30 Pins))

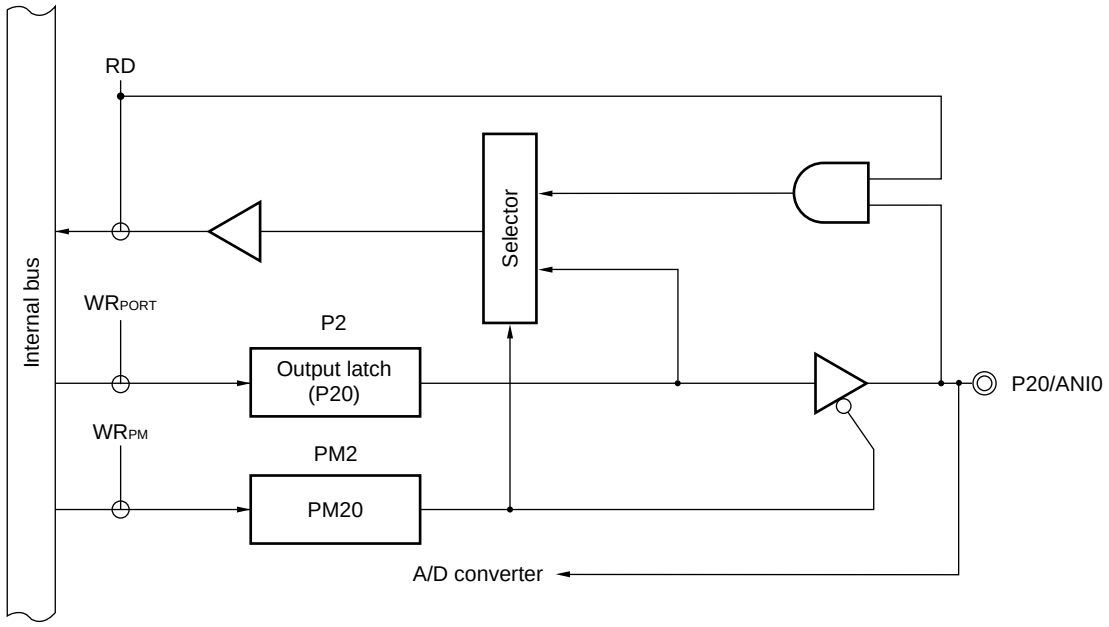
Function Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI000/INTP0
P01				TO00/TI010
P02				$\overline{\text{SSI11}}$/INTP5
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP-Note
P21				ANI1/AMPOUTNote/ PGAINNote
P22				ANI2/AMP+Note
P23				ANI3/CMP2+
P24				ANI4/CMP0+
P25				ANI5/CMP1+
P26				ANI6/CMPCOM
P27				ANI7
P30	I/O	Port 3. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOH1/TI51/INTP1
P31				TOX00/INTP2/TOOLC1
P32				TOX01/INTP3/TOOLD1
P33				TOX10
P34				TOX11/INTP4
P35				$\overline{\text{SCK11}}$
P36				SI11
P37				SO11
P60	I/O	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit units. Input can be set to SMBus input buffer in 1-bit units. Output can be set to N-ch open-drain output (V_{DD} tolerance). Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCLA0/TxD6
P61				SDAA0/RxD6
P70	I/O	Port 7. 1-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI8
P121	Input	Port 12. 3-bit input port. For only P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	X1/TOOLC0/<TI000>/ <INTP0>
P122				X2/EXCLK/TOOLD0
P125				$\overline{\text{RESET}}$

Note μPD78F0755, 78F0756 (products with operational amplifier) only

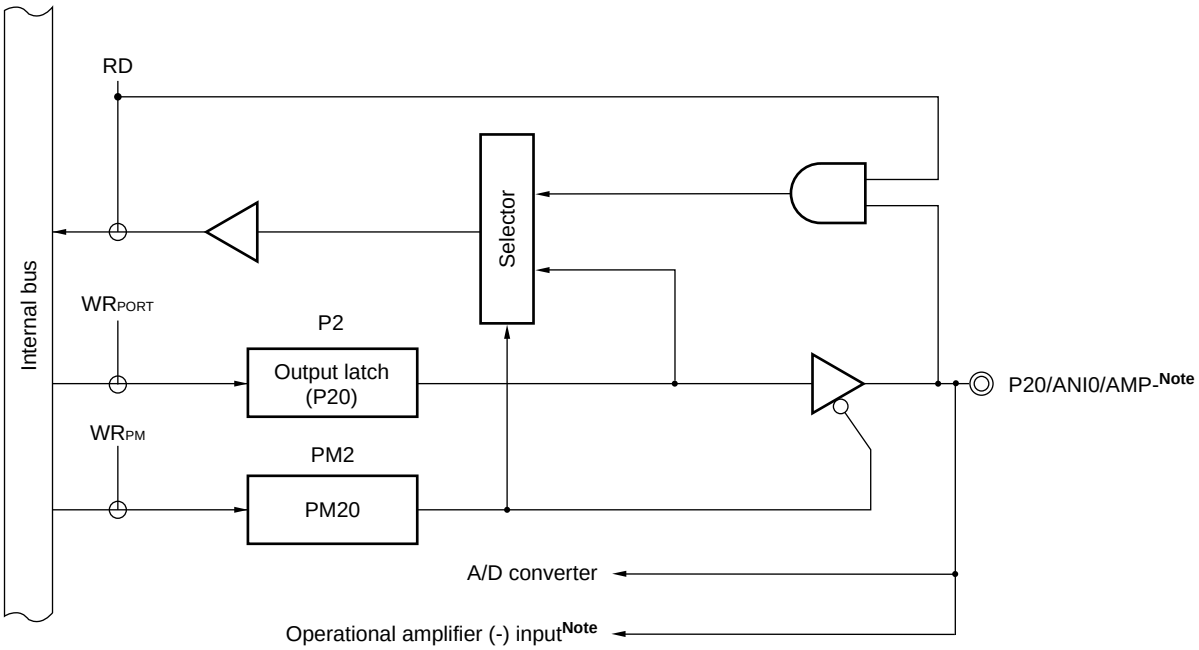
Remark Functions in angle brackets < > can be assigned by setting the input switch control register (MUXSEL).

Figure 4-4. Block Diagram of P20

(1) 78K0/IY2



(2) 78K0/IA2, 78K0/IB2



Note Products with operational amplifier only

P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Figure 4-10. Block Diagram of P26

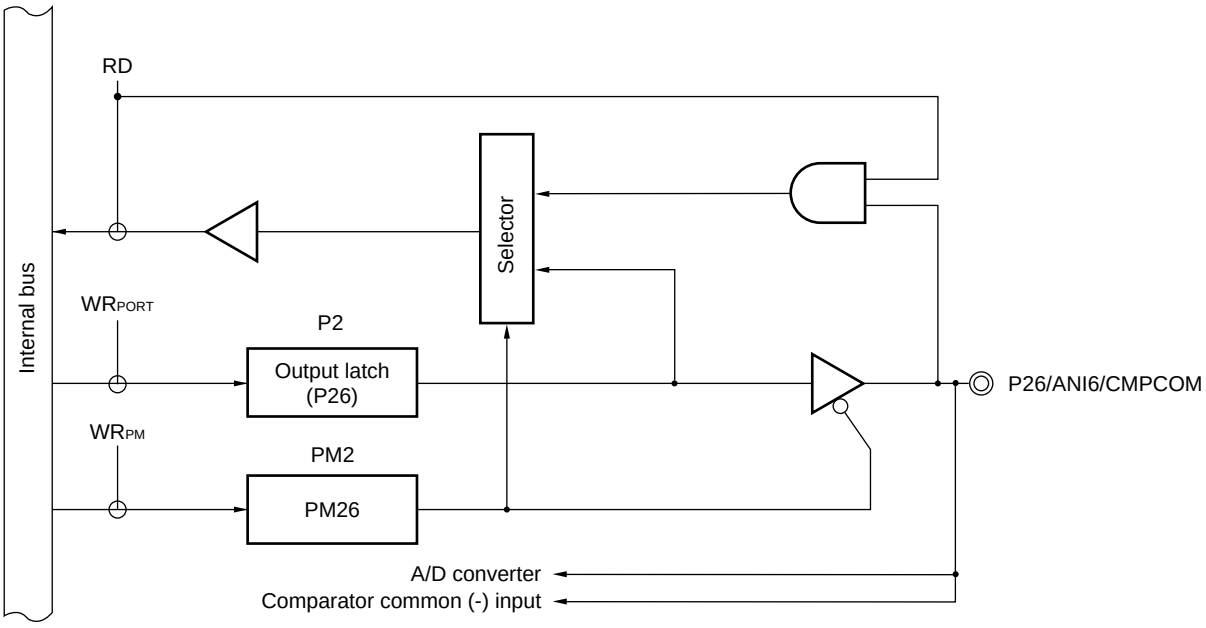
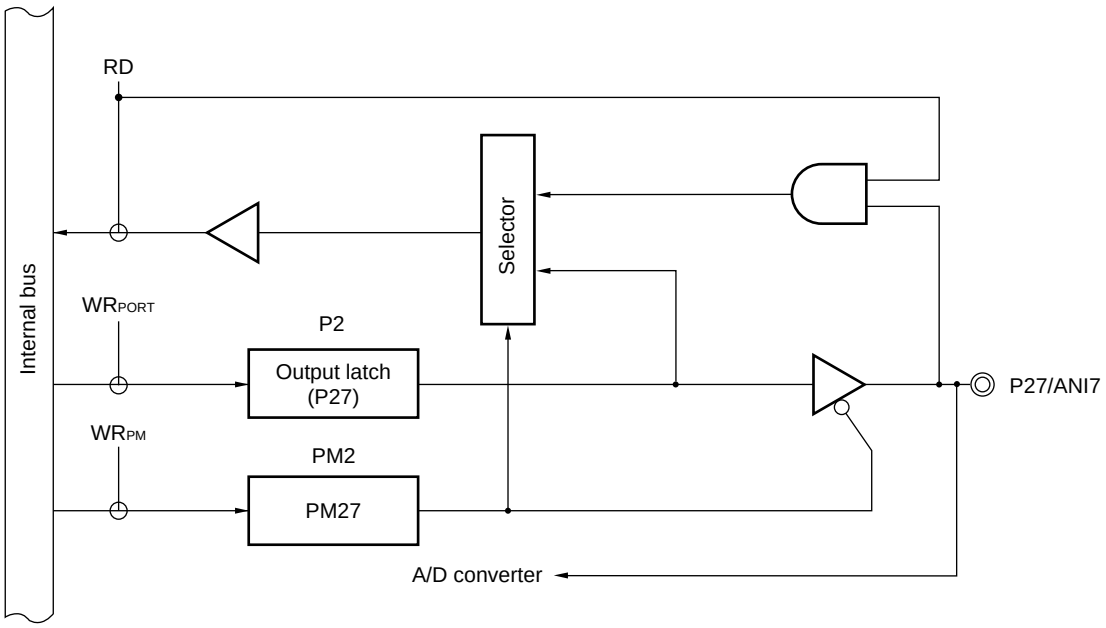


Figure 4-11. Block Diagram of P27



P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Table 6-2. Register Setting Bits Controlling Operation Mode and 16-bit Timers X0 and X1 (2/2)

Register	Bit	Operation mode					
		TMXn-only mode (n = 0, 1)		Synchronous start mode		Synchronous start/clear mode	
		TMX0	TMX1	Master (TMX0)	Slave (TMX1)	Master (TMX0)	Slave (TMX1)
TX0CTL4	TX0CMP1RP	Setting		Setting		–	–
	TX0CMP1RM1, TX0CMP1RM0	Setting is valid when TX0CMP 1RP = 0	–	Setting is valid when TX0CMP 1RP = 0	–	–	–
	TX0CMP0RP	Setting		Setting		–	–
	TX0CMP0RM1, TX0CMP0RM0	Setting is valid when TX0CMP 0RP = 0	–	Setting is valid when TX0CMP 0RP = 0	–	–	–
TX1CTL4	TX1CMP1RM1, TX1CMP1RM0	–	Setting is valid when TX0CMP 1RP = 1	–	Setting is valid when TX0CMP 1RP = 1	–	–
	TX1CMP0RM1, TX1CMP0RM0	–	Setting is valid when TX0CMP 0RP = 1	–	Setting is valid when TX0CMP 0RP = 1	–	–
TX0IOC0	TX0TOC1	Setting	–	Setting	–	Setting	–
	TX0TOC0	Setting	–	Setting	–	Setting	–
	TX0TOL1	Setting	–	Setting	–	Setting	–
	TX0TOL0	Setting	–	Setting	–	Setting	–
TX1IOC0	TX1TOC1	–	Setting	–	Setting	–	Setting
	TX1TOC0	–	Setting	–	Setting	–	Setting
	TX1TOL1	–	Setting	–	Setting	–	Setting
	TX1TOL0	–	Setting	–	Setting	–	Setting

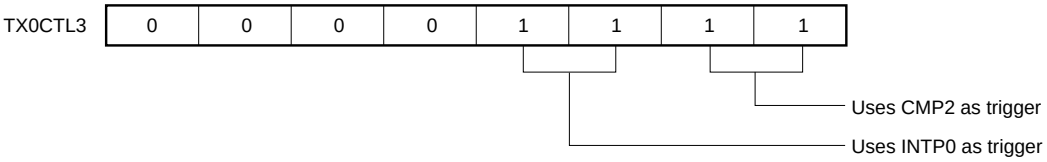
(3) Interlocking mode 3 (timer output reset mode)

This mode sets the output of the corresponding timer to the reset state from when the rising edge of the comparators 0 to 2 outputs or the INTP0 input is detected until the next interrupt is generated.

Caution Do not set to interlocking mode 3 when in TMX0 and TMX1 synchronous start/clear mode.

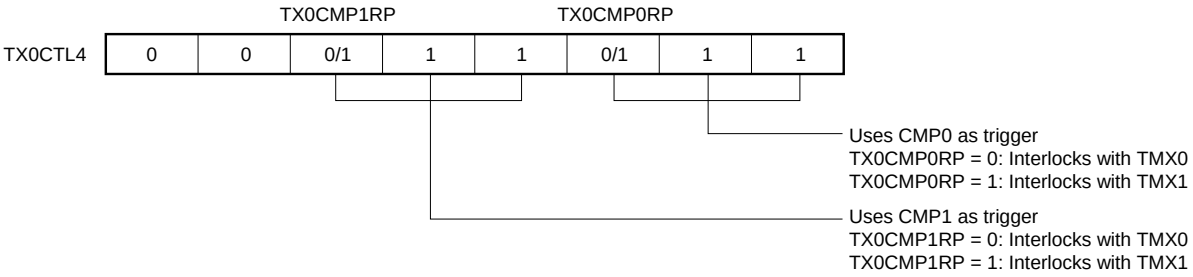
Figure 6-50. Example of Register Settings for Interlocking mode 3 (timer output reset mode)

- Using CMP2 and INTP0 as triggers



Remark When interlocking the timers with either CMP2 or INTP0, set all bits of CMP2 or INTP0, whichever is not used, to 0.

- Using CMP0 and CMP1 as triggers



Remark When interlocking the timers with either CMP0 or CMP1, set all bits of CMP0 or CMP1, whichever is not used, to 0.

(2) UART/DALI operation mode register 6 (ASIM6)

This 8-bit register controls the serial communication operations of serial interface UART6/DALI.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Remark ASIM6 can be refreshed (the same value is written) by software during a communication operation (when bits 7 and 6 (POWER6, TXE6) of ASIM6 = 1 or bits 7 and 5 (POWER6, RXE6) of ASIM6 = 1).

Figure 14-6. Format of UART/DALI Operation Mode Register 6 (ASIM6) (1/2)

Address: FF50H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM6	POWER6	TXE6	RXE6	PS61	PS60	CL6	SL6	ISRM6

POWER6	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].
1	Enables operation of the internal operation clock

TXE6	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).
1	Enables transmission

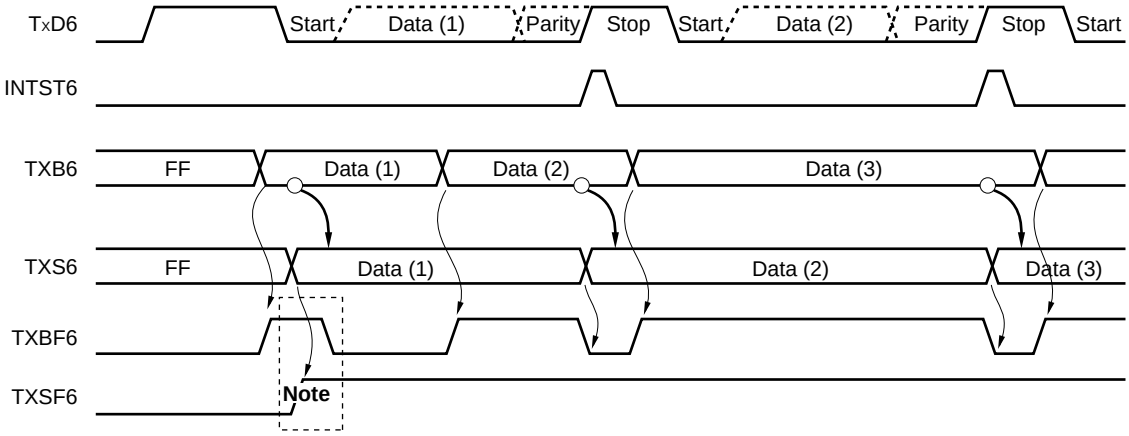
RXE6	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).
1	Enables reception

Notes 1. The output of the TxD6 pin is fixed to the high level (when TXDLV6 = 0) and the input from the RxD6 pin is fixed to the high level when POWER6 = 0 during transmission.

2. UART/DALI reception error status register 6 (ASIS6), UART transmission status register 6 (ASIF6), bit 7 (SBRF6) and bit 6 (SBRT6) of LIN operation control register 6 (ASICL6), UART receive buffer register 6 (RXB6), and DALI receive buffer register (RXBDL) are reset.

Figure 14-19 shows the timing of starting continuous transmission, and Figure 14-20 shows the timing of ending continuous transmission.

Figure 14-19. Timing of Starting Continuous Transmission



Note When ASIF6 is read, there is a period in which TXBF6 and TXSF6 = 1, 1. Therefore, judge whether writing is enabled using only the TXBF6 bit.

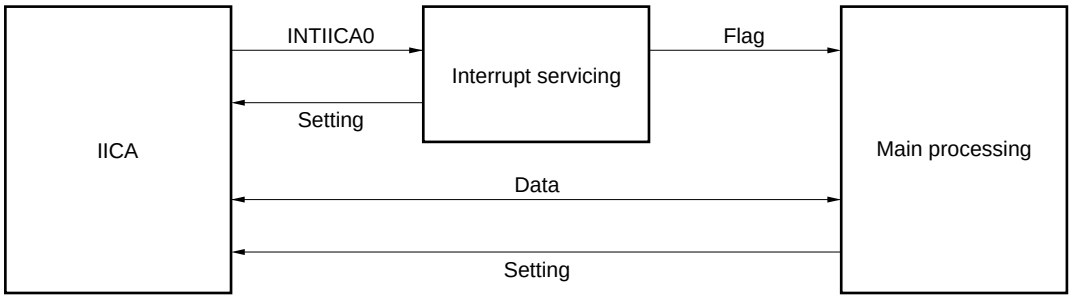
Remark TxD6: TxD6 pin (output)
INTST6: Interrupt request signal
TXB6: UART/DALI transmit buffer register 6
TXS6: Transmit shift register 6
ASIF6: UART transmission status register 6
TXBF6: Bit 1 of ASIF6
TXSF6: Bit 0 of ASIF6

(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA0 interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA0 interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA0.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

<2> Ready flag

This flag indicates that data communication is enabled. Its function is the same as the INTIICA0 interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as the TRC0 bit.

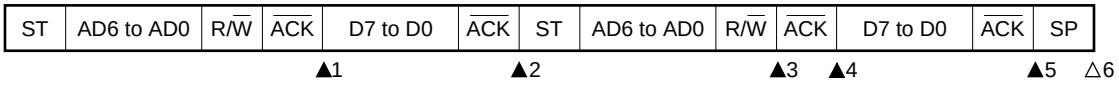
(c) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

(i) When WTIM0 = 0 (after restart, does not match address (= extension code))

▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001×000B
▲3: IICAS0 = 0010×010B
▲4: IICAS0 = 0010×000B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, does not match address (= extension code))



▲1: IICAS0 = 0001×110B
▲2: IICAS0 = 0001××00B
▲3: IICAS0 = 0010×010B
▲4: IICAS0 = 0010×110B
▲5: IICAS0 = 0010××00B
△6: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

18.4.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 18-5 shows relationship between interrupt requests enabled for multiple interrupt servicing and Figure 18-17 shows multiple interrupt servicing examples.

Table 18-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Interrupt Being Serviced \ Multiple Interrupt Request		Maskable Interrupt Request				Software Interrupt Request
		PR = 0		PR = 1		
		IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP = 0	○	×	×	×	○
	ISP = 1	○	×	○	×	○
Software interrupt		○	×	○	×	○

Remarks 1. ○: Multiple interrupt servicing enabled

2. ×: Multiple interrupt servicing disabled

3. ISP and IE are flags contained in the PSW.

ISP = 0: An interrupt with higher priority is being serviced.

ISP = 1: No interrupt request has been acknowledged, or an interrupt with a lower priority is being serviced.

IE = 0: Interrupt request acknowledgment is disabled.

IE = 1: Interrupt request acknowledgment is enabled.

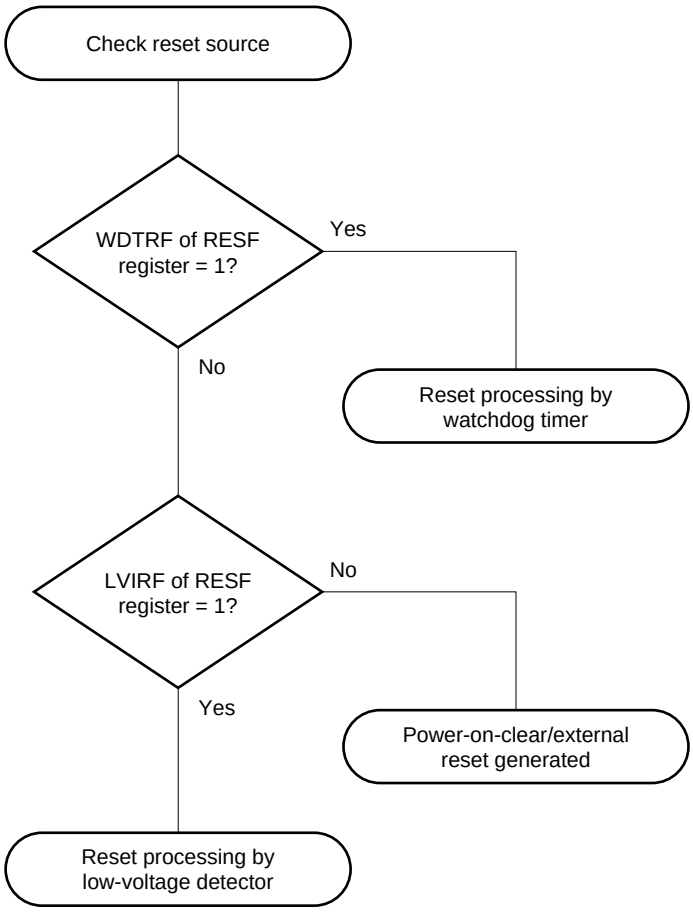
4. PR is a flag contained in PR0L, PR0H, PR1L, and PR1H.

PR = 0: Higher priority level

PR = 1: Lower priority level

Figure 22-8. Example of Software Processing After Reset Release (2/2)

• Checking reset source



Operation example 2: When used as interrupt

Interrupt requests may be generated frequently.

Take the following action.

<Action>

Confirm that "supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < LVI detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, in the servicing routine of the LVI interrupt by using bit 0 (LVIF) of the low-voltage detection register (LVIM). Clear bit 1 (LVIIF) of interrupt request flag register 0L (IF0L) to 0.

For a system with a long supply voltage fluctuation period near the LVI detection voltage, take the above action after waiting for the supply voltage fluctuation time.

Here is an example of description of the software for setting the option bytes.

```
OPT      CSEG   AT 0080H
OPTION:  DB     30H      ; Enables watchdog timer operation (illegal access detection operation),
                         ; Window open period of watchdog timer: 50%,
                         ; Overflow time of watchdog timer: 2^7/fIL,
                         ; Internal low-speed oscillator can be stopped by software.
         DB     00H      ; LVI default start function stopped
         DB     01H      ; Internal high-speed oscillation clock frequency 4 MHz (TYP.)
         DB     1EH      ; Use the TOOLC0/X1, TOOLD0/X2 pins
         DB     02H      ; Operation enabled.  Does not erase data of the flash memory in case
                         ; authentication of the on-chip debug security ID fails.
```

Remark Referencing of the option byte is performed during reset processing. For the reset processing timing, refer to **CHAPTER 20 RESET FUNCTION**.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit operation	**SUB**	A, #byte	2	4	–	A, CY ← A – byte	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte	× × ×
		A, r Note 3	2	4	–	A, CY ← A – r	× × ×
		r, A	2	4	–	r, CY ← r – A	× × ×
		A, saddr	2	4	5	A, CY ← A – (saddr)	× × ×
		A, !addr16	3	8	9	A, CY ← A – (addr16)	× × ×
		A, [HL]	1	4	5	A, CY ← A – (HL)	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B)	× × ×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C)	× × ×
	SUBC	A, #byte	2	4	–	A, CY ← A – byte – CY	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte – CY	× × ×
		A, r Note 3	2	4	–	A, CY ← A – r – CY	× × ×
		r, A	2	4	–	r, CY ← r – A – CY	× × ×
		A, saddr	2	4	5	A, CY ← A – (saddr) – CY	× × ×
		A, !addr16	3	8	9	A, CY ← A – (addr16) – CY	× × ×
		A, [HL]	1	4	5	A, CY ← A – (HL) – CY	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte) – CY	× × ×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B) – CY	× × ×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C) – CY	× × ×
	AND	A, #byte	2	4	–	A ← A ∧ byte	×
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∧ byte	×
		A, r Note 3	2	4	–	A ← A ∧ r	×
		r, A	2	4	–	r ← r ∧ A	×
		A, saddr	2	4	5	A ← A ∧ (saddr)	×
		A, !addr16	3	8	9	A ← A ∧ (addr16)	×
		A, [HL]	1	4	5	A ← A ∧ (HL)	×
		A, [HL + byte]	2	8	9	A ← A ∧ (HL + byte)	×
		A, [HL + B]	2	8	9	A ← A ∧ (HL + B)	×
		A, [HL + C]	2	8	9	A ← A ∧ (HL + C)	×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.