Renesas Electronics America Inc - UPD78F0746MC-CAB-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, DALI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0746mc-cab-ax

CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

There are two types of pin I/O buffer power supplies: AV_{REF} and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 4-1. Pin I/O Buffer Power Supplies

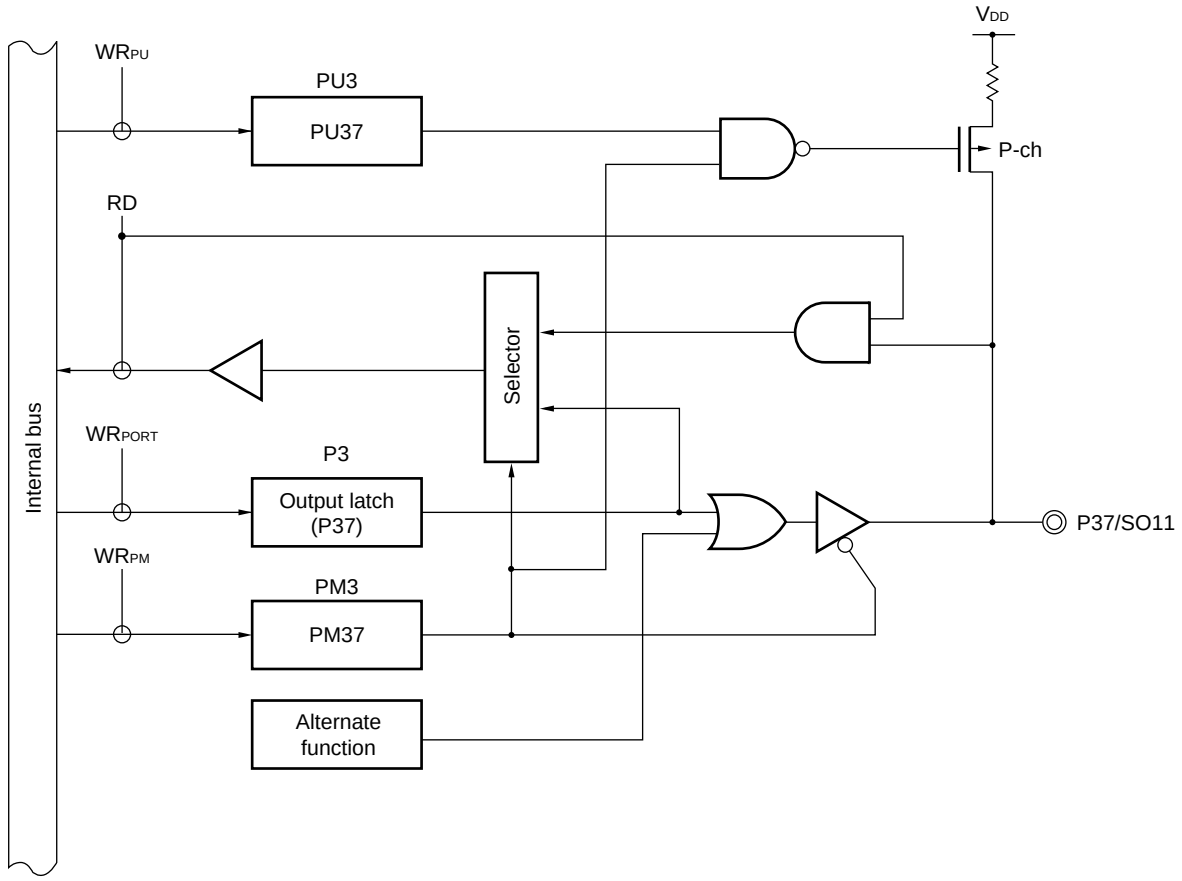
Power Supply	Corresponding Pins
AV_{REF}	P20 to P27, P70[Note]
V_{DD}	Pins other than P20 to P27, P70 [Note]

Note 78K0/IY2: P20, P21, P23 to P25
78K0/IA2: P20 to P25
78K0/IB2: P20 to P27, P70

78K0/Ix2 microcontrollers are provided with digital I/O ports, which enable variety of control operations. The functions of each port are shown in Tables 4-2 to 4-5.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, refer to **CHAPTER 2 PIN FUNCTIONS**.

Figure 4-19. Block Diagram of P37



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

CHAPTER 6 16-BIT TIMERS X0 AND X1

6.1 Functions of 16-Bit Timers X0 and X1

16-bit timers X0 and X1 are mounted onto all 78K0/Ix2 microcontroller products.

16-bit timers X0 and X1 are dedicated PWM output timers and have two outputs each, enabling the generation of up to four PWM outputs. Complementary PWM output can also be generated to control a half-bridge circuit (2 outputs) or full-bridge circuit (4 outputs). Also, by linking with a comparator or INTP0, PFC control and PWM output can be stopped urgently.

16-bit timers X0 and X1 are provided with the following functions.

(1) PWM output

- A variable pulse with any duty or cycle can be output while the timer is operating.
- The default timer output level (high or low level) can be set.

(2) A/D conversion start timing signal output

The A/D conversion start timing signal can be output by using a compare register (TXnCCR0 register: n = 0, 1).

(3) Capture function

This function captures the count value to the capture register by detecting a comparator output or an external interrupt input (INTP0).

(4) Timer start synchronization function

Up to 4 PWM outputs can be simultaneously started by combining two timer units (16-bit timers X0 and X1).

(5) Timer start/clear synchronization function

Up to 4 PWM output cycles can be synchronized by combining two timer units (16-bit timers X0 and X1).

(6) Timer output gating function (by interlocking with 8-bit timer H1)

Timer output can be gate-controlled by using the output of 8-bit timer H1 (the TOH1 output).

(7) Timer reset mode (comparator, INTP0 interlocking mode 1)

Timer output can be reset and the timer counter cleared while the comparator 0 to 2 outputs or the INTP0 input is high level. When the comparator 0 to 2 outputs or the INTP0 input go to low level, timer output restarts.

(8) Timer restart mode (comparator, INTP0 interlocking mode 2)

Timer can be restarted upon detection of the rising edge of the comparator 0 to 2 outputs or the INTP0 input.

(9) Timer output reset mode (comparator, INTP0 interlocking mode 3)

Timer output can be reset upon detection of the rising edge of the comparator 0 to 2 outputs or the INTP0 input. The reset status is cleared when the next timer interrupt occurs and timer output restarts.

(10) High-impedance output control function (by interlocking with comparator and INTP0)

Timer output can be made high impedance upon detection of the valid edge of the comparator 0 to 2 outputs or the INTP0 input.

Cautions 2. Be sure to clear bits 0 to 2, 6 to 0.

3. When using the output gate function, set bit 0 (TOEN1) of the TMHMD1 register to 1 (enable the TOH1 output).

Figure 6-9. Format of 16-Bit Timer X1 Operation Control Register 1 (TX1CTL1)

Address: FF95H After reset: 00H R/W

Symbol	7	6	<5>	4	<3>	2	<1>	<0>
TX1CTL1	0	0	TX1PWM CE	0	TX1PWM	0	TX1MD1	TX1MD0

TX1PWM CE	Control of TOX1n output gate function by TOH1 output (n = 0, 1)
0	Does not use output gate function.
1	Use output gate function.

TX1PWM	TMX1 PWM output operation setting
0	• Single output (TOX10 pin only) • INTTMX1 is generated upon match of counter and TX1CR1 register
1	• Dual output (TOX10 and TOX11 pins) • INTTMX1 is generated upon match of counter and TX1CR3 register

TX1MD1	TX1MD0	Operation mode setting
0	0	TMX1-only start mode
0	1	TMX0 and TMX1 Synchronous start mode
1	0	TMX0 and TMX1 Synchronous start/clear mode
1	1	Setting prohibited

Cautions 1. During the timer operation, setting the other bits of TX1CTL1 is prohibited. However, TX1CTL1 can be refreshed (the same value is written).

2. Be sure to clear bits 2, 4, 6 and 7 to 0.

3. When using the output gate function, set bit 0 (TOEN1) of the TMHMD1 register to 1 (enable the TOH1 output).

(3) 16-bit timer Xn operation control register 2 (TXnCTL2)

TXnCTL2 is a register that selects the capture trigger source, controls the generation of the A/D conversion synchronization trigger, and sets the TXnCCR0 register.

TXnCTL2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TXnCTL2 to 00H.

(2) A/D conversion start timing signal output

If bit 1 (TXnADEN) of the 16-bit timer Xn operation control register 2 (TXnCTL2) is set to 1, the generation of the A/D conversion synchronization trigger is enabled. If bit 7 (TXnTMC) of the 16-bit timer Xn operation control register 0 (TXnCTL0) is set to 1, the count operation is started in synchronization with the count clock.

When the value of the 16-bit timer counter Xn (TMXn) later matches the value of TXnCCR0, the A/D conversion synchronization trigger is generated. When the value of TMXn matches the value of TXnCRm, TMXn is cleared to 0000H.

To output the A/D conversion start timing signal, satisfy the relationship between TXnCCR0 and TXnCRm as follows.

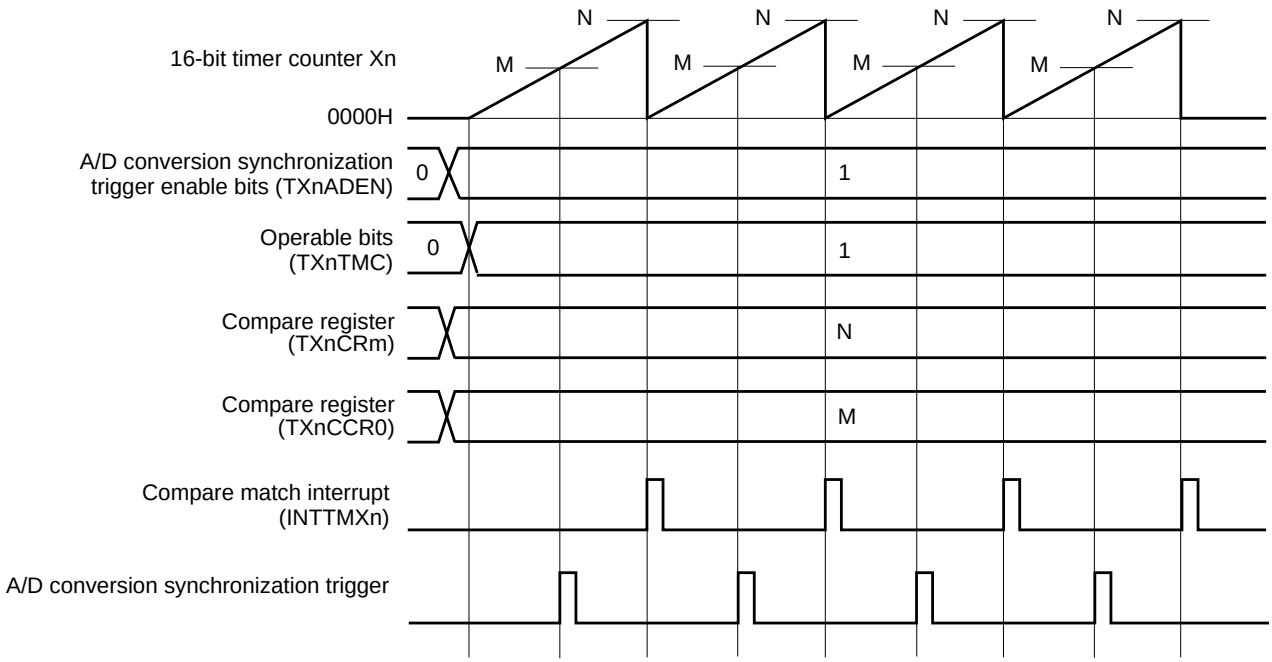
- TXnCCR0 < TXnCRm

If this relationship is not satisfied, the A/D conversion trigger is not generated.

Remarks 1. For details of the A/D conversion in combination with 16 bit timer X0 or X1, refer to **11.4.2 Basic operation of A/D converter (timer trigger mode)**.

2. m = 1, 3
n = 0, 1

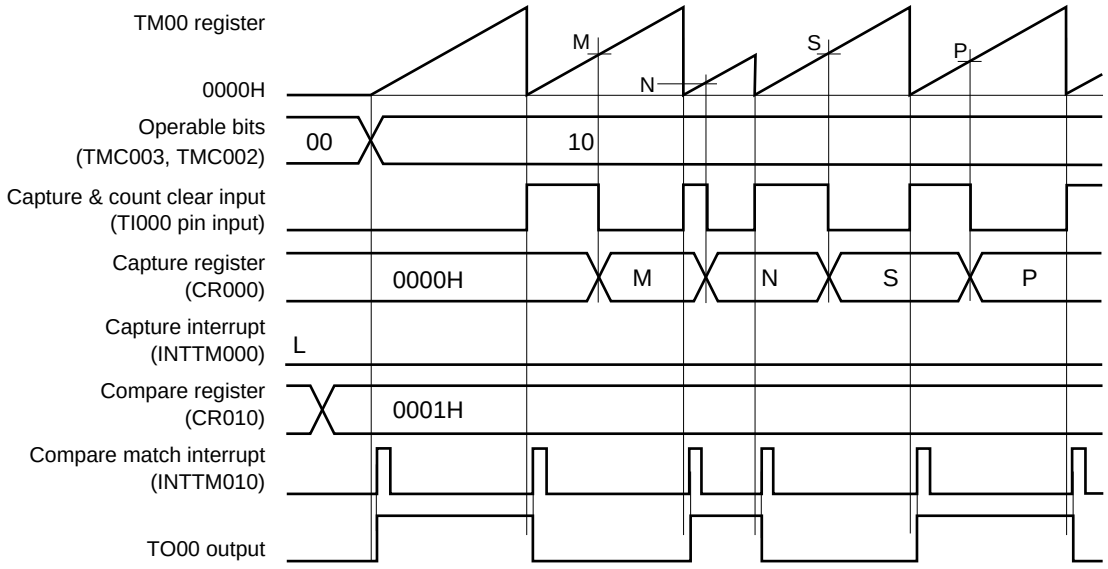
Figure 6-21. Basic Timing Example of A/D Conversion Start Timing Signal Output



Remark m = 1, 3
n = 0, 1

Figure 7-28. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00 = 03H, TMC00 = 08H, CR010 = 0001H



This is an application example where the TO00 output level is to be inverted when the count value has been captured & cleared.

TM00 is cleared at the rising edge detection of the TI000 pin and it is captured to CR000 at the falling edge detection of the TI000 pin.

When bit 1 (CRC001) of capture/compare control register 00 (CRC00) is set to 1, the count value of TM00 is captured to CR000 in the phase reverse to that of the signal input to the TI000 pin, but the capture interrupt signal (INTTM000) is not generated. However, the INTTM000 signal is generated when the valid edge of the TI010 pin is detected. Mask the INTTM000 signal when it is not used.

11.4 Operation of A/D Converter

11.4.1 Basic operation of A/D converter (software trigger mode)

<1> Set the A/D conversion time and the operation mode by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of the A/D converter mode register 0 (ADM0).

<2> Set bit 0 (ADCE) of ADM0 to 1 to start the operation of the A/D voltage comparator.

<3> Set channels for A/D conversion to analog input by using the A/D port configuration registers 0 and 1 (ADPC0, ADPC1) and set to input mode by using port mode registers 2 and 7 (PM2, PM7).

<4> Set the PGA operation to set the PGA output and the single Amp operation to set the operational amplifier output for analog input. (refer to **CHAPTER 12 OPERATIONAL AMPLIFIER**).

<5> Select one channel for A/D conversion by using the analog input channel specification register (ADS).

<6> Start the conversion operation by setting bit 7 (ADCS) of ADM0 to 1.
(<7> to <14> are operations performed by hardware.)

<7> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<8> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<9> Bit 9 of the successive approximation register (SAR) is set. The comparison voltage generator outputs (1/2) AV_{REF} voltage.

<10> The voltage difference between the output voltage of the comparison voltage generator and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB of SAR remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB is reset to 0.

<11> Next, bit 8 of SAR is automatically set to 1, and the operation proceeds to the next comparison. The output voltage of the comparison voltage generator is selected according to the preset value of bit 9, as described below.

- Bit 9 = 1: (3/4) AV_{REF}
- Bit 9 = 0: (1/4) AV_{REF}

The output voltage of the comparison voltage generator and sampled voltage are compared and bit 8 of SAR is manipulated as follows.

- Analog input voltage ≥ Output voltage of comparison voltage generator: Bit 8 = 1
- Analog input voltage < Output voltage of comparison voltage generator: Bit 8 = 0

<12> Comparison is continued in this way up to bit 0 of SAR.

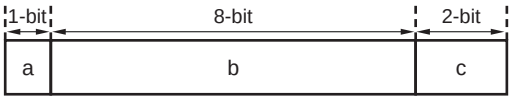
<13> Upon completion of the comparison of 10 bits, an effective digital result value remains in SAR, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH, ADCRL) and then latched.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.

<14> Repeat steps <7> to <13>, until ADCS is cleared to 0.
To stop the A/D converter, clear ADCS to 0.
To restart A/D conversion from the status of ADCE = 1, start from <6>. To start A/D conversion again when ADCE = 0, set ADCE to 1, wait for 1 μs or longer, and start <6>. To change a channel of A/D conversion, start from <5>.

- Backward frame

  This is a frame used when transmitting from the slave to a master. A frame consists of 11 bits.

Figure 14-28. Backward-Frame Structure



a: Start bit

This indicates the start of the frame. It is always the same waveform as “1”.

b: Data byte

This replies to the master.

c: Stop bit

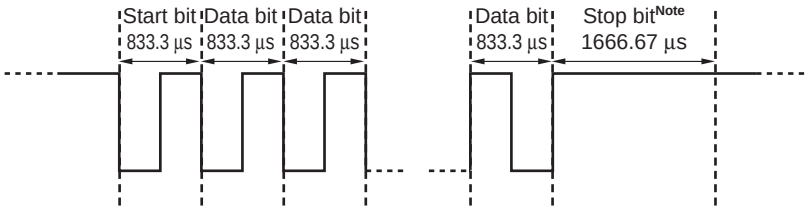
This indicates the end of the frame. It is fixed to the high level.

(2) Transmission/reception timing rules

<1> Timing in the frame

The DALI bit width is one bit (= 833.3 μs ±10%) for both Forward and Backward frames.

Figure 14-29. Timing in the Frame



Note The stop bit width is 1666.67 μs for 2 stop bits.

<2> Timing among frames

With DALI, the following timing must be controlled in frame units.

- Forward frame width: 15.83 ms ±10%
- Backward frame width: 9.17 ms ±10%
- Communication interval between one Forward frame and the Backward frame: 2.92 to 9.17 ms
- Communication interval between one Forward frame and the next Forward frame: 9.17 ms min.
- Communication interval between one Backward frame and the next Forward frame: 9.17 ms min.

Figure 14-30. Timing among frames

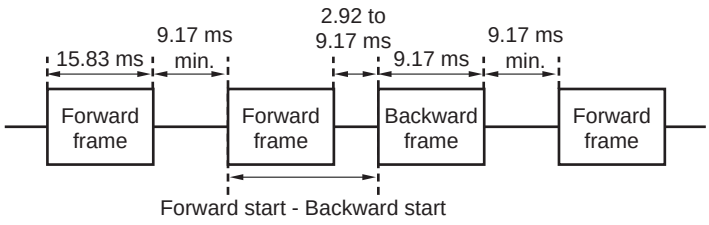


Figure 15-4. Format of Slave Address Register 0 (SVA0)

Address: FFA6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SVA0								0Note

Note Bit 0 is fixed to 0.

(3) SO latch

The SO latch is used to retain the SDAA0 pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request (INTIICA0) when the address received by this register matches the address value set to the slave address register 0 (SVA0) or when an extension code is received.

(5) Serial clock counter

This counter counts the serial clocks that are output or input during transmit/receive operations and is used to verify that 8-bit data was transmitted or received.

(6) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIICA0).

An I^2C interrupt request is generated by the following two triggers.

- Falling edge of eighth or ninth clock of the serial clock (set by WTIM0 bit)
- Interrupt request generated when a stop condition is detected (set by SPIE0 bit)

Remark WTIM0 bit: Bit 3 of IICA control register 0 (IICACTL0)
SPIE0 bit: Bit 4 of IICA control register 0 (IICACTL0)

(7) Serial clock controller

In master mode, this circuit generates the clock output via the SCLA0 pin from a sampling clock.

(8) Serial clock wait controller

This circuit controls the wait timing.

(9) ACK generator, stop condition detector, start condition detector, and ACK detector

These circuits generate and detect each status.

(10) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(11) Start condition generator

This circuit generates a start condition when the STT0 bit is set to 1.

However, in the communication reservation disabled status (IICRSV bit = 1), when the bus is not released (IICBSY bit = 1), start condition requests are ignored and the STCF bit is set to 1.

(12) Stop condition generator

This circuit generates a stop condition when the SPT0 bit is set to 1.

15.5.8 Interrupt request (INTIICA0) generation timing and wait control

The setting of bit 3 (WTIM0) of IICA control register 0 (IICACTL0) determines the timing by which INTIICA0 is generated and the corresponding wait control, as shown in Table 15-2.

Table 15-2. INTIICA0 Generation Timing and Wait Control

WTIM0	During Slave Device Operation			During Master Device Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 Notes 1, 2	8 Note 2	8 Note 2	9	8	8
1	9 Notes 1, 2	9 Note 2	9 Note 2	9	9	9

Notes 1. The slave device's INTIICA0 signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to the slave address register 0 (SVA0).
At this point, $\overline{ACK}$ is generated regardless of the value set to bit 2 (ACKE0) of the IICACTL0 register. For a slave device that has received an extension code, INTIICA0 occurs at the falling edge of the eighth clock.
However, if the address does not match after restart, INTIICA0 is generated at the falling edge of the 9th clock, but wait does not occur.

2. If the received address does not match the contents of the slave address register 0 (SVA0) and extension code is not received, neither INTIICA0 nor a wait occurs.

Remark The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

(1) During address transmission/reception

- Slave device operation: Interrupt and wait timing are determined depending on the conditions described in Notes 1 and 2 above, regardless of the WTIM0 bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIM0 bit.

(2) During data reception

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(3) During data transmission

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIM0 bit.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

- Writing data to IICA shift register (IICA)
- Setting bit 5 (WREL0) of IICA control register 0 (IICACTL0) (canceling wait)
- Setting bit 1 (STT0) of IICACTL0 register (generating start condition)Note
- Setting bit 0 (SPT0) of IICACTL0 register (generating stop condition)Note

Note Master only.

When an 8-clock wait has been selected (WTIM0 = 0), the presence/absence of $\overline{ACK}$ generation must be determined prior to wait cancellation.

(5) Stop condition detection

INTIICA0 is generated when a stop condition is detected (only when SPIE0 = 1).

15.5.9 Address match detection method

In I^2C bus mode, the master device can select a particular slave device by transmitting the corresponding slave address.

Address match can be detected automatically by hardware. An interrupt request (INTIICA0) occurs when a local address has been set to the slave address register 0 (SVA0) and when the address set to the SVA0 register matches the slave address sent by the master device, or when an extension code has been received.

15.5.10 Error detection

In I^2C bus mode, the status of the serial data bus (SDAA0) during data transmission is captured by the IICA shift register (IICA) of the transmitting device, so the IICA data prior to transmission can be compared with the transmitted IICA data to enable detection of transmission errors. A transmission error is judged as having occurred when the compared data values do not match.

15.5.11 Extension code

(1) When the higher 4 bits of the receive address are either “0000” or “1111”, the extension code reception flag (EXC0) is set to 1 for extension code reception and an interrupt request (INTIICA0) is issued at the falling edge of the eighth clock. The local address stored in the slave address register 0 (SVA0) is not affected.

(2) If “11110××0” is set to the SVA0 register by a 10-bit address transfer and “11110××0” is transferred from the master device, the results are as follows. Note that INTIICA0 occurs at the falling edge of the eighth clock.

- Higher four bits of data match: EXC0 = 1
- Seven bits of data match: COI0 = 1

Remark EXC0: Bit 5 of IICA status register 0 (IICAS0)
COI0: Bit 4 of IICA status register 0 (IICAS0)

(3) Since the processing after the interrupt request occurs differs according to the data that follows the extension code, such processing is performed by software.
If the extension code is received while a slave device is operating, then the slave device is participating in communication even if its address does not match.
For example, after the extension code is received, if you do not wish to operate the target device as a slave device, set bit 6 (LREL0) of the IICA control register 0 (IICACTL0) to 1 to set the standby mode for the next communication operation.

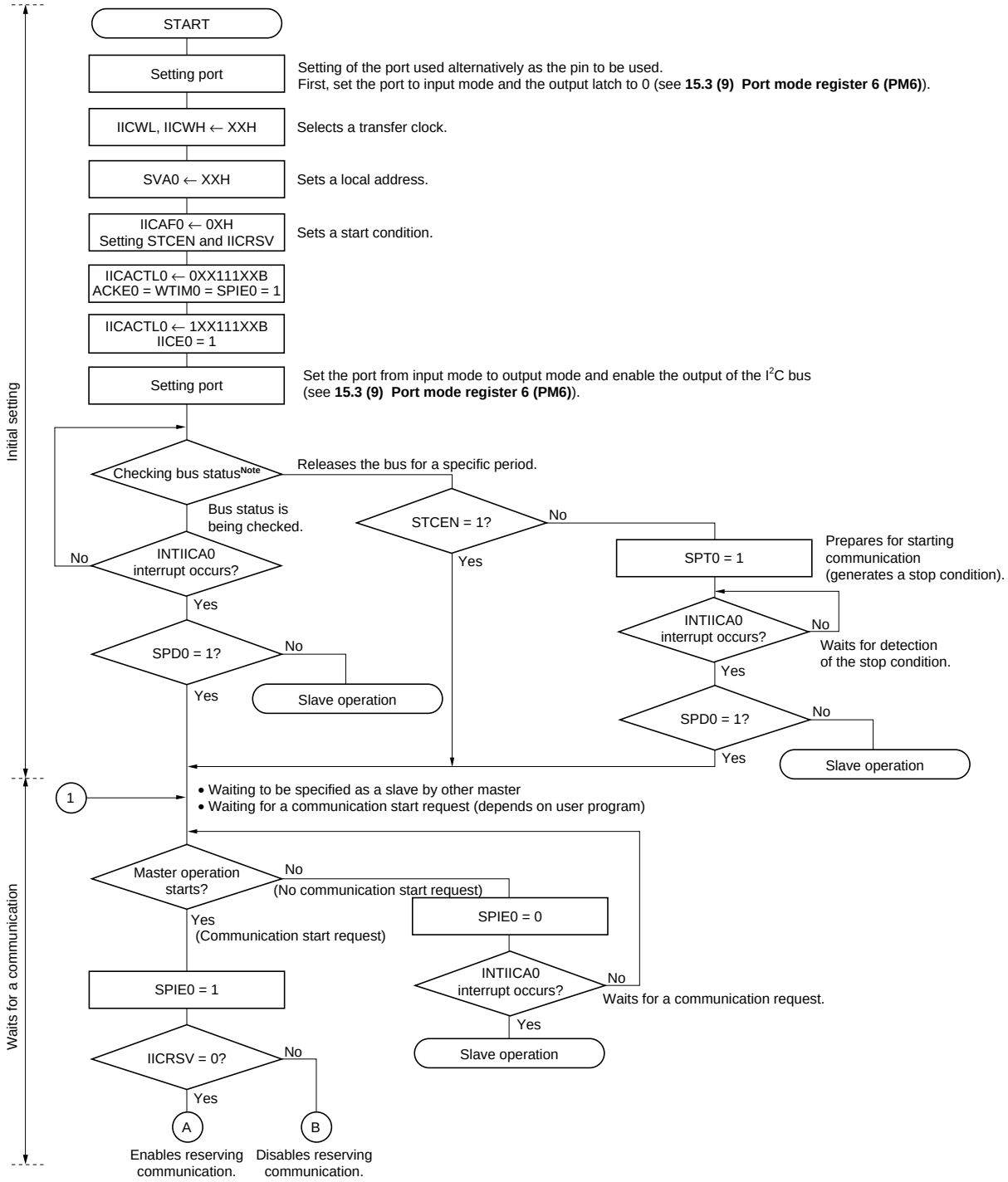
Table 15-3. Bit Definitions of Main Extension Code

Slave Address	R/W Bit	Description
0 0 0 0 0 0 0	0	General call address
1 1 1 1 0 x x	0	10-bit slave address specification (for address authentication)
1 1 1 1 0 x x	1	10-bit slave address specification (for read command issuance after address match)

Remark For extension codes other than the above, refer to THE I^2C-BUS SPECIFICATION published by NXP.

(2) Master operation in multi-master system

Figure 15-30. Master Operation in Multi-Master System (1/3)



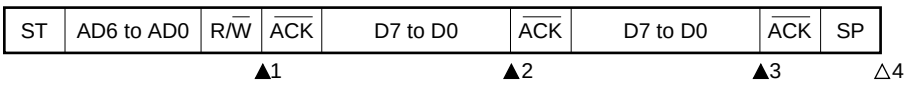
Note Confirm that the bus is released (CLD0 bit = 1, DAD0 bit = 1) for a specific period (for example, for a period of one frame). If the SDAA0 pin is constantly at low level, decide whether to release the I^2C bus (SCLA0 and SDAA0 pins = high level) in conformance with the specifications of the product that is communicating.

(3) Slave device operation (when receiving extension code)

The device is always participating in communication when it receives an extension code.

(a) Start ~ Code ~ Data ~ Data ~ Stop

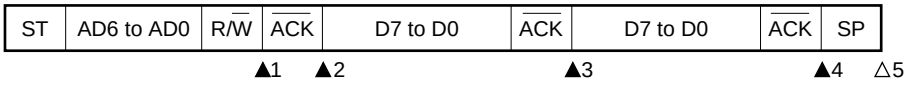
(i) When WTIM0 = 0



▲1: IICAS0 = 0010×010B
▲2: IICAS0 = 0010×000B
▲3: IICAS0 = 0010×000B
△4: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1



▲1: IICAS0 = 0010×010B
▲2: IICAS0 = 0010×110B
▲3: IICAS0 = 0010×100B
▲4: IICAS0 = 0010××00B
△5: IICAS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Table 25-1. Set Values of Internal Memory Size Switching Register

Products			IMS Setting
78K0/IY2	78K0/IA2	78K0/IB2	
μPD78F0740, 78F0750	–	–	61H
μPD78F0741, 78F0751	μPD78F0743, 78F0753	μPD78F0745, 78F0755	42H
μPD78F0742, 78F0752	μPD78F0744, 78F0754	μPD78F0746, 78F0756	04H

25.2 Writing with Flash Memory Programmer

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the 78K0/Ix2 microcontrollers have been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the 78K0/Ix2 microcontrollers are mounted on the target system.

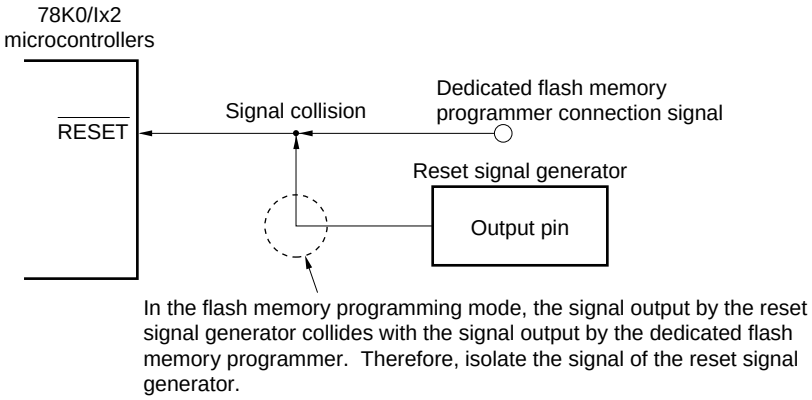
Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

25.4.2 $\overline{\text{RESET}}$ pin

If the reset signal of the dedicated flash memory programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board, signal collision takes place. To prevent this collision, isolate the connection with the reset signal generator.

If the reset signal is input from the user system while the flash memory programming mode is set, the flash memory will not be correctly programmed. Do not input any signal other than the reset signal of the dedicated flash memory programmer.

Figure 25-4. Signal Collision ($\overline{\text{RESET}}$ Pin)



25.4.3 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to V_{DD} or V_{SS} via a resistor.

25.4.4 REGC pin

Connect the REGC pin to V_{DD} via a capacitor (0.47 to 1 μF) in the same manner as during normal operation. However, when using the STOP mode that has been entered since operation of the internal high-speed oscillation clock and external main system clock, 0.47 μF is recommended. Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

25.4.5 Other signal pins

Connect X1 and X2 in the same status as in the normal operation mode.

Remark In the flash memory programming mode, the internal high-speed oscillation clock (f_{IH}) is used.

25.4.6 Power supply

To use the supply voltage output of the flash memory programmer, connect the V_{DD} pin to V_{DD} of the flash memory programmer, and the V_{SS} pin to GND of the flash memory programmer.

To use the on-board supply voltage, connect in compliance with the normal operation mode.

However, be sure to connect the V_{DD} and V_{SS} pins to V_{DD} and GND of the flash memory programmer to use the power monitor function with the flash memory programmer, even when using the on-board supply voltage.

Supply the same other power supplies (AV_{REF} and AV_{SS}) as those in the normal operation mode.

25.7 Processing Time for Each Command When PG-FP5 Is Used (Reference)

The following table shows the processing time for each command (reference) when the PG-FP5 is used as a dedicated flash memory programmer.

Table 25-9. Processing Time for Each Command When PG-FP5 Is Used (Reference) (1/2)

(1) Products with internal ROMs of the 4 KB: μPD78F0740, 78F0750

Command of PG-FP5	Port: UART-Internal-OSC (Internal high-speed oscillation clock (f_{IH}: 8 MHz (typ.)), Speed: 500,000 bps
Signature	0.5 s (typ.)
Blankcheck	0.5 s (typ.)
Erase	0.5 s (typ.)
Program	1 s (typ.)
Verify	1 s (typ.)
E.P.V	1 s (typ.)
Checksum	0.5 s (typ.)
Security	0.5 s (typ.)

(2) Products with internal ROMs of the 8 KB: μPD78F0741, 78F0743, 78F0745, 78F0751, 78F0753, 78F0755

Command of PG-FP5	Port: UART-Internal-OSC (Internal high-speed oscillation clock (f_{IH}: 8 MHz (typ.)), Speed: 500,000 bps
Signature	0.5 s (typ.)
Blankcheck	0.5 s (typ.)
Erase	1 s (typ.)
Program	1.5 s (typ.)
Verify	1 s (typ.)
E.P.V	1.5 s (typ.)
Checksum	0.5 s (typ.)
Security	0.5 s (typ.)

Caution When executing boot swapping, do not use the E.P.V. command with the dedicated flash memory programmer.

27.1.2 Description of operation column

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
RBS: Register bank select flag
IE: Interrupt request enable flag
( ): Memory contents indicated by address or register contents in parentheses
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
∧: Logical product (AND)
∨: Logical sum (OR)
$\veebar$: Exclusive logical sum (exclusive OR)
$\overline{\ \ }$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

27.1.3 Description of flag operation column

(Blank): Not affected
0: Cleared to 0
1: Set to 1
×: Set/cleared according to the result
R: Previously saved value is restored

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

28.3 DC Characteristics

28.3.1 Pin Characteristics

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P02, P30 to P37, P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–2.5	mA
		Total of P00 to P02	4.0 V ≤ V_{DD} ≤ 5.5 V			–4.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			–4	mA
		Total of P30 to P37, P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			–10	mA
			2.7 V ≤ V_{DD} < 4.0 V			–8	mA
		Total of P00 to P02, P30 to P37, P60, P61[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			–14.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			–12	mA
	I_{OH2}	Per pin for P20 to P27, P70	AV_{REF} = V_{DD}			–0.1	mA
Output current, low[Note 2]	I_{OL1}	Per pin for P00 to P02, P30 to P37	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
		Per pin for P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
		Total of P00 to P02	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			10.0	mA
		Total of P30 to P37, P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V			30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
		Total of P00 to P02, P30 to P37, P60, P61[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			45.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			25.0	mA
	I_{OL2}	Per pin for P20 to P27, P70	AV_{REF} = V_{DD}			0.4	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} to an output pin.

2. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

3. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of I_{OH} is n%: Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where the duty factor is 50%, I_{OH} = –12 mA

Total output current of pins = (–12 × 0.7)/(50 × 0.01) = –16.8 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

A.1 Software Package

SP78K0 78K0 microcontroller software package	Development tools (software) common to the 78K0 microcontrollers are combined in this package.

A.2 Language Processing Software

RA78K0[Note 1] Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (DF780756). **<Precaution when using RA78K0 in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
CC78K0[Note 1] C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file. **<Precaution when using CC78K0 in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
DF780756[Note 2] Device file	This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0, CC78K0, ID78K0-QB, and SM+ for 78K0). The corresponding OS and host machine differ depending on the tool to be used.

Notes 1. If the versions of RA78K0 and CC78K0 are Ver.4.00 or later, different versions of RA78K0 and CC78K0 can be installed on the same machine.

2. The DF780756 can be used in common with the RA78K0, CC78K0, ID78K0-QB, and SM+ for 78K0. Download the DF780588 from the download site for development tools

<R> (https://secure-resource.renesas.com/micro/tool_reg/OdsListTop.do?lang=en).