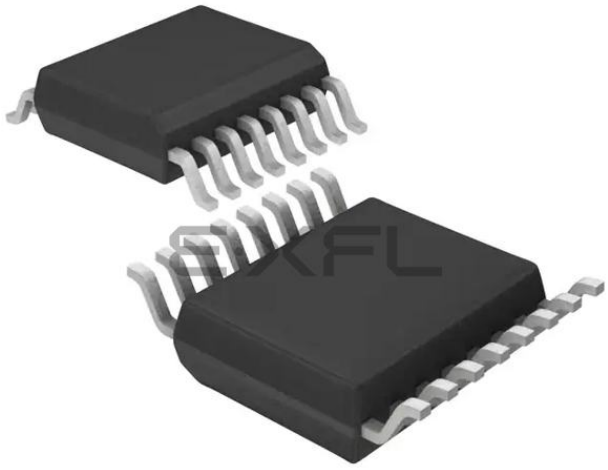
Renesas Electronics America Inc - UPD78F0752MA-FAA-AX Datasheet



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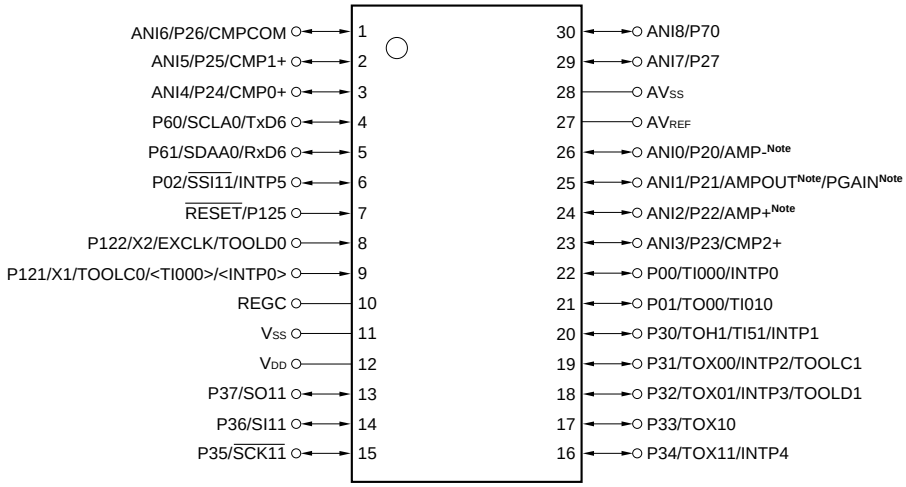
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	LVD, POR, PWM, WDT
Number of I/O	9
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0752ma-faa-ax

1.3.3 78K0/IB2

- 30-pin plastic SSOP (7.62 mm (300))



AMP-Note, AMP+Note:	Amplifier Input	REGC :	Regulator Capacitance
AMPOUTNote :	Amplifier Output	RESET :	Reset
PGAINNote :	Programmable Gain	RxD6 :	Receive Data
	Amplifier Input	SCLA0, SCK11 :	Serial Clock Input/Output
ANI0 to ANI8 :	Analog Input	SDAA0 :	Serial Data Input/Output
AVREF :	Analog Reference	SI11 :	Serial Data Input
	Voltage	SO11 :	Serial Data Output
AVSS :	Analog Ground	SSI11 :	Serial Interface Chip
EXCLK :	External Clock Input	TI000, TI010, TI51 :	Timer Input
	(Main System Clock)	TO00, TOH1 :	Timer Output
CMP0+ to CMP2+ :	Comparator Input	TOOLC0, TOOLC1 :	Clock Input for Tool
CMPCOM :	Comparator Common Input	TOOLD0, TOOLD1 :	Data Input/Output for Tool
INTP0 to INTP5 :	External Interrupt Input	TOX00, TOX01, TOX10,	
P00 to P02 :	Port 0	TOX11 :	Timer Output
P20 to P27 :	Port 2	TxD6 :	Transmit Data
P30 to P37 :	Port 3	VDD :	Power Supply
P60, P61 :	Port 6	VSS :	Ground
P70 :	Port 7	X1, X2 :	Crystal Oscillator
P121, P122, P125 :	Port 12		(Main System Clock)

Note μPD78F0755, 78F0756 (products with operational amplifier) only

Cautions 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

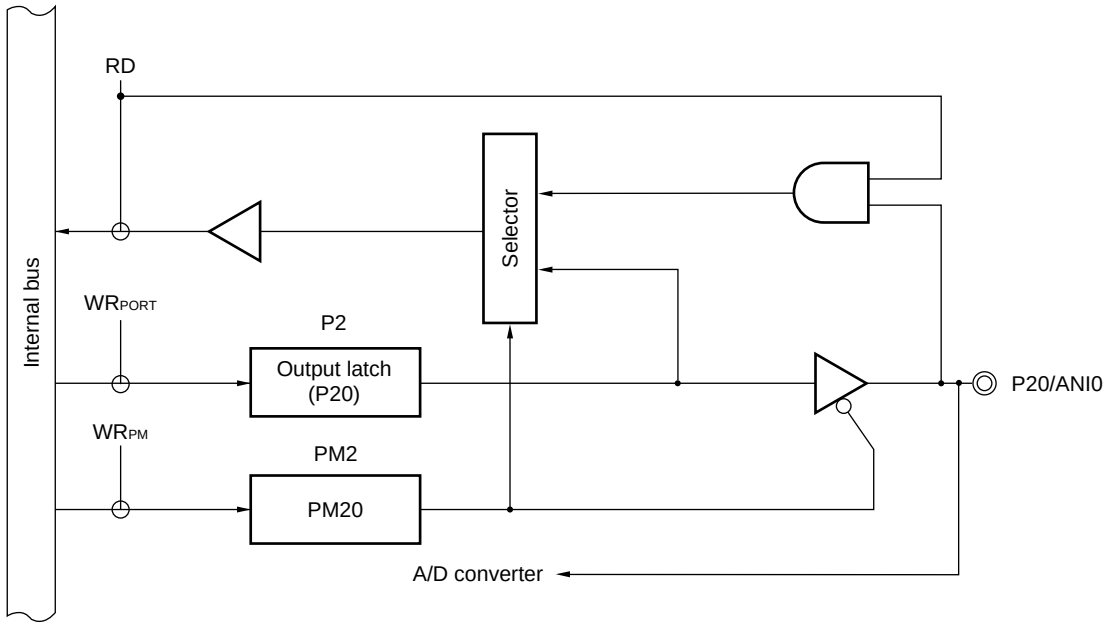
2. ANI0/P20/AMP-, ANI1/P21/AMPOUT/PGAIN, ANI2/P22/AMP+, ANI3/P23/CMP2+, ANI4/P24/CMP0+, ANI5/P25/CMP1+, ANI6/P26/CMPCOM, ANI7/P27, and ANI8/P70 are set in the analog input mode after release of reset.

3. RESET/P125 immediately after release of reset is set in the external reset input.

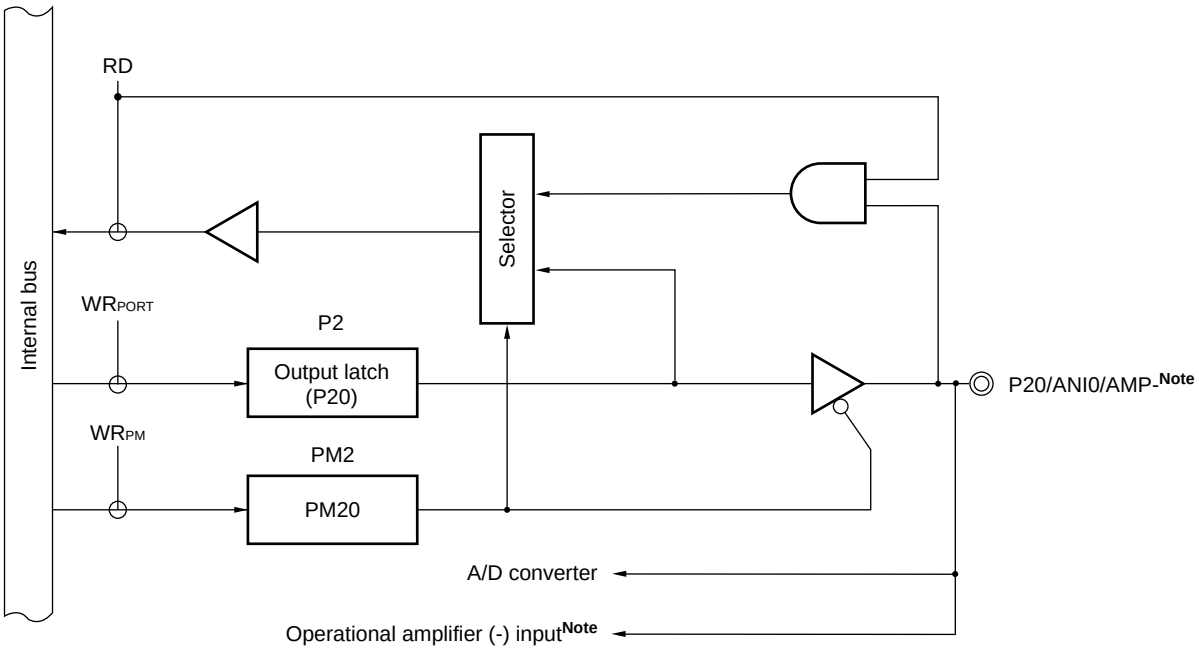
Remark Functions in angle brackets < > can be assigned by setting the input switch control register (MUXSEL).

Figure 4-4. Block Diagram of P20

(1) 78K0/IY2



(2) 78K0/IA2, 78K0/IB2



Note Products with operational amplifier only

P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Table 4-15. Settings of Port Mode Register and Output Latch When Using Alternate Function (78K0/IB2 (30 pins)) (2/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P31	TOX00	Output	0	0
	INTP2	Input	1	×
	TOOLC1	Input	×	×
P32	TOX01	Output	0	0
	INTP3	Input	1	×
	TOOLD1	I/O	×	×
P33	TOX10	Output	0	0
P34	TOX11	Output	0	0
	INTP4	Input	1	×
P35	$\overline{\text{SCK11}}$	Input	1	×
		Output	0	1
P36	SI11	Input	1	×
P37	SO11	Output	0	0
P60	SCLA0Notes 1, 2	I/O	0	1
	TxD6Note 3	Output	0	1
P61	SDAA0Notes 1, 2	I/O	0	1
	RxD6	Input	1	×
P70	ANI8Note 4	Input	1	×
P121	X1Note 5	–	×	×
	TOOLC0	Input	×	×
	<TI000>	Input	×	×
	<INTP0>	Input	×	×
P122	X2Note 5	–	×	×
	EXCLKNote 5	Input	×	×
	TOOLD0	I/O	×	×
P125	$\overline{\text{RESET}}$Note 6	Input	×	×

Notes 1. During I^2C communication, set SCLA0 and SDAA0 to N-ch open drain output (V_{DD} tolerance) mode by using POM6 register (refer to **4.3 (5) Port output mode register 6 (POM6)**).

2. When using an input compliant with the SMBus Specifications in I^2C communication, select the SMBus input buffer by using PIM6 register (refer to **4.3 (4) Port input mode register 6 (PIM6)**).

3. During UART/DALI communication, set TxD6 to normal output (CMOS output) mode by using POM6 register (refer to **4.3 (5) Port output mode register 6 (POM6)**).

4. The pin function can be selected by using ADPC1 register, PM7 register, and ADS register. Refer to **Table 4-12** of **4.2.5 Port 7**.

5. When using the P121 and P122 pins to connect a resonator for the main system clock (X1, X2) or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode or external clock input mode must be set by using OSCCTL register (for details, refer to **5.3 (1) Clock operation mode select register (OSCCTL)**). The reset value of OSCCTL is 00H (both P121 and P122 are input port pins).

6. Clear RSTM bit (bit 5 of RSTMASK register) to 0 when using P125 as an external reset input ($\overline{\text{RESET}}$).

Remark ×: Don't care
PM××: Port mode register
P××: Port output latch

4.6 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P20 is an output port, P21 to P27 are input ports (all pin statuses are high level), and the port latch value of port 2 is 00H, if the output of output port P20 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 2 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the 78K0/Ix2 microcontrollers.

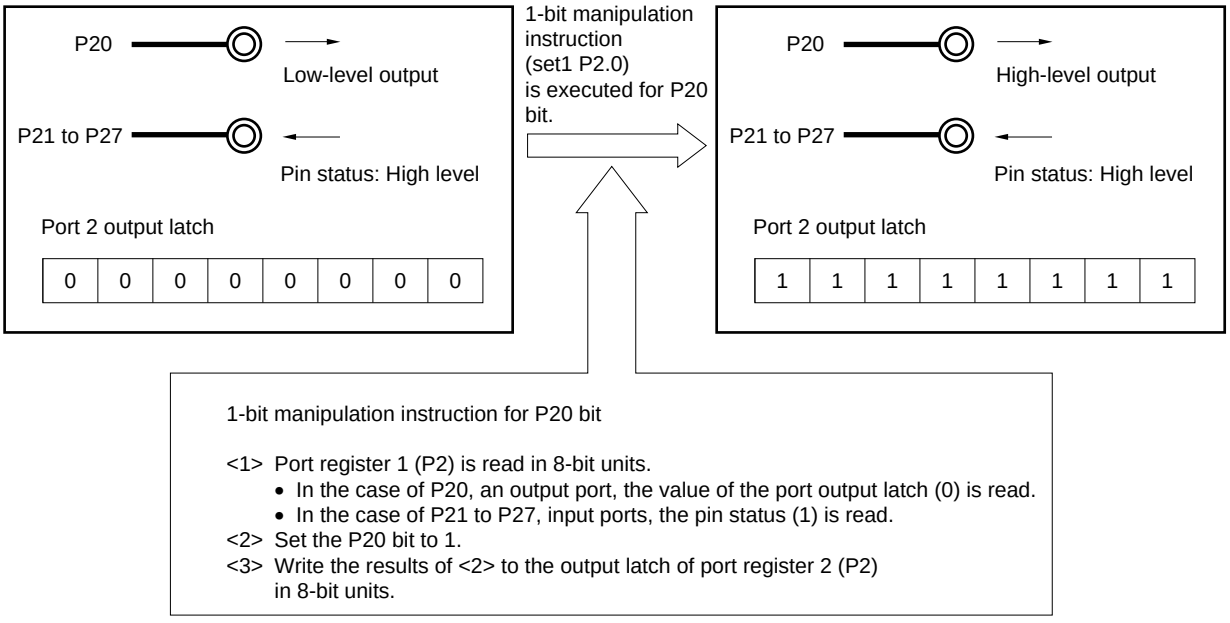
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P20, which is an output port, is read, while the pin statuses of P21 to P27, which are input ports, are read. If the pin statuses of P21 to P27 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 4-40. 1-Bit Manipulation Instruction (P20)



Remark The following instructions are 1-bit manipulation instructions.

- MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT11, NOT1

Figure 6-11. Format of 16-Bit Timer X1 Operation Control Register 2 (TX1CTL2)

Address: FF96H After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	<0>
TX1CTL2	0	0	0	0	0	0	TX1ADEN	TX1CCS

TX1ADEN	Control of generating A/D conversion synchronization trigger from TMX1
0	Disables generating A/D conversion synchronization trigger
1	Enables generating A/D conversion synchronization trigger[Note]

TX1CCS	TX1CCR0 register operation
0	Operates as compare register[Note]
1	Operates as capture register

Note When enabling generation of the A/D conversion synchronization trigger (TX1ADEN = 1), set the TX1CCR0 register to operate as a compare register (TX1CCS = 0), because the A/D conversion synchronization trigger is generated upon a match between the counter and the TX1CCR0 register.

Cautions 1. During the 16-bit timer operation, setting the other bits of TX1CTL2 is prohibited. However, TX1CTL2 can be refreshed (the same value is written).

2. The registers used by the A/D converter (ADM0, ADPC0, ADPC1, ADS) can be rewritten while the 16-bit timer X1 is operating.

3. A/D conversion synchronization triggers that occur while A/D conversion is stopped (ADCS = 0) are invalid. A/D conversion synchronization triggers that occur after A/D conversion has been enabled (ADCS = 1) are valid.

(4) 16-bit timer X0 operation control register 3 (TX0CTL3)

TX0CTL3 is a register that sets the mode of the interlocking function with comparator 2 and INTP0, and sets the operation when restarting upon comparator output.

TX0CTL3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TX0CTL3 to 00H.

Figure 6-16. 16-bit timer X1 output control register 0 (TX1IOC0)

Address: FF9BH After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
TX1IOC0	0	0	0	0	TX1TOC1	TX1TOC0	TX1TOL1	TX1TOL0

TX1TOC1	TOX11 output control
0	Disables timer output (Fixes to low-level output when TX1TOL1 = 0, and fixes to high-level output when TX1TOL1 = 1.)
1	Enables timer output (PWM output)

TX1TOC0	TOX10 output control
0	Disables timer output (Fixes to low-level output when TX1TOL0 = 0, and fixes to high-level output when TX1TOL0 = 1.)
1	Enables timer output (PWM output)

TX1TOL1	Default TOX11 output state setting
0	Normal output (low level)
1	Inverted output (high level)

TX1TOL0	Default TOX10 output state setting
0	Normal output (low level)
1	Inverted output (high level)

Cautions 1. During the timer operation, setting the other bits of TX1IOC0 is prohibited. However, TX1IOC0 can be refreshed (the same value is written).

2. The actual TOX10/P33 and TOX11/P34/INTP4 pin outputs are determined depending on PM33, P33, PM34, and P34 besides TOX10 and TOX11 outputs.

Table 6-2. Register Setting Bits Controlling Operation Mode and 16-bit Timers X0 and X1 (2/2)

Register	Bit	Operation mode					
		TMXn-only mode (n = 0, 1)		Synchronous start mode		Synchronous start/clear mode	
		TMX0	TMX1	Master (TMX0)	Slave (TMX1)	Master (TMX0)	Slave (TMX1)
TX0CTL4	TX0CMP1RP	Setting		Setting		–	–
	TX0CMP1RM1, TX0CMP1RM0	Setting is valid when TX0CMP 1RP = 0	–	Setting is valid when TX0CMP 1RP = 0	–	–	–
	TX0CMP0RP	Setting		Setting		–	–
	TX0CMP0RM1, TX0CMP0RM0	Setting is valid when TX0CMP 0RP = 0	–	Setting is valid when TX0CMP 0RP = 0	–	–	–
TX1CTL4	TX1CMP1RM1, TX1CMP1RM0	–	Setting is valid when TX0CMP 1RP = 1	–	Setting is valid when TX0CMP 1RP = 1	–	–
	TX1CMP0RM1, TX1CMP0RM0	–	Setting is valid when TX0CMP 0RP = 1	–	Setting is valid when TX0CMP 0RP = 1	–	–
TX0IOC0	TX0TOC1	Setting	–	Setting	–	Setting	–
	TX0TOC0	Setting	–	Setting	–	Setting	–
	TX0TOL1	Setting	–	Setting	–	Setting	–
	TX0TOL0	Setting	–	Setting	–	Setting	–
TX1IOC0	TX1TOC1	–	Setting	–	Setting	–	Setting
	TX1TOC0	–	Setting	–	Setting	–	Setting
	TX1TOL1	–	Setting	–	Setting	–	Setting
	TX1TOL0	–	Setting	–	Setting	–	Setting

<R> 6.4 Operation of 16-Bit Timer/Event Counter 00

(1) Interval timer operation

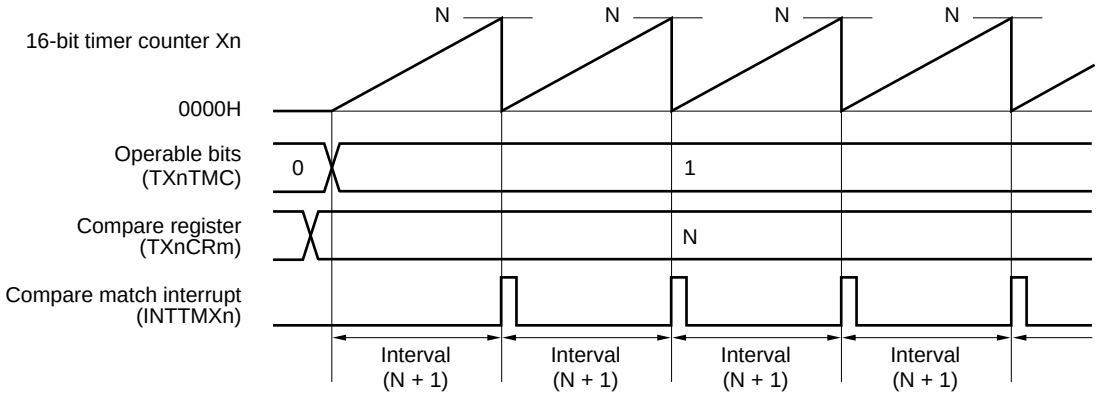
If bit 7 (TXnTMC) of the 16-bit timer Xn operation control register 0 (TXnCTL0) is set to 1, the count operation is started in synchronization with the count clock.

When the value of the 16-bit timer counter Xn (TMXn) later matches the value of TXnCRm, TMXn is cleared to 0000H and a match interrupt signal (INTTMXn) is generated. This INTTMXn signal enables TMXn to operate as an interval timer.

Remarks 1. For how to enable the INTTMXn interrupt, refer to **CHAPTER 17 INTERRUPT FUNCTIONS**.

2. m = 1, 3
n = 0, 1

Figure 6-18. Basic Timing Example of Interval Timer Operation



Remark m = 1, 3
n = 0, 1

CHAPTER 10 WATCHDOG TIMER

10.1 Functions of Watchdog Timer

The watchdog timer is mounted onto all 78K0/Ix2 microcontroller products.

The watchdog timer operates on the internal low-speed oscillation clock.

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases.

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than “ACH” is written to WDTE
- If data is written to WDTE during a window close period
- If the instruction is fetched from an area not set by the IMS register (detection of an invalid check while the CPU hangs up)
- If the CPU accesses an area that is not set by the IMS register (excluding FB00H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)

When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1. For details of RESF, refer to **CHAPTER 20 RESET FUNCTION**.

Cautions 1. Set a channel to be used for A/D conversion in the input mode by using port mode registers 2 and 7 (PM2, PM7).

2. Set ADS after PGA operation setting when selecting the PGA output signal as analog input. Set ADS after single AMP operation setting when selecting the operational amplifier output signal as analog input.

3. To select the internal voltage (1.2 V) as an analog input, set the ADCS bit to 1 when at least 10 μs have elapsed after having set the V12SEL bit to 1 while the A/D conversion operation was stopped (ADCS = 0).

4. If data is written to ADS, a wait cycle is generated. Do not write data to ADS when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.

(4) Port mode register 2 (PM2)

When using AMP-/ANI0/P20, AMPOUT/PGAIN/ANI1/P21, and AMP+/ANI2/P22 pins for the operational amplifier, set PM20 to PM22 to 1.

The output latches of P20 to P22 at this time may be 0 or 1.

If PM20 to PM22 are set to 0, they cannot be used as the operational amplifier pins.

PM2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM2 to FFH.

Figure 12-5. Format of Port Mode Register 2 (PM2)

(1) 78K0/IY2

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	PM25	PM24	PM23	PM22	1	PM20

Caution Be sure to set bits 1, 6, and 7 of PM2 to 1.

(2) 78K0/IA2

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20

Caution Be sure to set bits 6 and 7 of PM2 to 1.

(3) 78K0/IB2

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 13-5. Format of DA0 Internal Reference Voltage Selection Register (C0RVM)

Address: FF63H After reset: 00H R/W

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>
C0RVM	CVRE	0	0	C0VRS4	C0VRS3	C0VRS2	C0VRS1	C0VRS0

CVRE	Internal reference voltage generation operation control
0	Stops operation
1	Enables operation

C0VRS4	C0VRS3	C0VRS2	C0VRS1	C0VRS0	Reference voltage level (DA0) setting
0	0	0	0	0	0.05 V (TYP.)
0	0	0	0	1	0.1 V (TYP.)
0	0	0	1	0	0.15 V (TYP.)
0	0	0	1	1	0.2 V (TYP.)
0	0	1	0	0	0.25 V (TYP.)
0	0	1	0	1	0.3 V (TYP.)
0	0	1	1	0	0.35 V (TYP.)
0	0	1	1	1	0.4 V (TYP.)
0	1	0	0	0	0.44 V (TYP.)
0	1	0	0	1	0.49 V (TYP.)
0	1	0	1	0	0.54 V (TYP.)
0	1	0	1	1	0.59 V (TYP.)
0	1	1	0	0	0.64 V (TYP.)
0	1	1	0	1	0.69 V (TYP.)
0	1	1	1	0	0.74 V (TYP.)
0	1	1	1	1	0.79 V (TYP.)
1	0	0	0	0	0.84 V (TYP.)
1	0	0	0	1	0.89 V (TYP.)
1	0	0	1	0	0.94 V (TYP.)
1	0	0	1	1	0.99 V (TYP.)
1	0	1	0	0	1.04 V (TYP.)
1	0	1	0	1	1.09 V (TYP.)
1	0	1	1	0	1.14 V (TYP.)
1	0	1	1	1	1.19 V (TYP.)
1	1	0	0	0	1.23 V (TYP.)
1	1	0	0	1	1.28 V (TYP.)
1	1	0	1	0	1.33 V (TYP.)
1	1	0	1	1	1.38 V (TYP.)
1	1	1	0	0	1.43 V (TYP.)
1	1	1	0	1	1.48 V (TYP.)
1	1	1	1	0	1.53 V (TYP.)
1	1	1	1	1	1.58 V (TYP.)

Caution To change the reference voltage level when the internal reference voltage generation operation is enabled (CVRE = 1), a voltage stabilization wait time is required. See Figure 13-12 Example of Procedure for Changing Internal Reference Voltage for the setting method.

(4) DALI communication (slave transmission/reception) operation procedure

An example of DALI slave processing is shown below.

<1> Perform initial settings such as of the port I/Os and baud rate (1,200 bps).

<2> Wait for a command to be transmitted from the master.

<3> After receiving the command from the master, acquire and analyze the command data stored in the DALI receive buffer register (RXBDL).

<4> After analyzing the command, perform the following processing.

- **Successive receive commands**
  - **→ After receiving a command again, perform command processing and return to step <2>.**
- **Command without a response in a single reception**
  - **→ Perform command processing and return to step <2>.**
- **Command requiring a response in a single reception**
  - **→ Perform command processing, and if a response is required, return to step <2> after transmitting data.**
- **Command other than the above**
  - **→ Perform processing as an undefined command and return to step <2>.**

The flow of the above operation procedure and the transmission/reception timing chart are shown below.

Figure 15-7. Format of IICA Flag Register 0 (IICAF0)

Address: FFA9H After reset: 00H R/W[Note]

Symbol	<7>	<6>	5	4	3	2	<1>	<0>
IICAF0	STCF	IICBSY	0	0	0	0	STCEN	IICRSV

STCF	STT0 clear flag
0	Generate start condition
1	Start condition generation unsuccessful: clear STT0 flag

Condition for clearing (STCF = 0)	Condition for setting (STCF = 1)
• Cleared by STT0 = 1 • When IICE0 = 0 (operation stop) • Reset	• Generating start condition unsuccessful and the STT0 bit cleared to 0 when communication reservation is disabled (IICRSV = 1).

IICBSY	I^2C bus status flag
0	Bus release status (communication initial status when STCEN = 1)
1	Bus communication status (communication initial status when STCEN = 0)

Condition for clearing (IICBSY = 0)	Condition for setting (IICBSY = 1)
• Detection of stop condition • When IICE0 = 0 (operation stop) • Reset	• Detection of start condition • Setting of the IICE0 bit when STCEN = 0

STCEN	Initial start enable trigger
0	After operation is enabled (IICE0 = 1), enable generation of a start condition upon detection of a stop condition.
1	After operation is enabled (IICE0 = 1), enable generation of a start condition without detecting a stop condition.

Condition for clearing (STCEN = 0)	Condition for setting (STCEN = 1)
• Cleared by instruction • Detection of start condition • Reset	• Set by instruction

IICRSV	Communication reservation function disable bit
0	Enable communication reservation
1	Disable communication reservation

Condition for clearing (IICRSV = 0)	Condition for setting (IICRSV = 1)
• Cleared by instruction • Reset	• Set by instruction

Note Bits 6 and 7 are read-only.

Cautions 1. Write to the STCEN bit only when the operation is stopped (IICE0 = 0).

2. As the bus release status (IICBSY = 0) is recognized regardless of the actual bus status when STCEN = 1, when generating the first start condition (STT0 = 1), it is necessary to verify that no third party communications are in progress in order to prevent such communications from being destroyed.

3. Write to the IICRSV bit only when the operation is stopped (IICE0 = 0).

Remark STT0: Bit 1 of IICA control register 0 (IICACTL0)
IICE0: Bit 7 of IICA control register 0 (IICACTL0)

15.4.2 Setting transfer clock by using IICWL and IICWH registers

(1) Setting transfer clock on master side

$$\text{Transfer clock} = \frac{f_{PRS}}{IICWL + IICWH + f_{PRS}(t_R + t_F)}$$

At this time, the optimal setting values of the IICWL and IICWH registers are as follows.
(The fractional parts of all setting values are rounded up.)

- When the fast mode

$$IICWL = \frac{0.52}{\text{Transfer clock}} \times f_{PRS}$$
$$IICWH = \left(\frac{0.48}{\text{Transfer clock}} - t_R - t_F\right) \times f_{PRS}$$

- When the normal mode

$$IICWL = \frac{0.47}{\text{Transfer clock}} \times f_{PRS}$$
$$IICWH = \left(\frac{0.53}{\text{Transfer clock}} - t_R - t_F\right) \times f_{PRS}$$

(2) Setting IICWL and IICWH on slave side

(The fractional parts of all setting values are truncated.)

- When the fast mode

$$IICWL = 1.3\ \mu s \times f_{PRS}$$
$$IICWH = (1.2\ \mu s - t_R - t_F) \times f_{PRS}$$

- When the normal mode

$$IICWL = 4.7\ \mu s \times f_{PRS}$$
$$IICWH = (5.3\ \mu s - t_R - t_F) \times f_{PRS}$$

Caution Note the minimum f_{PRS} operation frequency when setting the transfer clock. The minimum f_{PRS} operation frequency for serial interface IICA is determined according to the mode.

Fast mode: f_{PRS} = 3.5 MHz (min.)

Normal mode: f_{PRS} = 1 MHz (min.)

Remarks 1. Calculate the rise time (t_R) and fall time (t_F) of the SDA0 and SCLA0 signals separately, because they differ depending on the pull-up resistance and wire load.

2. IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDAA0 and SCLA0 signal falling times (refer to **CHAPTER 28 ELECTRICAL SPECIFICATIONS**)
t_R: SDAA0 and SCLA0 signal rising times (refer to **CHAPTER 28 ELECTRICAL SPECIFICATIONS**)
f_{PRS}: Peripheral hardware clock frequency

Figure 18-6. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L, MK1H) (78K0/IA2)

Address: FFE4H After reset: FFH R/W

Symbol	<7>	6	<5>	<4>	<3>	2	<1>	<0>
MK0L	SREMK6	1	PMK4	PMK3	PMK2	1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5	<4>	<3>	2	<1>	<0>
MK0H	TMMK010	TMMK000	TMMKX1	TMMKX0	TMMKH1	1	STMK6	SRMK6

Address: FFE6H After reset: FFH R/W

Symbol	7	<6>	<5>	<4>	<3>	2	1	<0>
MK1L	1	CMPMK2	CMPMK1	CMPMK0	TMMK51	1	1	ADMK

Address: FFE7H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	<0>
MK1H	1	1	1	1	1	1	1	IICAMK0

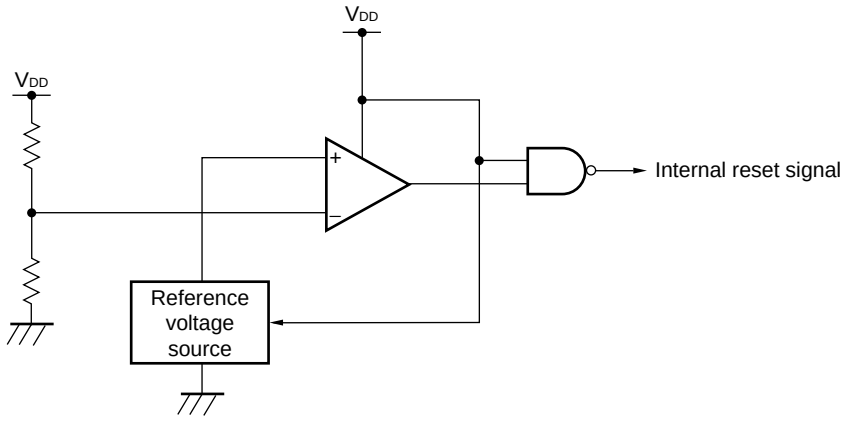
XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution Be sure to set bits 2 and 6 of MK0L, bit 2 of MK0H, bits 1, 2, and 7 of MK1L, and bits 1 to 7 of MK1H to 1.

21.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 21-1.

Figure 21-1. Block Diagram of Power-on-Clear Circuit



21.3 Operation of Power-on-Clear Circuit

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds POC detection voltage (V_{POR} = 1.61 V ±0.09 V), the reset status is released.

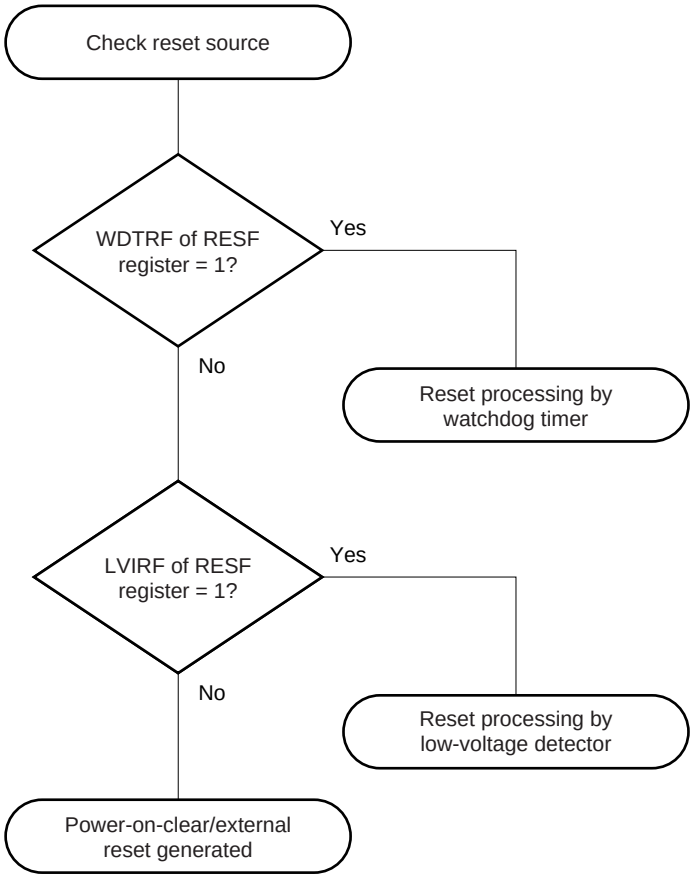
Caution If the LVI default function enabled is set by using an option byte, the reset signal is not released until the supply voltage (V_{DD}) exceeds 1.91 V ±0.1 V.

- The supply voltage (V_{DD}) and POC detection voltage (V_{PDR} = 1.59 V ±0.09 V) are compared. When $V_{DD} < V_{PDR}$, the internal reset signal is generated.

The timing of generation of the internal reset signal by the power-on-clear circuit and low-voltage detector is shown below.

Figure 21-3. Example of Software Processing After Reset Release (2/2)

• Checking reset source



(2) Non-port functions

Port		78K0/IY2	78K0/IA2	78K0/IB2	
		16 pins	20 pins	30 pins	32 pins
Power supply, ground		V_{DD}, V_{SS}, AV_{REF}		V_{DD}, AV_{REF}, V_{SS}, AV_{SS}	
Regulator		REGC			
Reset		$\overline{\text{RESET}}$			
Clock oscillation		X1, X2, EXCLK			
Interrupt		INTP0, INTP2 to INTP4		INTP0 to INTP5	INTP0, INTP2 to INTP5
Timer	TMX0, TMX1	TOX00, TOX01, TOX10, TOX11			
	TM00	TI000		TI000, TI010, TO00	TI000
	TM51	TI51			
	TMH1	TOH1			
Serial interface	UART6/ DALI	–	RxD6, TxD6		
	IICA	–	SCLA0, SDAA0		
	CSI11	–		$\overline{\text{SCK11}}$, SI11, SO11, $\overline{\text{SSI11}}$	
A/D converter		ANI0, ANI1, ANI3 to ANI5	ANI0 to ANI5	ANI0 to ANI8	
Operational amplifier[Note]		PGAIN	AMP+, AMP-, AMPOUT, PGAIN		
Comparator		CMP0+ to CMP2+		CMP0+ to CMP2+, CMPCOM	
On-chip debug function		TOOLC0, TOOLC1, TOOLD0, TOOLD1			

Note Products with operational amplifier only.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

28.5.7 Supply Voltage Rise Time

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 2.7 V (V_{DD} (MIN.)) Note (V_{DD}: 0 V → 2.7 V)	t_{PUP1}	LVI default start function stopped is set (LVISTART (Option Byte) = 0), when $\overline{\text{RESET}}$ input is not used			5.4	ms
Maximum time to rise to 2.7 V (V_{DD} (MIN.)) Note (releasing $\overline{\text{RESET}}$ input → V_{DD}: 2.7 V)	t_{PUP2}	LVI default start function stopped is set (LVISTART (Option Byte) = 0), when $\overline{\text{RESET}}$ input is used			1.9	ms

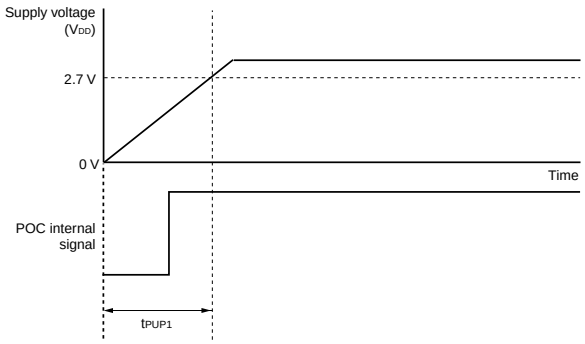
Note Make sure to raise the power supply in a shorter time than this.

Caution The operation guaranteed range is 2.7 V ≤ V_{DD} ≤ 5.5 V. If the rise of the voltage to reach 2.7 V after turning on the power is more gradual than 0.5 V/ms (MIN.), perform one of the following operations.

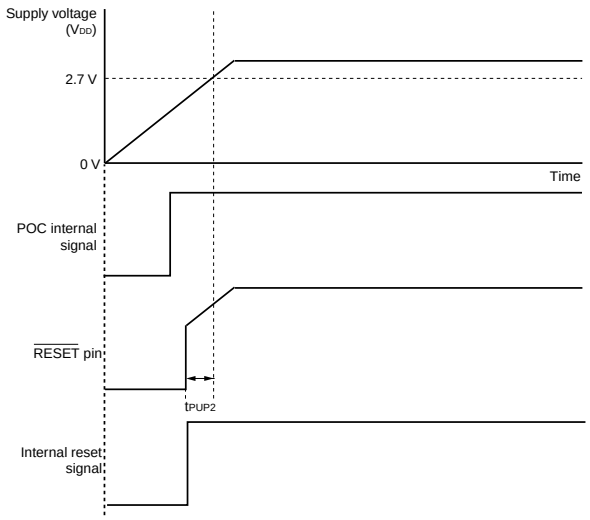
- **Input a low level to the $\overline{\text{RESET}}$ pin until 2.7 V is reached after turning on the power.**
- **Set the LVI default start function to operate (LVISTART = 1) using the option byte and perform a wait processing until the supply voltage rises from 1.91 V (TYP.) to 2.7 V.**

Supply Voltage Rise Time Timing

- When $\overline{\text{RESET}}$ pin input is not used



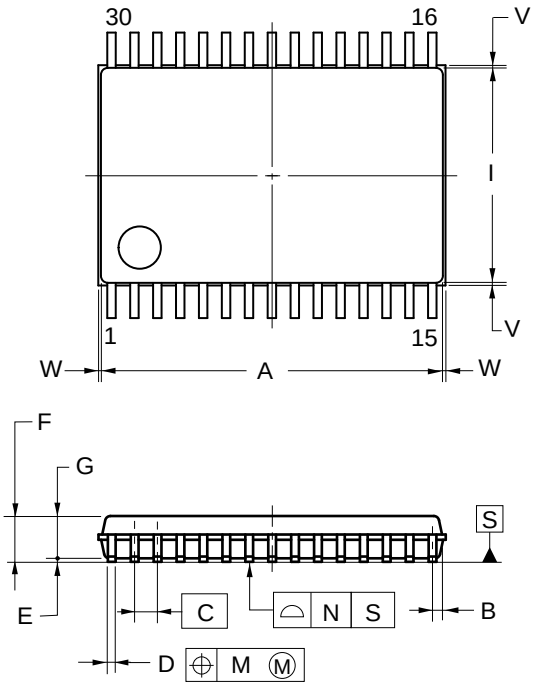
- When $\overline{\text{RESET}}$ pin input is used (when external reset is released by the $\overline{\text{RESET}}$ pin, after POC has been released)

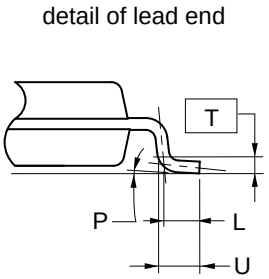


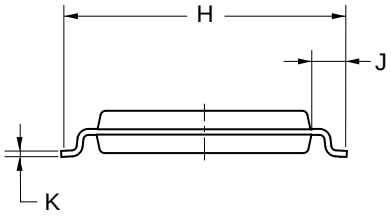
29.3 78K0/IB2

- μPD78F0745MC-CAB-AX, 78F0746MC-CAB-AX, 78F0755MC-CAB-AX, 78F0756MC-CAB-AX

30-PIN PLASTIC SSOP (7.62mm (300))







NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

(UNIT:mm)

ITEM	DIMENSIONS
A	9.70±0.10
B	0.30
C	0.65 (T.P.)
D	$0.22^{+0.10}_{-0.05}$
E	0.10±0.05
F	1.30±0.10
G	1.20
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.05}_{-0.01}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

P30MC-65-CAB