Renesas Electronics America Inc - UPD78F0753MC-CAA-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	DALI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0753mc-caa-ax

(g) $\overline{\text{SSI11}}$

This is a chip select input pin of serial interface CSI11.

2.2.2 P20 to P27 (port 2)

P20 to P27 function as an I/O port. These pins also function as pins for A/D converter analog input, operational amplifier I/O, and PGA input.

78K0/IY2	78K0/IA2	78K0/IB2
16 Pins	20 Pins	30 Pins/32 Pins
P20/ANI0	P20/ANI0/AMP-Note	P20/ANI0/AMP-Note
P21/ANI1/PGAINNote	P21/ANI1/AMPOUTNote/PGAINNote	P21/ANI1/AMPOUTNote/PGAINNote
–	P22/ANI2/AMP+Note	P22/ANI2/AMP+Note
P23/ANI3/CMP2+	P23/ANI3/CMP2+	P23/ANI3/CMP2+
P24/ANI4/CMP0+	P24/ANI4/CMP0+	P24/ANI4/CMP0+
P25/ANI5/CMP1+	P25/ANI5/CMP1+	P25/ANI5/CMP1+
–	–	P26/ANI6/CMPCOM
–	–	P27/ANI7

Note Products with operational amplifier only

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P27 function as an I/O port. P20 to P27 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P27 function as A/D converter analog input, operational amplifier I/O, and PGA input.

(a) ANI0 to ANI7

These are A/D converter analog input pins. When using these pins as analog input pins, refer to **(5) ANI0/P20 to ANI7/P27 and ANI8/P70** in **11.6 Cautions for A/D Converter**.

(b) AMP+, AMP-

These are operational amplifier input pins.

(c) AMPOUT

This is an operational amplifier output pin.

(d) PGAIN

This is a PGA (Programmable gain amplifier) input pin.

(e) CMP0+ to CMP2+

These are comparator input pins.

(7) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using OSTS after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with OSTC that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using OSTC.

OSTS can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets OSTS to 05H.

Figure 5-8. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection	
				f_X = 10 MHz
0	0	1	$2^{11}/f_X$	204.8 μs
0	1	0	$2^{13}/f_X$	819.2 μs
0	1	1	$2^{14}/f_X$	1.64 ms
1	0	0	$2^{15}/f_X$	3.27 ms
1	0	1	$2^{16}/f_X$	6.55 ms
Other than above			Setting prohibited	

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

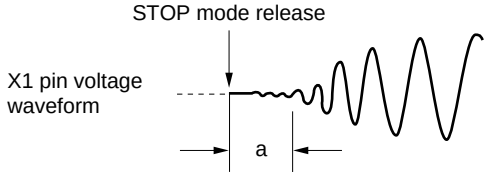
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).



Remark f_X: X1 clock oscillation frequency

Figure 6-11. Format of 16-Bit Timer X1 Operation Control Register 2 (TX1CTL2)

Address: FF96H After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	<0>
TX1CTL2	0	0	0	0	0	0	TX1ADEN	TX1CCS

TX1ADEN	Control of generating A/D conversion synchronization trigger from TMX1
0	Disables generating A/D conversion synchronization trigger
1	Enables generating A/D conversion synchronization trigger[Note]

TX1CCS	TX1CCR0 register operation
0	Operates as compare register[Note]
1	Operates as capture register

Note When enabling generation of the A/D conversion synchronization trigger (TX1ADEN = 1), set the TX1CCR0 register to operate as a compare register (TX1CCS = 0), because the A/D conversion synchronization trigger is generated upon a match between the counter and the TX1CCR0 register.

Cautions 1. During the 16-bit timer operation, setting the other bits of TX1CTL2 is prohibited. However, TX1CTL2 can be refreshed (the same value is written).

2. The registers used by the A/D converter (ADM0, ADPC0, ADPC1, ADS) can be rewritten while the 16-bit timer X1 is operating.

3. A/D conversion synchronization triggers that occur while A/D conversion is stopped (ADCS = 0) are invalid. A/D conversion synchronization triggers that occur after A/D conversion has been enabled (ADCS = 1) are valid.

(4) 16-bit timer X0 operation control register 3 (TX0CTL3)

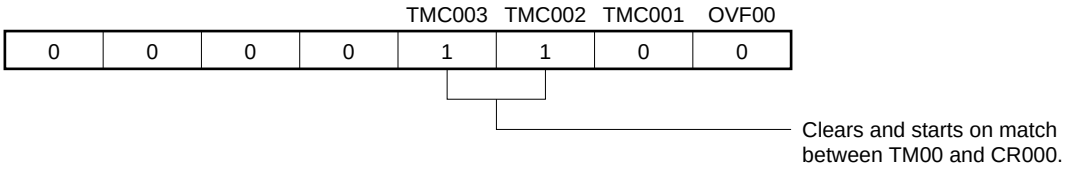
TX0CTL3 is a register that sets the mode of the interlocking function with comparator 2 and INTP0, and sets the operation when restarting upon comparator output.

TX0CTL3 can be set by a 1-bit or 8-bit memory manipulation instruction.

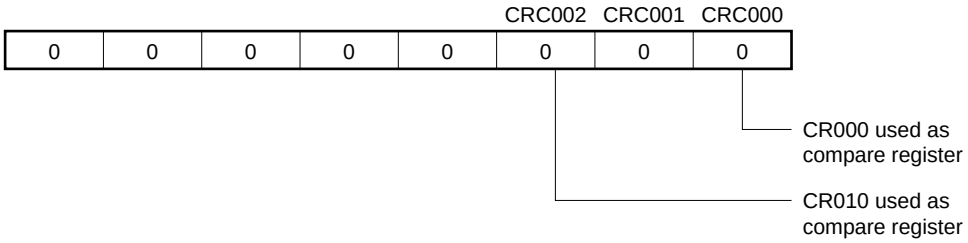
Reset signal generation clears TX0CTL3 to 00H.

Figure 7-42. Example of Register Settings for PPG Output Operation (1/2)

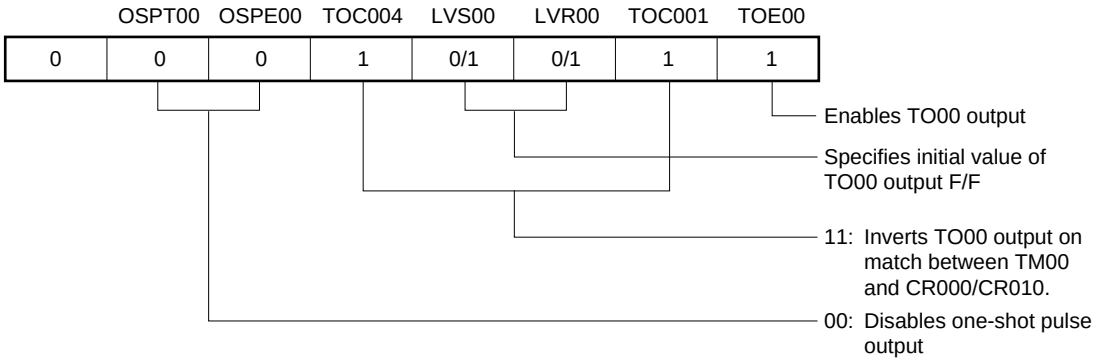
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)

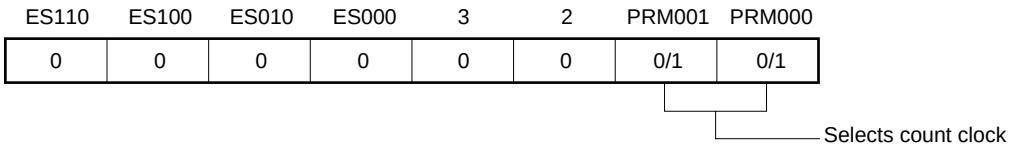


Figure 7-52. Example of Register Settings for Pulse Width Measurement (2/2)

(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

This register is used as a capture register. Either the TI000 or TI010 pin is selected as a capture trigger. When a specified edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

(g) 16-bit capture/compare register 010 (CR010)

This register is used as a capture register. The signal input to the TI000 pin is used as a capture trigger. When the capture trigger is detected, the count value of TM00 is stored in CR010.

(8) 8-bit A/D conversion result register L (ADCRL)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the lower 8 bits of the A/D conversion result.

(9) 8-bit A/D conversion result register H (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

(10) 10-bit A/D conversion result register for TMXn synchronization (ADCRXn = 0, 1)

If A/D conversion is started with the output of 16-bit timer Xn as the trigger, the conversion result is loaded from the successive approximation register and the A/D conversion result is held in the lower 10 bits (the higher 6 bits are fixed to 0) every time an A/D conversion ends.

(11) 8-bit A/D conversion result register L for TMXn synchronization (ADCRXnL = 0, 1)

If A/D conversion is started with the output of 16-bit timer Xn as the trigger, the conversion result is loaded from the successive approximation register and the lower 8 bits of the A/D conversion result are held in ADCRXnL register, every time an A/D conversion ends.

Caution When data is read from ADCR, ADCRL, ADCRH, ADCRX0, ADCRX1, ADCRX0L, and ADCRX1L, a wait cycle is generated. Do not read data from ADCR, ADCRL, ADCRH, ADCRX0, ADCRX1, ADCRX0L, and ADCRX1L when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.

(12) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When all the specified A/D conversion has been completed, this controller generates an A/D conversion end interrupt request signal (INTAD).

(13) AV_{REF} pin

This pin inputs an analog power/reference voltage to the A/D converter. Make this pin the same potential as the V_{DD} pin when ports 2 and 7 are used as a digital port.

The signal input to ANI0 to ANI8 is converted into a digital signal, based on the voltage applied across AV_{REF} and AV_{SS}.

(14) AV_{SS} pin (78K0/IB2 only)

This is the ground potential pin of the A/D converter. Always use this pin at the same potential as that of the V_{SS} pin even when the A/D converter is not used.

(15) V_{SS} pin

This is the ground potential pin. In the 78K0/IY2 and 78K0/IA, V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

Cautions 1. Set a channel to be used for A/D conversion in the input mode by using port mode registers 2 and 7 (PM2, PM7).

2. Set ADS after PGA operation setting when selecting the PGA output signal as analog input. Set ADS after single AMP operation setting when selecting the operational amplifier output signal as analog input.

3. To select the internal voltage (1.2 V) as an analog input, set the ADCS bit to 1 when at least 10 μs have elapsed after having set the V12SEL bit to 1 while the A/D conversion operation was stopped (ADCS = 0).

4. If data is written to ADS, a wait cycle is generated. Do not write data to ADS when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 31 CAUTIONS FOR WAIT.

(4) Port mode register 2 (PM2)

When using AMP-/ANI0/P20, AMPOUT/PGAIN/ANI1/P21, and AMP+/ANI2/P22 pins for the operational amplifier, set PM20 to PM22 to 1.

The output latches of P20 to P22 at this time may be 0 or 1.

If PM20 to PM22 are set to 0, they cannot be used as the operational amplifier pins.

PM2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM2 to FFH.

Figure 12-5. Format of Port Mode Register 2 (PM2)

(1) 78K0/IY2

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	PM25	PM24	PM23	PM22	1	PM20

Caution Be sure to set bits 1, 6, and 7 of PM2 to 1.

(2) 78K0/IA2

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20

Caution Be sure to set bits 6 and 7 of PM2 to 1.

(3) 78K0/IB2

Address: FF22H After reset: FFH R/W

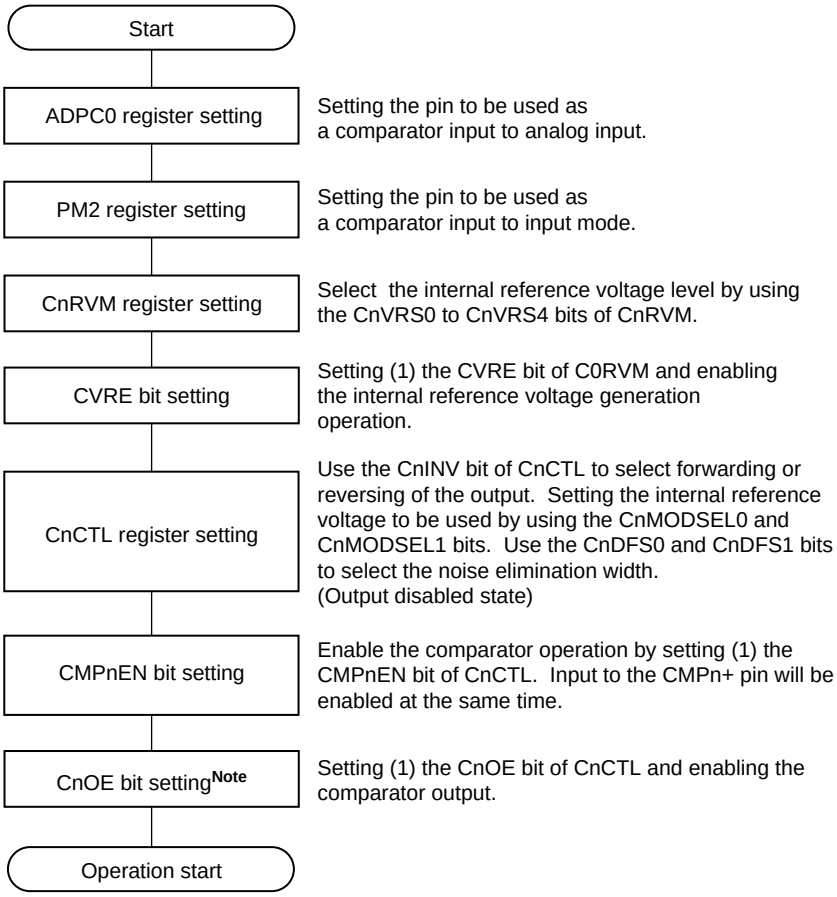
Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

13.4 Operation of Comparators

13.4.1 Starting comparator operation (using internal reference voltage for comparator reference voltage)

Figure 13-11. Example of Setting Procedure when Starting Comparator Operation (Using Internal Reference Voltage for Comparator Reference Voltage)



Note Set the CnOE bit to 1 when at least 20 μs have elapsed after having set the CVRE register.

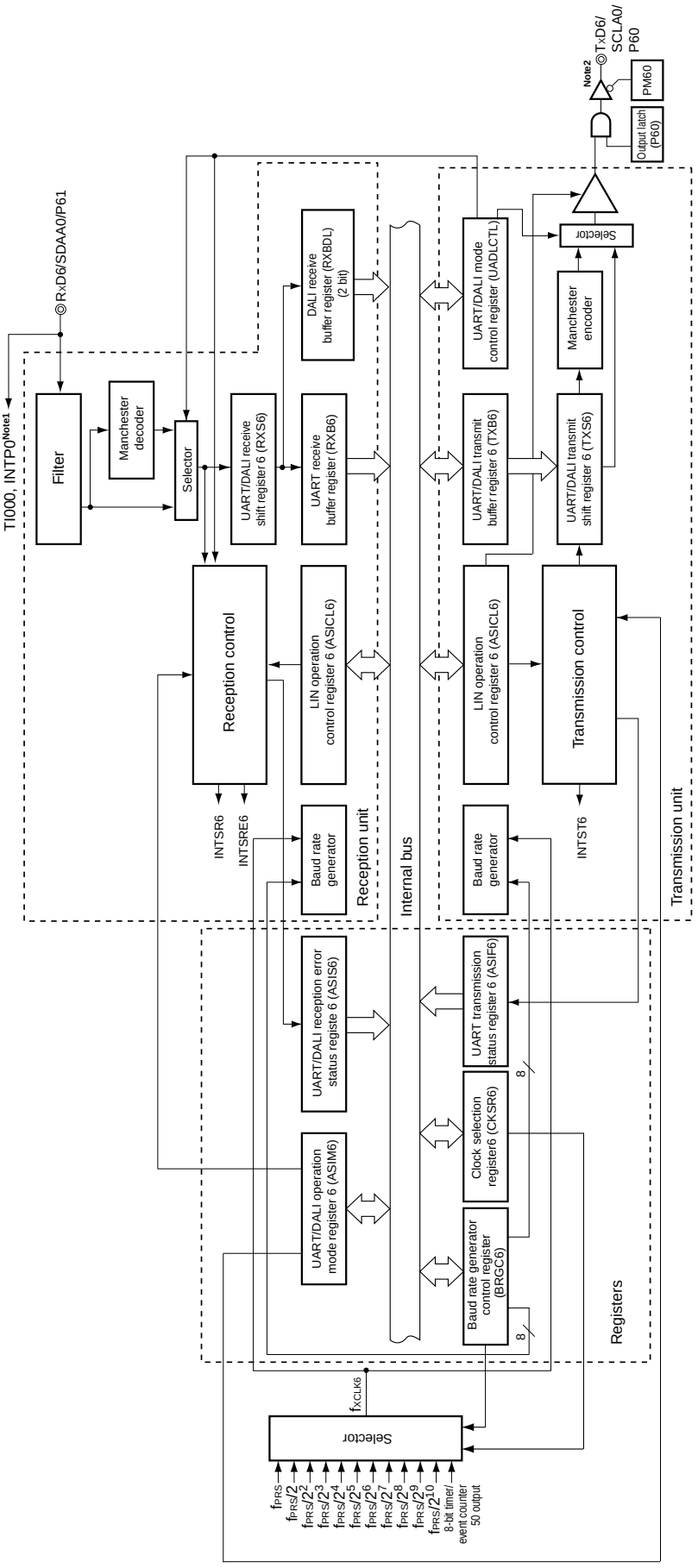
14.2 Configuration of Serial Interface UART6/DALI

Serial interface UART6/DALI includes the following hardware.

Table 14-1. Configuration of Serial Interface UART6/DALI

Item	Configuration
Registers	UART receive buffer register 6 (RXB6) UART/DALI receive shift register 6 (RXS6) DALI receive buffer register (RXBDL) UART/DALI transmit buffer register 6 (TXB6) UART/DALI transmit shift register 6 (TXS6)
Control registers	UART/DALI mode control register (UADLCTL) UART/DALI operation mode register 6 (ASIM6) UART/DALI reception error status register 6 (ASIS6) UART transmission status register 6 (ASIF6) Clock selection register 6 (CKSR6) Baud rate generator control register 6 (BRGC6) LIN operation control register 6 (ASICL6) Input switch control register (ISC) Port mode register 6 (PM6) Port register 6 (P6) Port output mode register 6 (POM6)

Figure 14-4. Block Diagram of Serial Interface UART6/DALI



Notes 1. Selectable with input switch control register (ISC).

2. When using the P60/TxD6/SCLA0 pin as the data output of serial interface UART6/DALI, clear POM60 to 0

15.5.12 Arbitration

When several master devices simultaneously generate a start condition (when the STT0 bit is set to 1 before the STD0 bit is set to 1), communication among the master devices is performed as the number of clocks are adjusted until the data differs. This kind of operation is called arbitration.

When one of the master devices loses in arbitration, an arbitration loss flag (ALD0) in the IICA status register 0 (IICAS0) is set (1) via the timing by which the arbitration loss occurred, and the SCLA0 and SDAA0 lines are both set to high impedance, which releases the bus.

The arbitration loss is detected based on the timing of the next interrupt request (the eighth or ninth clock, when a stop condition is detected, etc.) and the ALD0 = 1 setting that has been made by software.

For details of interrupt request timing, refer to **15.5.8 Interrupt request (INTIICA0) generation timing and wait control**.

Remark STD0: Bit 1 of IICA status register 0 (IICAS0)
STT0: Bit 1 of IICA control register 0 (IICACTL0)

Figure 15-22. Arbitration Timing Example

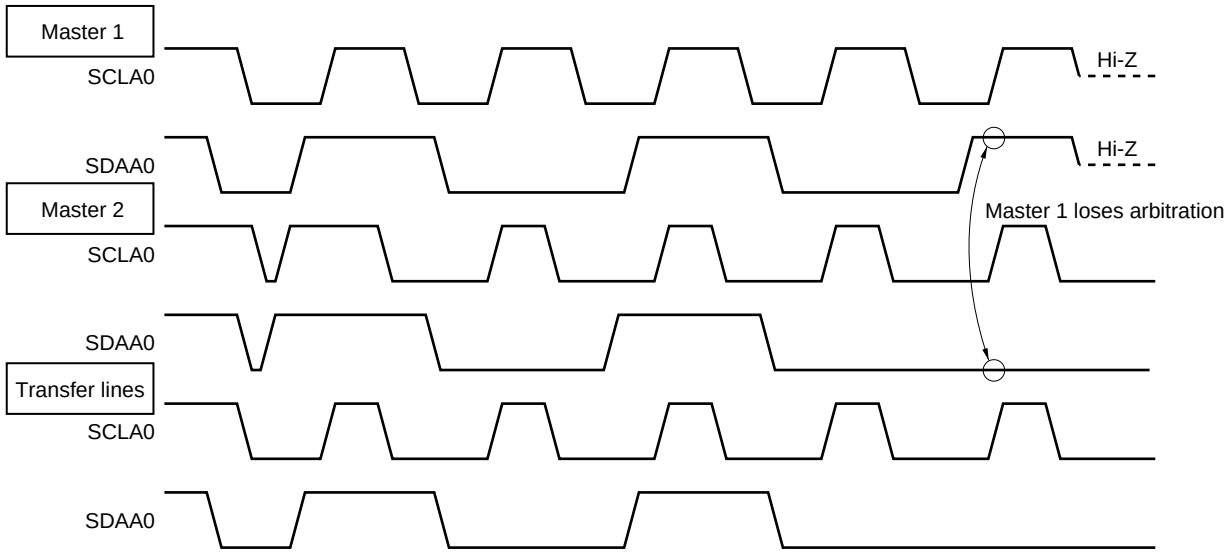
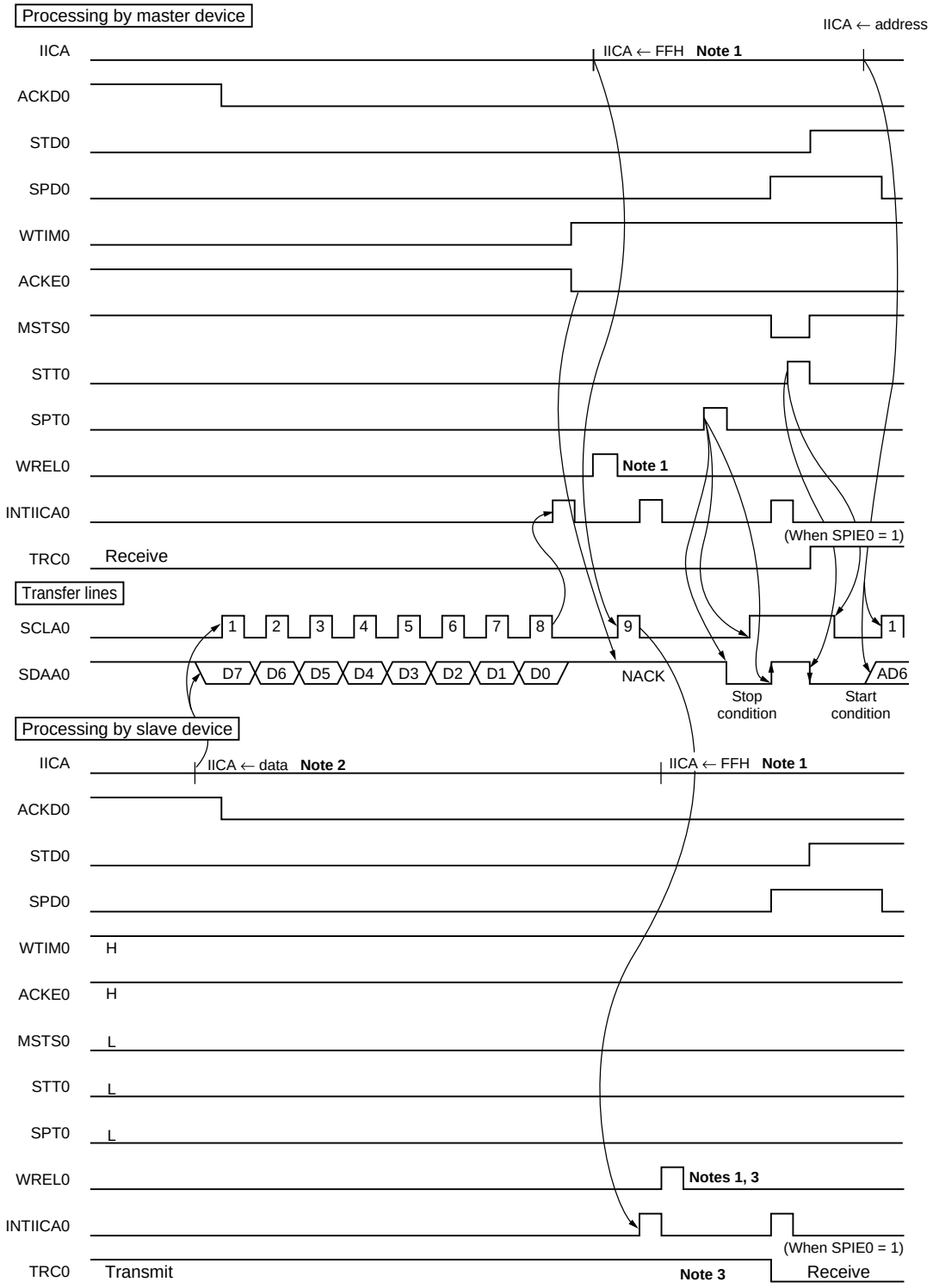


Figure 15-34. Example of Slave to Master Communication
(When 8-Clock and 9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (3/3)

(3) Stop condition



Notes 1. To cancel wait, write “FFH” to IICA or set WREL0.

2. Write data to IICA, not setting WREL0, in order to cancel a wait state during slave transmission.

3. If a wait state during slave transmission is canceled by setting WREL0, TRC0 will be cleared.

18.4.4 Interrupt request hold

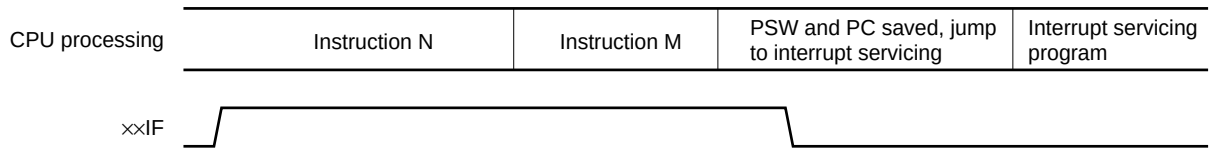
There are instructions where, even if an interrupt request is issued for them while another instruction is being executed, request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV A, PSW
- MOV PSW, A
- MOV1 PSW. bit, CY
- MOV1 CY, PSW. bit
- AND1 CY, PSW. bit
- OR1 CY, PSW. bit
- XOR1 CY, PSW. bit
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- PUSH PSW
- POP PSW
- BT PSW. bit, $addr16
- BF PSW. bit, $addr16
- BTCLR PSW. bit, $addr16
- EI
- DI
- Manipulation instructions for the IF0L, IF0H, IF1L, IF1H, MK0L, MK0H, MK1L, MK1H, PR0L, PR0H, PR1L, and PR1H registers.

Caution The BRK instruction is not one of the above-listed interrupt request hold instructions. However, the software interrupt activated by executing the BRK instruction causes the IE flag to be cleared. Therefore, even if a maskable interrupt request is generated during execution of the BRK instruction, the interrupt request is not acknowledged.

Figure 18-18 shows the timing at which interrupt requests are held pending.

Figure 18-18. Interrupt Request Hold



Remarks 1. Instruction N: Interrupt request hold instruction

2. Instruction M: Instruction other than interrupt request hold instruction

3. The ××PR (priority level) values do not affect the operation of ××IF (interrupt request).

Table 20-1. Operation Statuses During Reset Period

Item			During Reset Period
System clock			Clock supply to the CPU is stopped.
	Main system clock	f_{IH}	Operation stopped
		f_X	Operation stopped (X1 and X2 pins are input port mode)
		f_{EXCLK}	Clock input invalid (EXCLK pin is input port mode)
	f_{IL}		Operation stopped
CPU			
Flash memory			
RAM			Operation stopped (The value, however, is retained when the voltage is at least the power-on clear detection voltage.)
Port (latch)			Operation stopped
16-bit timer		X0	
		X1	
16-bit timer/event counter 00			
8-bit timer/event counter 51			
8-bit timer H1			
Watchdog timer			
A/D converter			
Operational amplifier (AMP, PGA)			
Comparators 0 to 2			
Serial interface		UART6/DALI	
		CSI11	
		IICA	
Multiplier			
External interrupt			
Power-on-clear function			Operable
Low-voltage detection function			Operation stopped (however, operation continues at LVI reset)
On-chip debug function			Operation stopped

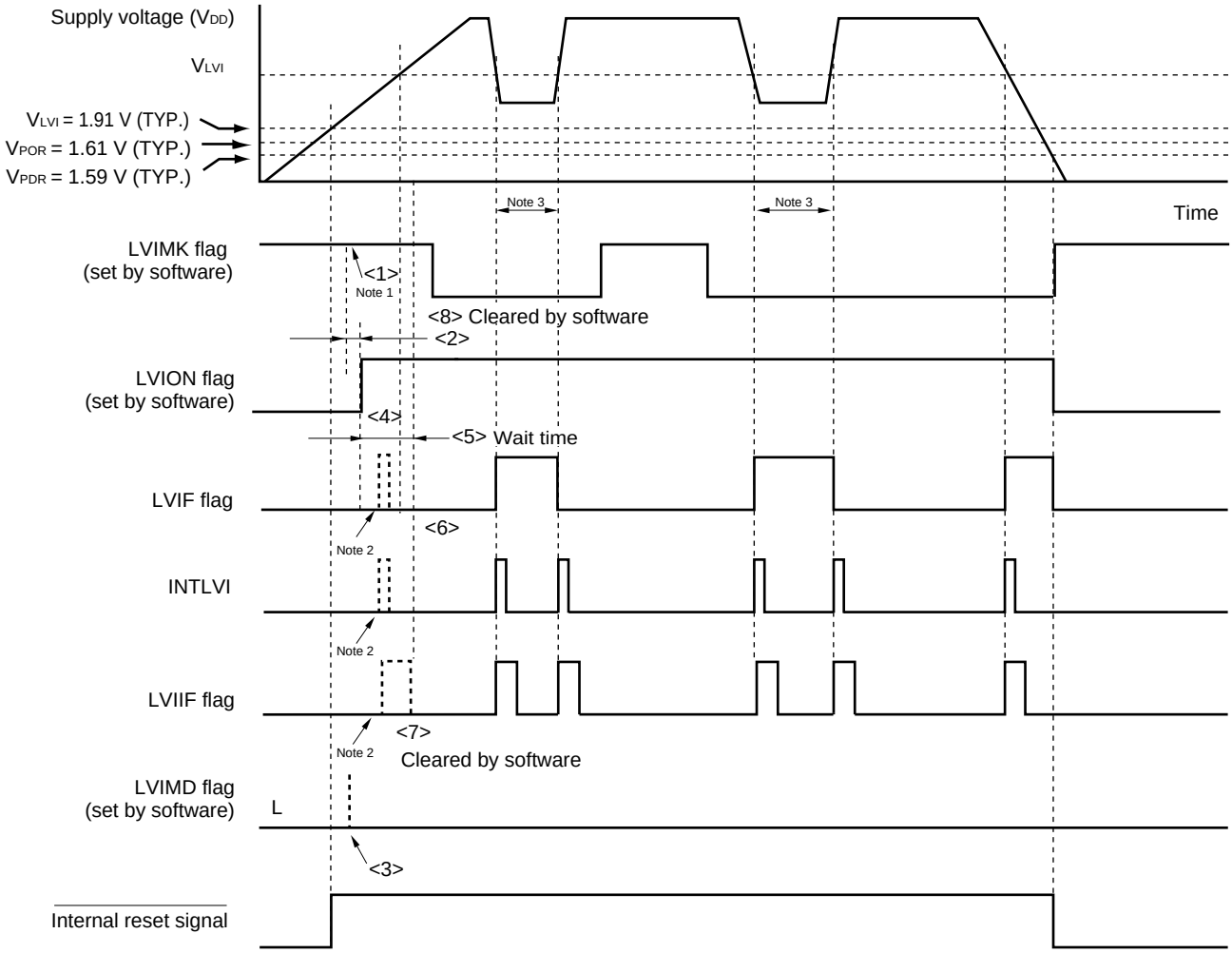
Remarks 1. f_{IH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{IL}: Internal low-speed oscillation clock

2. The functions mounted depend on the product. Refer to **1.4 Block Diagram** and **1.5 Outline of Functions**.

(2) When LVI default start function enabled is set (LVISTART = 1)

The setting when operation starts and when operation stops is the same as described in **22.4.2 (1) When LVI default start function stopped is set (LVISTART = 0)**.

Figure 22-7. Timing of Low-Voltage Detector Interrupt Signal Generation (LVISTART = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVI operation is disabled (clears LVION) when the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

Remarks 1. <1> to <8> in Figure 22-7 above correspond to <1> to <8> in the description of "When starting operation" in **22.4.2 (1) When LVI default start function stopped is set (LVISTART = 0).**

2. V_{POR}: POC power supply rise detection voltage
V_{PDR}: POC power supply fall detection voltage

Table 25-9. Processing Time for Each Command When PG-FP5 Is Used (Reference) (2/2)

(3) Products with internal ROMs of the 16 KB: μPD78F0742, 78F0744, 78F0746, 78F0752, 78F0754, 78F0756

Command of PG-FP5	Port: UART-Internal-OSC (Internal high-speed oscillation clock (f_{IH}: 8 MHz (typ.)), Speed: 500,000 bps
Signature	0.5 s (typ.)
Blankcheck	0.5 s (typ.)
Erase	1 s (typ.)
Program	2.5 s (typ.)
Verify	1.5 s (typ.)
E.P.V	2.5 s (typ.)
Checksum	1 s (typ.)
Security	0.5 s (typ.)

Caution When executing boot swapping, do not use the E.P.V. command with the dedicated flash memory programmer.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P02, P30 to P37, P60, P61	−10	mA
		Total of all pins −40 mA	P00 to P02	−15	mA
			P30 to P37, P60, P61	−25	mA
	I_{OH2}	Per pin	P20 to P27, P70	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I_{OL1}	Per pin	P00 to P02, P30 to P37, P60, P61	30	mA
		Total of all pins 120 mA	P00 to P02	45	mA
			P30 to P37, P60, P61	75	mA
	I_{OL2}	Per pin	P20 to P27, P70	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T_A			−40 to +105	°C
Storage temperature	T_{stg}			−65 to +150	°C

Cautions 1. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2. The value of the current that can be run per pin must satisfy the value of the current per pin and the total value of the currents of all pins.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P37, P121, P122, P125		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P20 to P27, P70	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH3}	P60, P61 (I/O port mode)		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P00 to P02, P30 to P36, $\overline{\text{RESET}}$, EXCLK		0.8V_{DD}		V_{DD}	V
	V_{IH5}	P60, P61 (SMBus input mode)	3.4 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}			V
			2.7 V ≤ V_{DD} < 3.4 V	2.1			V
	V_{IH6}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P37, P121, P122, P125		0		0.3V_{DD}	V
	V_{IL2}	P20 to P27, P70	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
	V_{IL3}	P60, P61 (I/O port mode)		0		0.3V_{DD}	V
	V_{IL4}	P00 to P02, P30 to P36, $\overline{\text{RESET}}$, EXCLK		0		0.2V_{DD}	V
	V_{IL5}	P60, P61 (SMBus input mode)	3.4 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			2.7 V ≤ V_{DD} < 3.4 V	0		0.8	V
	V_{IL6}	X1, X2		0		0.1	V
Output voltage, high	V_{OH1}	P00 to P02, P30 to P37, P60, P61	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH1} = –2.5 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27, P70	AV_{REF} = V_{DD}, I_{OH2} = –100 μA	V_{DD} – 0.5			V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Caution For P122/EXCLK, the value of V_{IH} and V_{IL} differs according to the input port mode or external clock mode.
Make sure to satisfy the DC characteristics of EXCLK in external clock input mode.

28.6 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = AV_{SS} = 0 V)

- **Basic characteristics**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
V_{DD} supply current	I_{DD}						4.5	14	mA
Number of rewrites per chip	C_{erwr}	1 erase + 1 write after erase = 1 rewrite Note 1	In normal power mode (RMC = 00H)	When a flash memory programmer is used, and the self-programming libraries provided by Renesas Electronics are used	Retention: 15 years	1000			Times
				When the EEPROM emulation libraries (the rewritable ROM size is 4 KB) provided by Renesas Electronics are used	Retention: 5 years	10000			Times
			In low power consump-tion mode (RMC = 56H)	When the self-programming libraries Note 2, and the EEPROM emulation libraries (the rewritable ROM size is 4 KB) provided by Renesas Electronics are used	Retention: 5 years	1000			Times
Operating temperature		When a flash memory programmer is used: 10 to 40 °C, during self-programming: –40 to +105 °C							
Operating voltage range		In normal power mode (RMC = 00H)		When a flash memory programmer is used		2.7 to 5.5 V@8 MHz (MAX.)			
				During self-programming		2.7 to 5.5 V@20 MHz (MAX.)			
		In low power consumption mode (RMC = 56H)		During self-programming		2.7 to 5.5 V@5 MHz (MAX.)			

Notes 1. When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

2. Only the data area can be rewritten.

APPENDIX C REVISION HISTORY

C.1 Major Revisions in This Edition

Page	Description	Classification
Throughout		
–	Update of URL	–
CHAPTER 6 16-BIT TIMERS X0 AND X1		
p. 207-215	Addition of **6.4 Operation of 16-Bit Timer/Event Counter 00**	(c)
p. 216, 218, 219, 224, 225	• Duty = (Set value of TXnCR1[Note1] – Set value of TXnCR0 [Note 1]) / (Set value of TXnCR1 + 1) Addition of Note1	(c)
p. 218, 220, 223, 227	Modification of Figure 6-28, 6-30, 6-32, 6-34 PWM Output Timing	(c)
CHAPTER 11 A/D CONVERTER		
p. 397	Modification of description in **(6) Input impedance of ANI0 to ANI8 pins**	(a)
CHAPTER 28 ELECTRICAL SPECIFICATIONS		
p. 710	Modification of Remarks	(a)

(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents