Renesas Electronics America Inc - UPD78F0754MC-CAA-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	DALI, I²C, LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0754mc-caa-ax

Table 2-3. Pin I/O Circuit Types (78K0/IA2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/TI000/INTP0/<TOH1>/<TI51>	5-AQ	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
ANI0/P20/AMP-[Note 1]	11-P		<Digital input setting> Independently connect to AV_{REF} or V_{SS} via a resistor. <Analog input setting and digital output setting> Leave open[Note 3].
ANI1/P21/AMPOUT[Note 1]/PGAIN[Note 1]	11-O		
ANI2/P22/AMP+[Note 1]	11-N		
ANI3/P23/CMP2+	11-Q		
ANI4/P24/CMP0+			
ANI5/P25/CMP1+			
P31/TOX00/INTP2/TOOLC1	5-AQ		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P32/TOX01/INTP3/TOOLD1			
P33/TOX10			
P34/TOX11/INTP4/<TOH1>/<TI51>			
P60/SCLA0/TxD6	5-AS		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave this pin open at low-level output after clearing the output latch of the port to 0.
P61/SDAA0/RxD6			
P121/X1/TOOLC0[Note 2]/<TI000>/<INTP0>	37-A	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122/X2/EXCLK/TOOLD0[Note 2]			
$\overline{\text{RESET}}$/P125	42-A		Connect directly to V_{DD} or via a resistor.
AV_{REF}	–	–	Connect directly to V_{DD}.

Notes 1. μPD78F0753, 78F0754 (products with operational amplifier) only

2. Use recommended connection above in input port mode (refer to **Figure 5-2 Format of Clock Operation Mode Select Register (OSCCTL)**) when these pins are not used.

3. If this pin is left open when specified as an analog input pin, the input voltage level might become undefined. It is therefore recommended to leave this pin open after specifying it as a digital output pin.

Cautions 1. ANI0/P20/AMP-, ANI1/P21/AMPOUT/PGAIN, ANI2/P22/AMP+, ANI3/P23/CMP2+, ANI4/P24/CMP0+, and ANI5/P25/CMP1+ are set in the analog input mode after release of reset.

2. Pin function of $\overline{\text{RESET}}$/P125 is set in the external reset input after release of reset.

Remark Functions in angle brackets < > can be assigned by setting the input switch control register (MUXSEL).

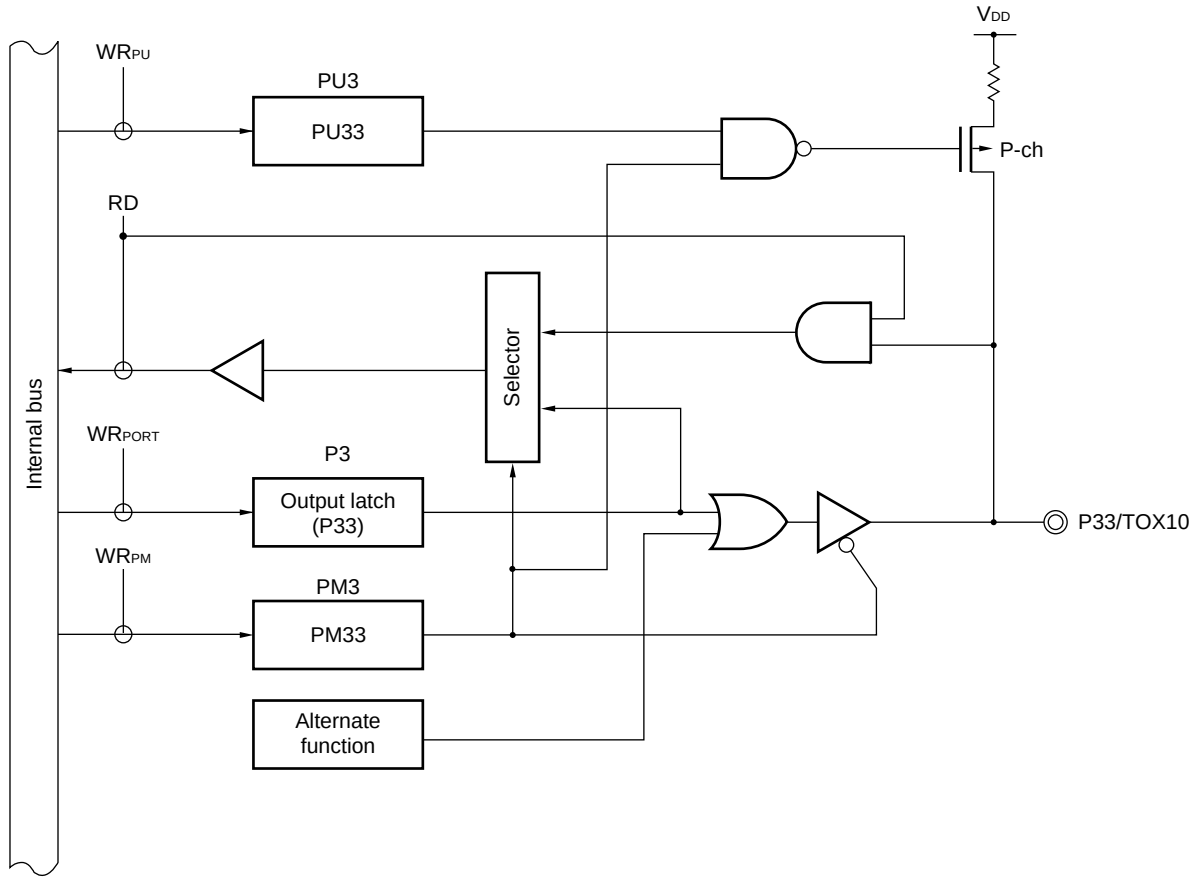
Table 3-8. Special Function Register List : 78K0/IB2 (30 Pins) (6/7)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FFA1H	MCM	0	0	0	0	0	<XSEL>	<MCS>	<MCM0>	R/W	√	√	–	00H	177
FFA2H	MOC	<MSTOP>	0	0	0	0	0	0	0	R/W	√	√	–	80H	176
FFA3H	OSTC	0	0	0	MOST11	MOST13	MOST14	MOST15	MOST16	R	√	√	–	00H	178, 606
FFA4H	OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	R/W	–	√	–	05H	179, 607
FFA5H	IICA	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	482
FFA6H	SVA0	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	482
FFA7H	IICACTL0	<IICE0>	<LREL0>	<WREL0>	<SPIE0>	<WTIM0>	<ACKE0>	<STT0>	<SPT0>	R/W	√	√	–	00H	484
FFA8H	IICACTL1	<WUP>	0	<CLD0>	<DAD0>	<SMC0>	<DFC0>	0	0	R/W	√	√	–	00H	493
FFA9H	IICAF0	<STCF>	<IICBSY>	0	0	0	0	<STCEN>	<IICRSV>	R/W	√	√	–	00H	491
FFAAH	IICAS0	<MSTS0>	<ALD0>	<EXC0>	<COI0>	<TRC0>	<ACKD0>	<STD0>	<SPD0>	R	√	√	–	00H	489
FFABH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFACH	RESF	0	0	0	WDTRF	0	0	0	LVIRF	R	–	√	–	00H[Note]	628
FFADH	IICWL	–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	495
FFAEH	IICWH	–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	495
FFAFH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFB0H	TX1CR1	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	204
FFB1H		–	–	–	–	–	–	–	–						
FFB2H	TX1CR2	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	204
FFB3H		–	–	–	–	–	–	–	–						
FFB4H	TX1CR3	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	204
FFB5H		–	–	–	–	–	–	–	–						
FFB6H	TX1CCR0	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	204
FFB7H		–	–	–	–	–	–	–	–						
FFB8H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFB9H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFBAH	TMC00	0	0	0	0	TMC003	TMC002	TMC001	<OVF00>	R/W	√	√	–	00H	263
FFBBH	PRM00	ES110	ES100	ES010	ES000	0	0	PRM001	PRM000	R/W	√	√	–	00H	268
FFBCH	CRC00	0	0	0	0	0	CRC002	CRC001	CRC000	R/W	√	√	–	00H	264

Note The reset value of RESF varies depending on the reset source.

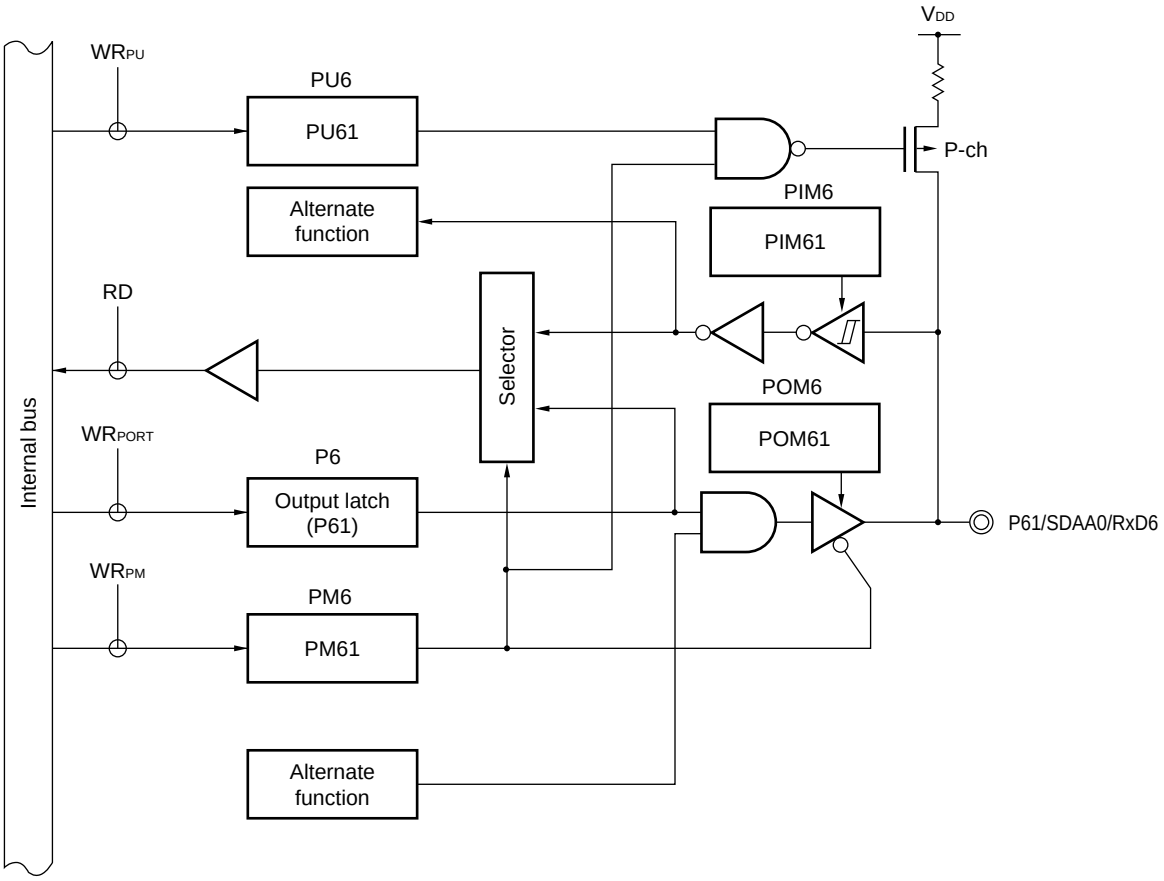
Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

Figure 4-15. Block Diagram of P33



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 4-21. Block Diagram of P61



P6: Port register 6
PU6: Pull-up resistor option register 6
PM6: Port mode register 6
PIM6: Port input mode register 6
POM6: Port output mode register 6
RD: Read signal
WR××: Write signal

4.6 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P20 is an output port, P21 to P27 are input ports (all pin statuses are high level), and the port latch value of port 2 is 00H, if the output of output port P20 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 2 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the 78K0/Ix2 microcontrollers.

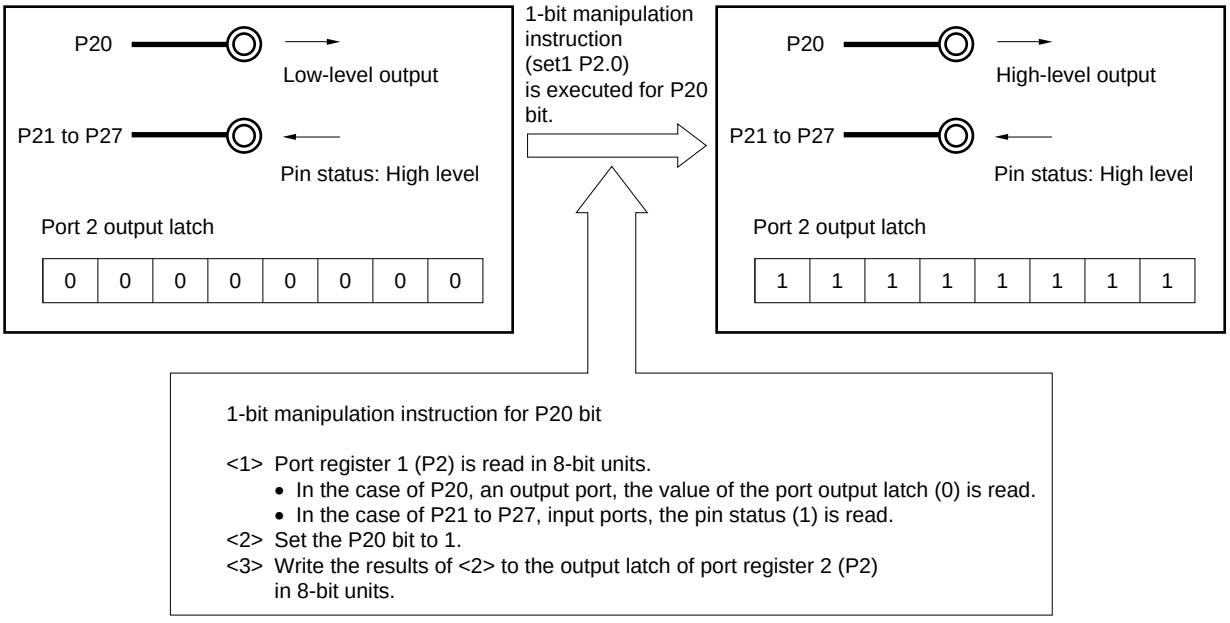
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P20, which is an output port, is read, while the pin statuses of P21 to P27, which are input ports, are read. If the pin statuses of P21 to P27 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 4-40. 1-Bit Manipulation Instruction (P20)



Remark The following instructions are 1-bit manipulation instructions.

- MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT11, NOT1

Caution When setting RSTOP to 1, be sure to confirm that the CPU operates with a clock other (MCS = 1) than the internal high-speed oscillation clock. Specifically, set under either of the following conditions.

In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock before setting RSTOP to 1.

Remarks 1. The source clock supplied to the peripheral hardware differs depending on the SELPLL setting.

SELPLL	16 bit timer X0, X1	Peripheral hardware
0	$f_{PRS} = f_{XP}$	$f_{PRS} = f_{XP}$
1	• When TXnCKS0 = 0: $f_{TMX} = 10\ f_{XP}$ (40 MHz: f_{XP} = 4 MHz operation) • When TXnCKS0 = 0: $f_{PRS} = 10\ f_{XP} \times 1/2$ (20 MHz: f_{XP} = 4 MHz operation)	$f_{PRS} = 10\ f_{XP} \times 1/2$ (20 MHz: f_{XP} = 4 MHz operation)

2. TXnCKS0: Bit 0 of the 16 bit timer Xn operation control register 0 (TXnCTL0)

(4) Main OSC control register (MOC)

This register selects the operation mode of the high-speed system clock.

This register is used to stop the X1 oscillator or to disable an external clock input from the EXCLK pin when the CPU operates with a clock other than the high-speed system clock.

MOC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 80H.

Figure 5-5. Format of Main OSC Control Register (MOC)

Address: FFA2H After reset: 80H R/W

Symbol	<7>	6	5	4	3	2	1	0
MOC	MSTOP	0	0	0	0	0	0	0

MSTOP	Control of high-speed system clock operation	
	X1 oscillation mode	External clock input mode
0	X1 oscillator operating	External clock from EXCLK pin is enabled
1	X1 oscillator stopped	External clock from EXCLK pin is disabled

Cautions 1. Clear MSTOP to 0 while the regulator mode control register (RMC) is 00H.

2. When setting MSTOP to 1, be sure to confirm that the CPU operates with a clock other (MCS = 0) than the high-speed system clock.

In addition, stop peripheral hardware that is operating on the high-speed system clock before setting MSTOP to 1.

3. Do not clear MSTOP to 0 while bit 6 (OSCSEL) of the clock operation mode select register (OSCCTL) is 0 (input port mode).

4. The peripheral hardware cannot operate when the peripheral hardware clock is stopped. To resume the operation of the peripheral hardware after the peripheral hardware clock has been stopped, initialize the peripheral hardware.

Table 5-4 shows transition of the CPU clock and examples of setting the SFR registers.

Table 5-4. CPU Clock Transition and SFR Register Setting Examples (1/3)

(1) CPU operating with internal high-speed oscillation clock (B) after reset release (A)

Status Transition	SFR Register Setting
(A) → (B)	SFR registers do not have to be set (default status after reset release).

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock (B) immediately after a reset release.)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL	MCM0
(A) → (B) → (C) (X1 clock)	0	1	0	Must be checked	1	1
(A) → (B) → (C) (external main system clock)	1	1	0	Must not be checked	1	1

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (refer to CHAPTER 28 ELECTRICAL SPECIFICATIONS).

(3) CPU clock changing from internal high-speed oscillation clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL[Note]	MCM0
(B) → (C) (X1 clock)	0	1	0	Must be checked	1	1
(B) → (C) (external main system clock)	1	1	0	Must not be checked	1	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Note The value of this flag can be changed only once after a reset release. This setting is not necessary if it has already been set.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (refer to CHAPTER 28 ELECTRICAL SPECIFICATIONS).

Remarks 1. (A) to (K) in Table 5-4 correspond to (A) to (K) in Figure 5-14.

2. EXCLK, OSCSEL: Bits 7 and 6 of the clock operation mode select register (OSCCTL)
MSTOP: Bit 7 of the main OSC control register (MOC)
XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)

CHAPTER 6 16-BIT TIMERS X0 AND X1

6.1 Functions of 16-Bit Timers X0 and X1

16-bit timers X0 and X1 are mounted onto all 78K0/Ix2 microcontroller products.

16-bit timers X0 and X1 are dedicated PWM output timers and have two outputs each, enabling the generation of up to four PWM outputs. Complementary PWM output can also be generated to control a half-bridge circuit (2 outputs) or full-bridge circuit (4 outputs). Also, by linking with a comparator or INTP0, PFC control and PWM output can be stopped urgently.

16-bit timers X0 and X1 are provided with the following functions.

(1) PWM output

- A variable pulse with any duty or cycle can be output while the timer is operating.
- The default timer output level (high or low level) can be set.

(2) A/D conversion start timing signal output

The A/D conversion start timing signal can be output by using a compare register (TXnCCR0 register: n = 0, 1).

(3) Capture function

This function captures the count value to the capture register by detecting a comparator output or an external interrupt input (INTP0).

(4) Timer start synchronization function

Up to 4 PWM outputs can be simultaneously started by combining two timer units (16-bit timers X0 and X1).

(5) Timer start/clear synchronization function

Up to 4 PWM output cycles can be synchronized by combining two timer units (16-bit timers X0 and X1).

(6) Timer output gating function (by interlocking with 8-bit timer H1)

Timer output can be gate-controlled by using the output of 8-bit timer H1 (the TOH1 output).

(7) Timer reset mode (comparator, INTP0 interlocking mode 1)

Timer output can be reset and the timer counter cleared while the comparator 0 to 2 outputs or the INTP0 input is high level. When the comparator 0 to 2 outputs or the INTP0 input go to low level, timer output restarts.

(8) Timer restart mode (comparator, INTP0 interlocking mode 2)

Timer can be restarted upon detection of the rising edge of the comparator 0 to 2 outputs or the INTP0 input.

(9) Timer output reset mode (comparator, INTP0 interlocking mode 3)

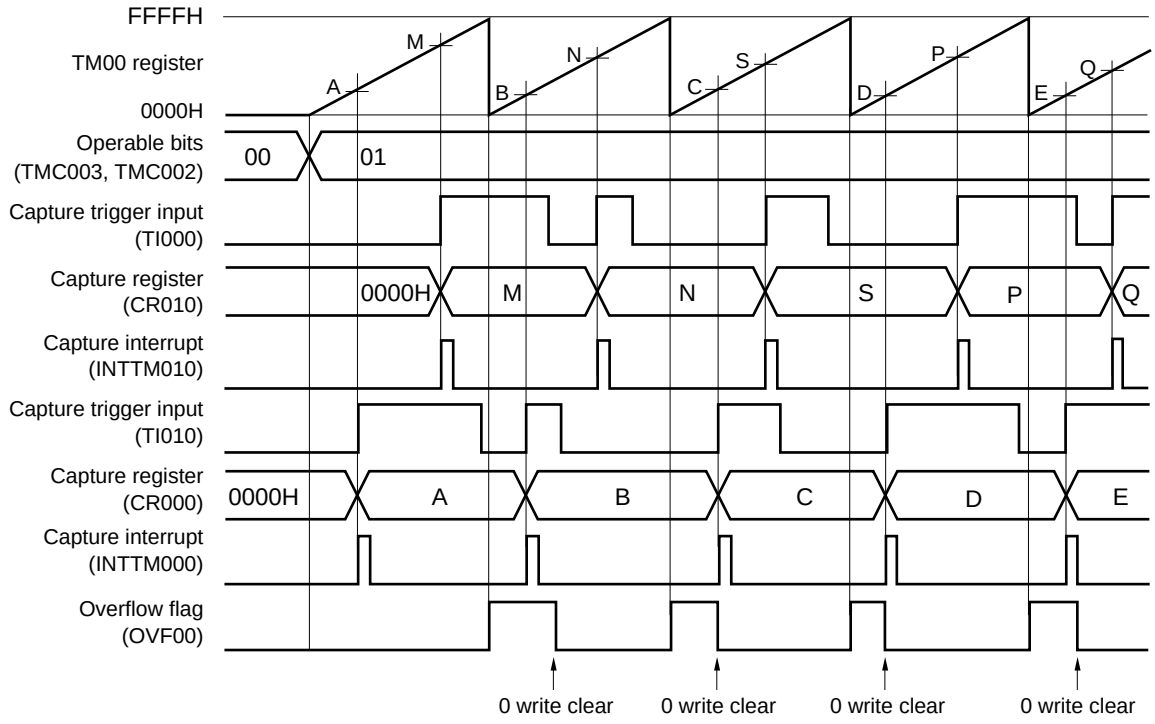
Timer output can be reset upon detection of the rising edge of the comparator 0 to 2 outputs or the INTP0 input. The reset status is cleared when the next timer interrupt occurs and timer output restarts.

(10) High-impedance output control function (by interlocking with comparator and INTP0)

Timer output can be made high impedance upon detection of the valid edge of the comparator 0 to 2 outputs or the INTP0 input.

Figure 7-38. Timing Example of Free-Running Timer Mode
(CR000: Capture Register, CR010: Capture Register) (1/2)

(a) TOC00 = 13H, PRM00 = 50H, CRC00 = 05H, TMC00 = 04H



This is an application example where the count values that have been captured at the valid edges of separate capture trigger signals are stored in separate capture registers in the free-running timer mode.
The count value is captured to CR010 when the valid edge of the TI000 pin input is detected and to CR000 when the valid edge of the TI010 pin input is detected.

(4) Port mode registers 0 and 3 (PM0, PM3)

These registers set ports 0 and 3 input/output in 1-bit units.

PM0 and PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

• 78K0/IY2

When using the <TI51>/P34/TOX11/<TOH1>/INTP4 pin for timer input, set PM34 to 1. The output latch of P34 at this time may be 0 or 1.

• 78K0/IA2, 78K0/IB2 (32 pins)

When using the <TI51>/P34/TOX11/<TOH1>/INTP4 and <TI51>/P00/TI000/<TOH1>/INTP0 pins for timer input, set PM34 and PM00 to 1. The output latches of P34 and P00 at this time may be 0 or 1.

• 78K0/IB2 (30 pins)

When using the TI51/P30/TOH1/INTP1pin for timer input, set PM30 to 1. The output latch of P30 at this time may be 0 or 1.

Figure 8-7. Format of Port Mode Register 0 (PM0)

Address: FF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	1	1	1	1	1	1	PM00

PM00	P00 pin I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 0 of the 78K0/IA2.

Figure 8-8. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

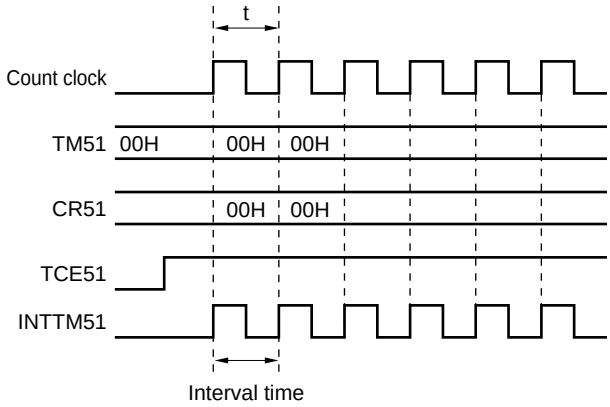
Symbol	7	6	5	4	3	2	1	0
PM3	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

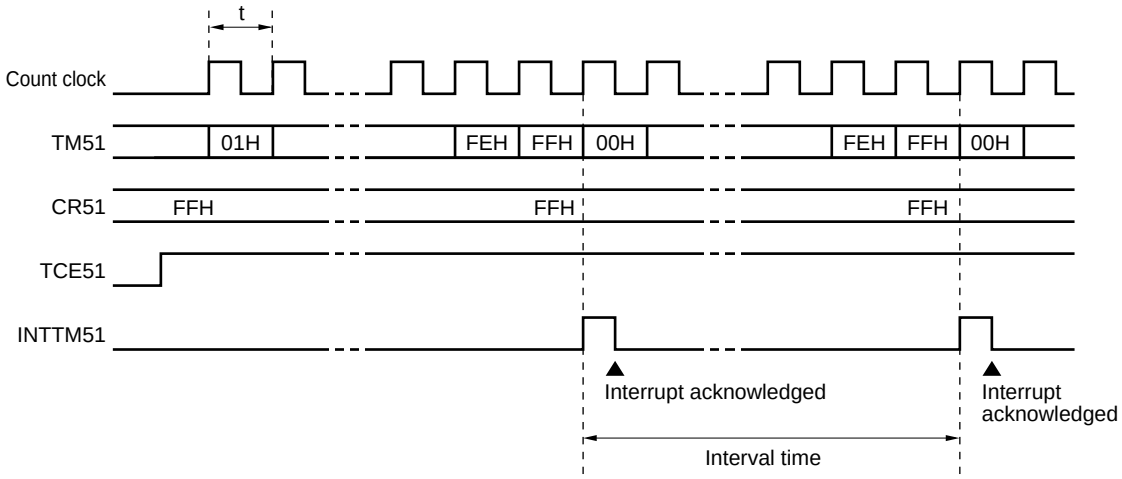
Remark The figure shown above presents the format of port mode register 3 of the 78K0/IB2 (30 pins). For the format of port mode register 3 of other products, refer to **(1) Port mode registers (PMxx)** in **4.3 Registers Controlling Port Function**.

Figure 8-9. Interval Timer Operation Timing (2/2)

(b) When CR51 = 00H



(c) When CR51 = FFH



11.4.2 Basic operation of A/D converter (timer trigger mode)

<1> Set the A/D conversion time and the operation mode by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of the A/D converter mode register 0 (ADM0).

<2> Set bit 0 (ADCE) of ADM0 to 1 to start the operation of the A/D voltage comparator.

<3> Set channels for A/D conversion to analog input by using the A/D port configuration registers 0 and 1 (ADPC0, ADPC1) and set to input mode by using port mode registers 2 and 7 (PM2, PM7).

<4> Set the PGA operation to set the PGA output and the single Amp operation to set the operational amplifier output for analog input. (refer to **CHAPTER 12 OPERATIONAL AMPLIFIER**).

<5> Select TMX0 or TMX1 synchronization by using bits 4 and 5 (ADTRG0, ADTRG1) of the analog input channel specification register (ADS).

<6> Select one channel for A/D conversion by using the analog input channel specification register (ADS).

<7> Set the timer trigger wait state by setting (1) bit 7 (ADCS) of ADM0.
(<8> to <16> are operations performed by hardware.)

<8> A conversion operation is started when a trigger signal (TMX0 or TMX1 output) is detected.

<9> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<10> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<11> Bit 9 of the successive approximation register (SAR) is set. The comparison voltage generator outputs (1/2) AV_{REF} voltage.

<12> The voltage difference between the output voltage of the comparison voltage generator and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB of SAR remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB is reset to 0.

<13> Next, bit 8 of SAR is automatically set to 1, and the operation proceeds to the next comparison. The output voltage of the comparison voltage generator is selected according to the preset value of bit 9, as described below.

- Bit 9 = 1: (3/4) AV_{REF}
- Bit 9 = 0: (1/4) AV_{REF}

The output voltage of the comparison voltage generator and sampled voltage are compared and bit 8 of SAR is manipulated as follows.

- Analog input voltage ≥ Output voltage of comparison voltage generator: Bit 8 = 1
- Analog input voltage < Output voltage of comparison voltage generator: Bit 8 = 0

<14> Comparison is continued in this way up to bit 0 of SAR.

<15> Upon completion of the comparison of 10 bits, an effective digital result value remains in SAR, and the result value is transferred to the A/D conversion result register (TMX0 synchronization: ADCRX0, ADCRX0L, TMX1 synchronization: ADCRX1, ADCRX1L) and then latched.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.

<16> Repeat steps <9> to <15>, until ADCS is cleared to 0.
To stop the A/D converter, clear ADCS to 0.
To restart A/D conversion from the status of ADCE = 1, start from <7>. To start A/D conversion again when ADCE = 0, set ADCE to 1, wait for 1 μs or longer, and start <7>. To change a channel of A/D conversion, start from <6>.

CHAPTER 12 OPERATIONAL AMPLIFIER

Item	78K0/IY2	78K0/IA2	78K0/IB2	
	16 Pins	20 Pins	30 Pins	32 Pins
Operational amplifier (products with operational amplifier only)	1 ch (PGA mode only)	1 ch (Single AMP mode and PGA mode)		

12.1 Function of Operational Amplifier

Operational amplifier is mounted onto products with operational amplifier of the 78K0/Ix2 microcontrollers. The operational amplifier has the following modes.

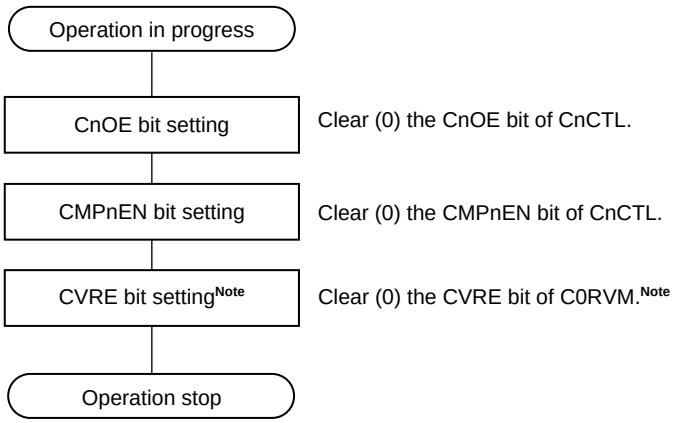
- **Single AMP mode**[Note]
  Operational amplifier has two input pins (the AMP- pin and the AMP+ pin) and one output pin (the AMPOUT pin), and can be used as single-power supply amplifier that can be externally connected.
  The amplified voltage can be used as an analog input of the A/D converter, because the AMPOUT pin is alternatively used with analog input pin of the A/D converter.

  Note Products with operational amplifier of the 78K0/IA2, 78K0/IB2 only.

- **PGA (Programmable gain amplifier) mode**
  In this mode, the analog voltage input from the PGAIN pin is amplified within the microcontroller. The gain can be selected from four types (×4, ×8, ×16, ×32).
  The amplified voltage can be used as an analog input of the A/D converter.

13.4.3 Stopping comparator operation

Figure 13-14. Example of Setting Procedure when Stopping Comparator Operation



Note Only when using the internal reference voltage.

Figure 18-4. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H) (78K0/IB2)

Address: FFE0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0L	SREIF6	PIF5	PIF4	PIF3	PIF2	PIF1 Note	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF010	TMIF000	TMIFX1	TMIFX0	TMIFH1	CSIIF11	STIF6	SRIF6

Address: FFE2H After reset: 00H R/W

Symbol	7	<6>	<5>	<4>	<3>	2	1	<0>
IF1L	0	CMPIF2	CMPIF1	CMPIF0	TMIF51	0	0	ADIF

Address: FFE3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
IF1H	0	0	0	0	0	0	0	IICAIF0

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Note 78K0/IB2 (30 pins) only

Caution When using the 78K0/IB2 (30 pins), be sure to clear bits 1, 2, and 7 of IF1L, and bits 1 to 7 of IF1H to 0. When using the 78K0/IB2 (32 pins), be sure to clear bit 2 of IF0L, bits 1, 2, and 7 of IF1L, and bits 1 to 7 of IF1H to 0.

Table 18-3. Ports Corresponding to EGPn and EGNn (1/2)

(3) 78K0/IB2 (30 pins)

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P00 or P121[Note]	INTP0
EGP1	EGN1	P30	INTP1
EGP2	EGN2	P31	INTP2
EGP3	EGN3	P32	INTP3
EGP4	EGN4	P34	INTP4
EGP5	EGN5	P02	INTP5
EGP6	EGN6	–	INTCMP0
EGP7	EGN7	–	INTCMP1
EGP8	EGN8	–	INTCMP2

(4) 78K0/IB2 (32 pins)

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P00 or P121[Note]	INTP0
EGP2	EGN2	P31	INTP2
EGP3	EGN3	P32	INTP3
EGP4	EGN4	P34	INTP4
EGP5	EGN5	P02	INTP5
EGP6	EGN6	–	INTCMP0
EGP7	EGN7	–	INTCMP1
EGP8	EGN8	–	INTCMP2

Note The pin functions can be assigned by setting the port alternate switch control register (MUXSEL).

Caution Select the port mode by clearing EGPn and EGNn to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 8: 78K0/IB2 (30 pins)
n = 0, 2 to 8: 78K0/IB2 (32 pins)

Table 20-2. Hardware Statuses After Reset Acknowledgment (1/4)

Hardware		After Reset Acknowledgment[Note 1]
Program counter (PC)		The contents of the reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Port registers 0, 2, 3, 6, 7, 12 (P0, P2, P3, P6, P7, P12) (output latches)		00H
Port mode registers 0, 2, 3, 6, 7 (PM0, PM2, PM3, PM6, PM7)		FFH
Pull-up resistor option registers 0, 3, 6 (PU0, PU3, PU6)		00H
Pull-up resistor option register 12 (PU12)		20H
Port input mode register 6 (PIM6)		00H
Port output mode register 6 (POM6)		00H
Reset pin mode register (RSTMASK)		00H
Port alternate switch control register (MUXSEL)		00H
Internal memory size switching register (IMS)		CFH[Note 3]

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. When a reset is executed in the standby mode, the pre-reset status is held even after reset.

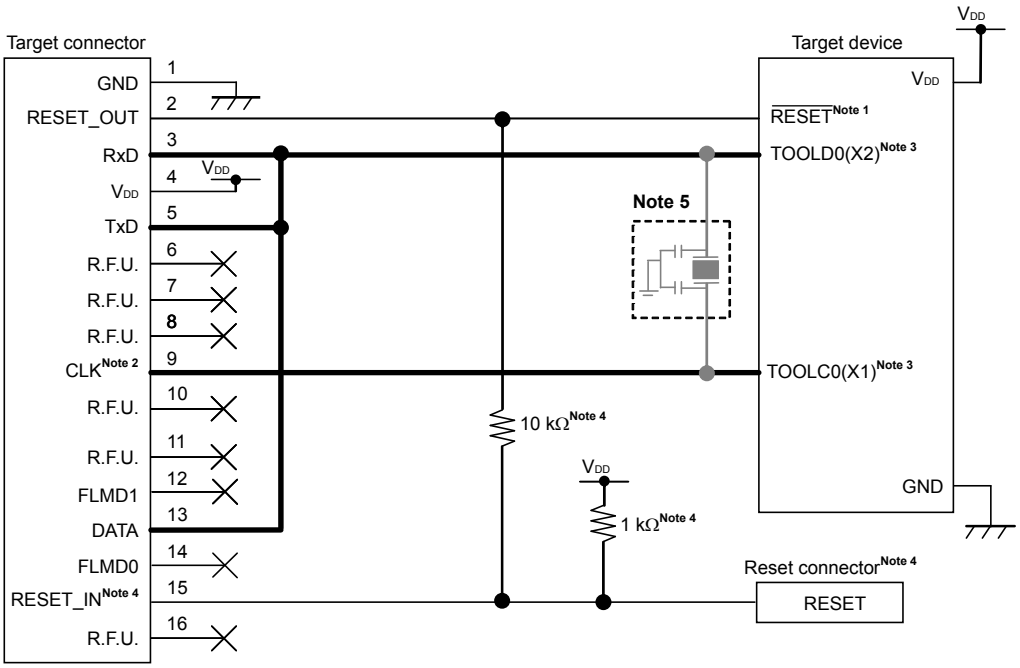
3. Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated below after release of reset.

Products			IMS	ROM Capacity	Internal High-Speed RAM Capacity
78K0/IY2	78K0/IA2	78K0/IB2			
μPD78F0740, 78F0750	–	–	61H	4 KB	384 bytes
μPD78F0741, 78F0751	μPD78F0743, 78F0753	μPD78F0745, 78F0755	42H	8 KB	512 bytes
μPD78F0742, 78F0752	μPD78F0744, 78F0754	μPD78F0746, 78F0756	04H	16 KB	768 bytes

Remark The special function registers (SFRs) mounted depend on the product. Refer to **3.2.3 Special function registers (SFRs)**.

Figure 26-1. Connection Example of QB-MINI2 and 78K0/Ix2 Microcontrollers (2/3)

(2) When using the TOOLC0 and TOOLD0 pins (with X1/X2 oscillator is used, both debugging and programming are performed)



Notes 1. If there are capacitance elements such as capacitors, on-chip debugging might not operate normally.

2. A clock signal provided on the 78K0-OCD board, a 4, 8, or 16 MHz clock signal generated in QB-MINI2, or the clock signal generated by the internal high-speed oscillator of the device can be used for the clock signal of the target device during on-chip debugging.
Only the internal high-speed oscillator of the device can be used during flash programming.

3. During on-chip debugging, the settings specified by the user program are ignored, because these pins are used as pins dedicated to on-chip debugging. However, if the pins are specified as input pins, the pins must be processed (because they are left open when QB-MINI2 is not connected.)

4. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less). For details, refer to **4.1.3 Connection of reset pin** of QB-MINI2 On-Chip Debug Emulator with Programming Function (18371E).

5. Never connect an oscillation circuit to the 78K0-OCD board during on-chip debugging and flash programming.
To prevent an oscillation circuit from not oscillating due to wiring capacitance when the target device operates (when QB-MINI2 is not connected), also consider countermeasures such as disconnecting the oscillation circuit from the target connectors by setting the jumpers.
A program that was downloaded using the debugger does not operate when QB-MINI2 is not connected.

Caution The bold lines in the figure (TOOLD0 and TOOLC0) must be designed so that the device pins are less than 30 mm from the QB-MINI2 connectors or the paths must be shielded by connecting them to GND.

(2) Non-port functions

Port		78K0/IY2	78K0/IA2	78K0/IB2	
		16 pins	20 pins	30 pins	32 pins
Power supply, ground		V_{DD}, V_{SS}, AV_{REF}		V_{DD}, AV_{REF}, V_{SS}, AV_{SS}	
Regulator		REGC			
Reset		$\overline{\text{RESET}}$			
Clock oscillation		X1, X2, EXCLK			
Interrupt		INTP0, INTP2 to INTP4		INTP0 to INTP5	INTP0, INTP2 to INTP5
Timer	TMX0, TMX1	TOX00, TOX01, TOX10, TOX11			
	TM00	TI000		TI000, TI010, TO00	TI000
	TM51	TI51			
	TMH1	TOH1			
Serial interface	UART6/ DALI	–	RxD6, TxD6		
	IICA	–	SCLA0, SDAA0		
	CSI11	–		$\overline{\text{SCK11}}$, SI11, SO11, $\overline{\text{SSI11}}$	
A/D converter		ANI0, ANI1, ANI3 to ANI5	ANI0 to ANI5	ANI0 to ANI8	
Operational amplifier[Note]		PGAIN	AMP+, AMP-, AMPOUT, PGAIN		
Comparator		CMP0+ to CMP2+		CMP0+ to CMP2+, CMPCOM	
On-chip debug function		TOOLC0, TOOLC1, TOOLD0, TOOLD1			

Note Products with operational amplifier only.

Table 30-1. Surface Mounting Type Soldering Conditions (2/2)

(2) 32-pin plastic WQFN (fine pitch) (5 x 5)

μPD78F0745K8-3B4-AX, 78F0746K8-3B4-AX, 78F0755K8-3B4-AX, 78F0756K8-3B4-AX

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: 3 times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR60-107-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Cautions 1. Do not use different soldering methods together (except for partial heating).

2. The 78K0/Ix2 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.